Jameco Part Number 1362581

PC Card Controllers

FEATURES

- **Ability to wake from $D3_{hot}$ and $D3_{cold}$**
- **Full compatiblity with the Intel 430TX (Mobile Triton II) chipset**
- **A 144-terminal low-profile QFP (PGE), 144-terminal MicroStar BGA™ ball grid array (GGU) package, or 209-terminal MicroStar BGA™ (GHK) package**
- **3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments**
- **Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards**
- **Single PC Card or CardBus slot with hot insertion and removal**
- **Burst transfers to maximize data throughput on the PCI bus and the CardBus bus**
- **Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts**
- **Serial EEPROM interface for loading subsystem ID and subsystem vendor ID**
- **Pipelined architecture allows greater than 130 Mbit/s sustained throughput from CardBus to PCI and from PCI to CardBus**
- **Interface to parallel single-slot PC Card power-switch interfaces like the TI™ TPS2211 device**
- **Up to five general-purpose I/Os**
- **Programmable output select for $\overline{\text{CLKRUN}}$**
- **Five PCI memory windows and two I/O windows available to the 16-bit PC Card socket**
- **Two I/O windows and two memory windows available to the CardBus socket**
- **Exchangeable card architecture (ExCA) compatible registers are mapped in memory and I/O space**
- **Compatibility with Intel 82365SL-DF and 82365SL registers**
- **Distributed DMA (DDMA) and PC/PCI DMA**
- **16-bit DMA on the PC Card socket**
- **Ring indicate, $\overline{\text{SUSPEND}}$, PCI $\overline{\text{CLKRUN}}$, and CardBus $\overline{\text{CCLKRUN}}$**
- **Socket-activity LED pins**
- **PCI bus lock ($\overline{\text{LOCK}}$)**
- **Advanced submicron, low-power CMOS technology**
- **Internal ring oscillator**

DESCRIPTION

The TI™ PCI1410A device is a high-performance PCI-to-PC Card controller that supports a single PC Card socket compliant with the *PC Card Standard*. The PCI1410A device provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The *PC Card Standard* retains the 16-bit PC Card specification defined in *PCI Local Bus Specification* and defines the new 32-bit PC Card, CardBus, as being capable of full 32-bit data transfers at 33 MHz. The PCI1410A device supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

The PCI1410A device is compliant with the *PCI Local Bus Specification*, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bridging transactions. The PCI1410A device also is compliant with the latest *PCI Bus Power Management Interface Specification* and *PCI Bus Power Management Interface Specification for PCI to CardBus Bridges*.

All card signals are buffered internally to allow hot insertion and removal without external buffering. The PCI1410A device is register-compatible with the Intel™ 82365SL-DF and 82365SL ExCA controllers. The PCI1410A internal data-path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1410A device also can be programmed to accept fast-posted writes to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the PCI1410A device, such as socket-activity light-emitting diode (LED) outputs, are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption, while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

Special Note: This product is for high-volume CE applications only. Contact support@ti.com for more information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCI1410AGGU	NRND	BGA	GGU	144	160	TBD	SNPB	Level-3-220C-168 HR
PCI1410APGE	NRND	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCI1410APGEG4	NRND	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

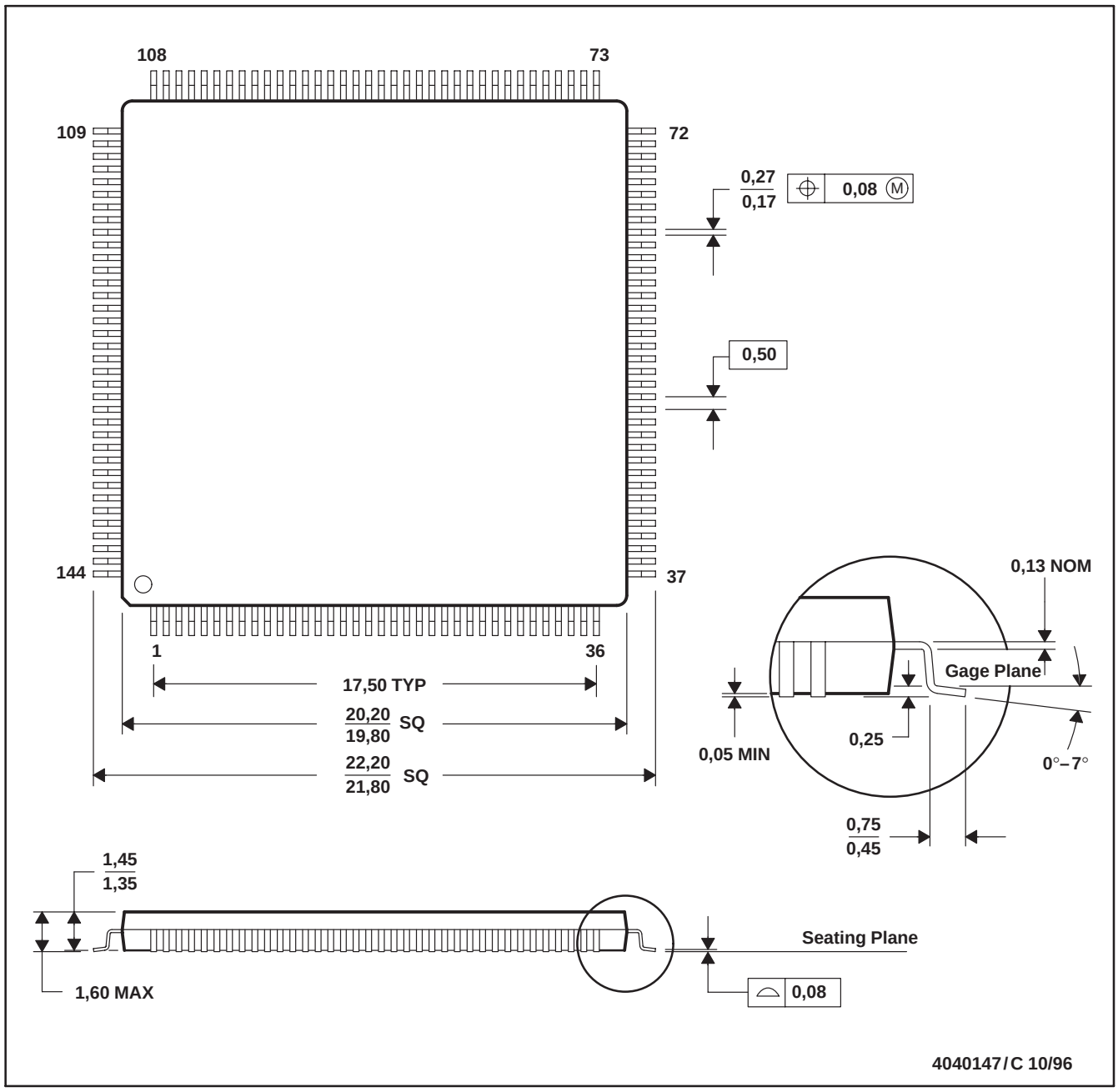
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

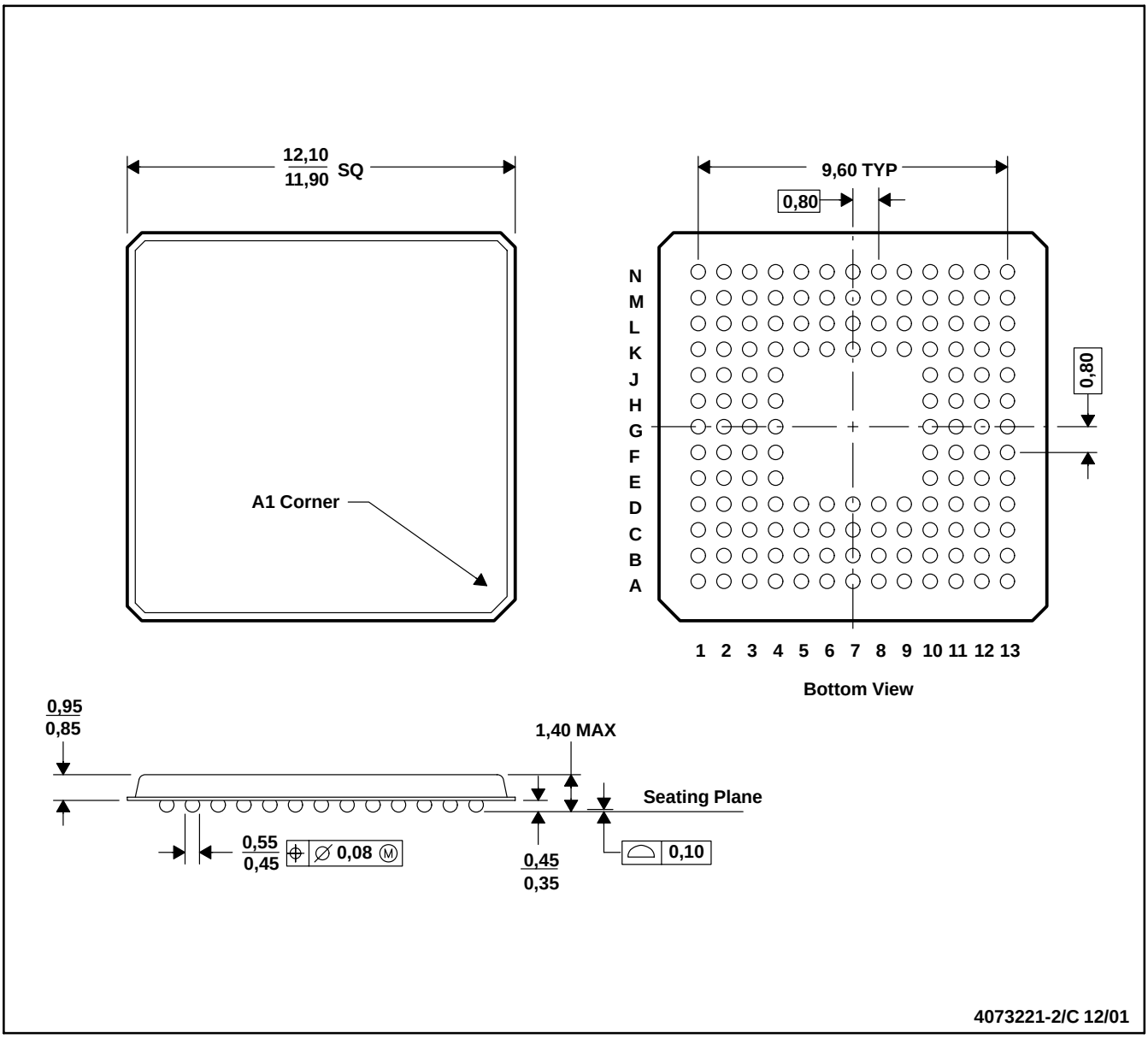
PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MPBG021C – DECEMBER 1996 – REVISED MAY 2002

GGU (S–PBGA–N144) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA™ configuration

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