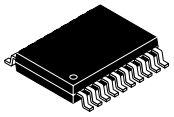


SLES022A – DECEMBER 2001

FULL DIFFERENTIAL ANALOG INPUT 24-BIT, 192-kHz STEREO A/D CONVERTER

FEATURES

- 24-Bit Delta-Sigma Stereo A/D Converter
- High Performance:
  - Dynamic Range: 112 dB (Typically)
  - SNR: 111 dB (Typically)
  - THD+N: -102 dB (Typically)
- High Performance Linear Phase antialias Digital Filter:
  - Pass-Band Ripple: ±0.005 dB
  - Stop-Band Attenuation: –100 dB
- Fully Differential Analog Input: ±2.5 V
- Audio Interface: Master or Slave Mode Selectable
- Data Formats: Left Justified, I^2S, Standard 24-Bit and DSD
- Function:
  - Peak Detection
  - Low-Cut Filter (HPF): –3 dB at 1 Hz, f_S = 48 kHz
- Sampling Rate up to 192 kHz
- System Clock: 128 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S
- Dual Power Supplies:
  - 5 V for Analog
  - 3.3 V for Digital
- Power Dissipation: 225 mW
- Small 28-Pin SSOP
- DSD Output: 1 Bit, 64 f_S
- Lead-Free Product

APPLICATIONS

- AV Amp
- MD Player
- Digital VTR
- Digital Mixer
- Digital Recorder

DESCRIPTION

The PCM1804 is a high-performance single chip stereo A/D converter with full differential analog voltage input. The PCM1804 uses a precision delta-sigma modulator and includes a linear phase antialias digital filter and HPF (low-cut filter) that removes dc offset of the input signal. The PCM1804 is suitable for a wide variety of mid-to-high grade consumer and professional applications, where excellent performance and 5-V analog supply and 3.3-V digital power supply operation are required. The PCM1804 can achieve both PCM audio and DSD format due to precision delta-sigma modulator. The PCM1804 is fabricated on an advanced CMOS process and is available in small 28-pin SSOP package.

PACKAGE/ORDERING INFORMATION

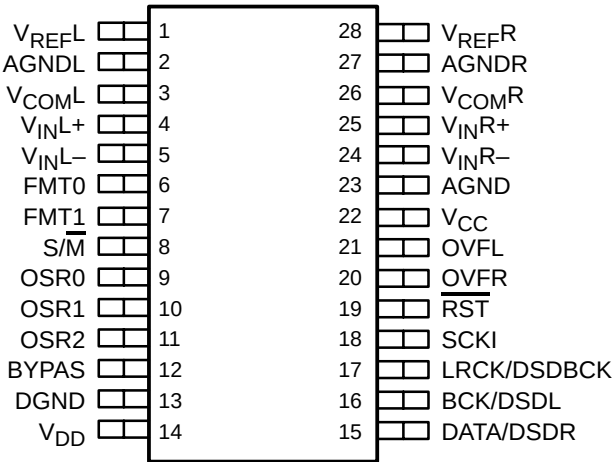
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1804DB	28-Lead SSOP	28DB	–10°C to 70°C	PCM1804DB	PCM1804DB	Tube
					PCM1804DBR	Tape and Reel

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

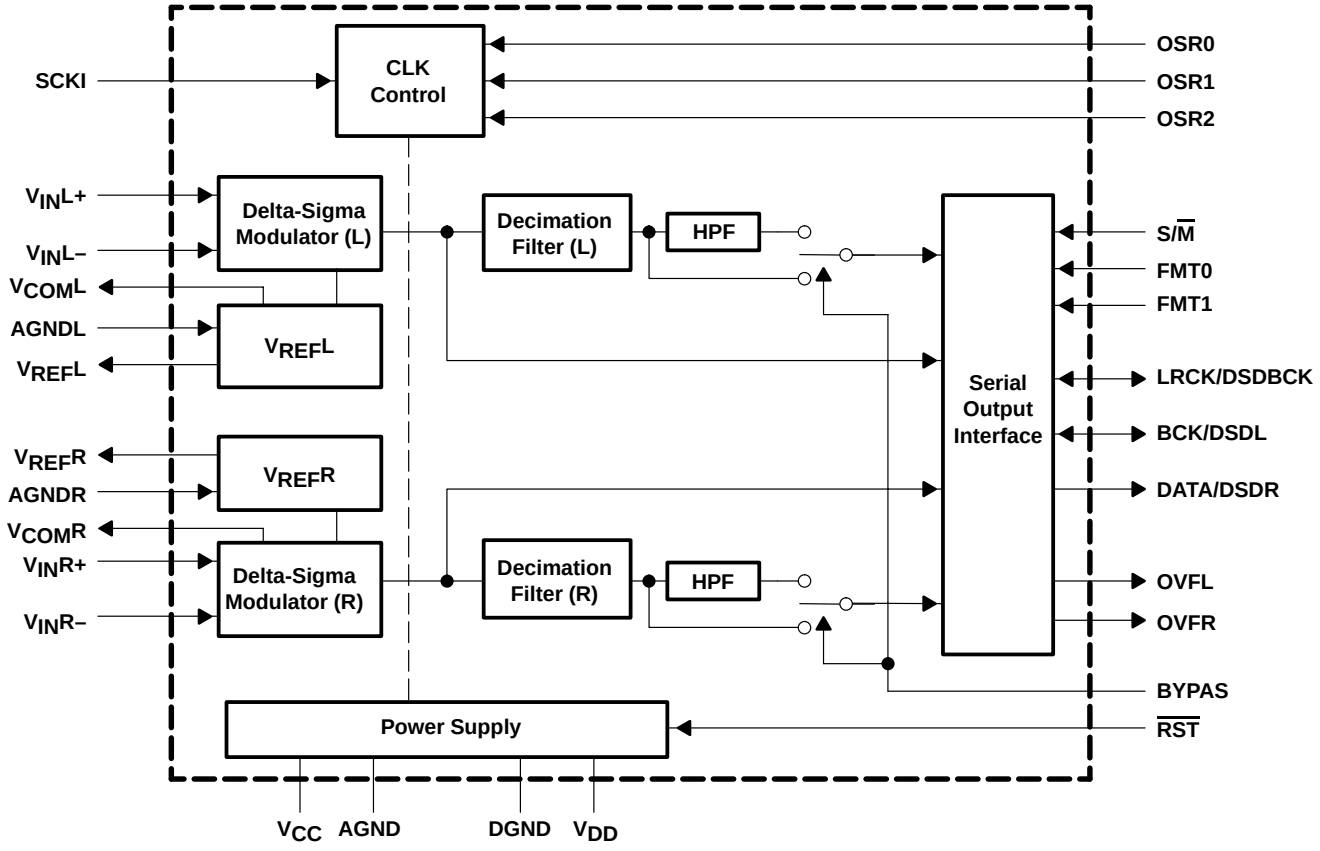
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

pin assignments

PCM1804 PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
AGND	23	–	Analog ground
AGNDL	2	–	Analog ground for $V_{REF}L$
AGNDR	27	–	Analog ground for $V_{REF}R$
BCK/DSDL	16	I/O	Bit clock input/output in PCM mode. L-channel audio data output in DSD mode. §
BYPAS	12	I	HPF bypass control. High: HPF disable, Low: HPF enable§
DATA/DSDR	15	O	L-channel and R-channel audio data output in PCM mode. R-channel audio data output in DSD mode. (DSD output, when DSD mode)
DGND	13	–	Digital ground
FMT0	6	I	Audio data format 0. See Table 5†
FMT1	7	I	Audio data format 1. See Table 5†
LRCK/DSDBCK	17	I/O	Sampling clock input / output in PCM and DSD mode. §
OSR0	9	I	Oversampling ratio 0. See Table 1 and Table 2†
OSR1	10	I	Oversampling ratio 1. See Table 1 and Table 2†
OSR2	11	I	Oversampling ratio 2. See Table 1 and Table 2†
OVFL	21	O	Overflow signal of L-channel in PCM mode. This is available in PCM mode only.
OVFR	20	O	Overflow signal of R-channel in PCM mode. This is available in PCM mode only.
$\overline{RST}$	19	I	Reset, power down input, active low†
SCKI	18	I	System clock input; 128 f_S, 256 f_S, 384 f_S, 512 f_S or 768 f_S.‡
S/$\overline{M}$	8	I	Master / slave mode selection. See Table 4.†
V_{CC}	22	–	Analog power supply
$V_{COM}L$	3	–	L-channel analog common mode voltage (2.5 V)
$V_{COM}R$	26	–	R-channel analog common mode voltage (2.5 V)
V_{DD}	14	–	Digital power supply
$V_{IN}L–$	5	I	L-channel analog input, negative pin
$V_{IN}L+$	4	I	L-channel analog input, positive pin
$V_{IN}R–$	24	I	R-channel analog input, negative pin
$V_{IN}R+$	25	I	R-channel analog input, positive pin
$V_{REF}L$	1	–	L-channel voltage reference output, requires capacitors for decoupling to AGND
$V_{REF}R$	28	–	R-channel voltage reference output, requires capacitors for decoupling to AGND

† Schmitt-trigger input with internal pulldown (51 kΩ typically), 5-V tolerant.
‡ Schmitt-trigger input, 5-V tolerant.
§ Schmitt-trigger input

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{CC}	6.5 V
V_{DD}	4 V
Ground voltage differences: AGND, AGNDL, AGNDR, DGND	±0.1 V
Digital input voltage: FMT0, FMT1, S/$\overline{M}$, OSR0, OSR1, OSR2, SCKI, $\overline{RST}$	–0.3 V to 6.5 V
BYPAS, DATA/DSDR, BCK/DSDL, LRCK/DSDBCK, OVFL, OVFR	–0.3 V to (V_{DD} + 0.3 V)
Analog input voltage: $V_{REF}L$, $V_{REF}R$, $V_{COM}L$, $V_{COM}R$, $V_{IN}L+$, $V_{IN}R+$, $V_{IN}L–$, $V_{IN}R–$	–0.3 V to (V_{CC} + 0.3 V)
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias, T_A	–40°C to 125°C
Storage temperature, T_{stg}	–55°C to 150°C
Junction temperature, T_J	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C, 10 s

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1804DB			UNIT
			MIN	TYP	MAX	
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			Standard, I^2S, left justified		
	Audio data bit length			24-bits		
	Audio data format			MSB first, 2s complement, DSD		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	High-level input voltage	See Notes 1 and 2	2		5.5	VDC
		See Note 3	2		V_{DD}	VDC
V_{IL}	Low-level input voltage	See Notes 1, 2, and 3			0.8	VDC
I_{IH}	High-level input current	V_{IN} = V_{DD}, See Note 1		65	100	µA
		V_{IN} = V_{DD}, See Note 2			±10	µA
		V_{IN} = V_{DD}, See Note 3			±100	µA
I_{IL}	Low-level input current	V_{IN} = 0 V, See Notes 1 and 2			±10	µA
		V_{IN} = 0 V, See Note 3			±50	µA
V_{OH}	High-level output voltage	I_{OH} = –1 mA, See Note 4	2.4			VDC
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, See Note 5			0.4	VDC
CLOCK FREQUENCY						
f_S	Sampling frequency		32		192	kHz
	System clock frequency	256 f_S, Single rate, See Note 5		12.288		MHz
		384 f_S, Single rate, See Note 5		18.432		MHz
		512 f_S, Single rate, See Note 5		24.576		MHz
		768 f_S, Single rate, See Note 5		36.864		MHz
		256 f_S, Dual rate, See Note 6		24.576		MHz
		384 f_S, Dual rate, See Note 6		36.864		MHz
		128 f_S, Quad rate, See Note 7		24.576		MHz
		192 f_S, Quad rate, See Note 7		36.864		MHz
DC ACCURACY						
	Gain mismatch channel-to-channel				±3	%/FSR
	Gain error (V_{IN} = –0.5 dB)				±4	%/FSR
	Bipolar zero error	HPF bypass		±0.2		%/FSR

NOTES: 1. Pins 6–11, 19: FMT0, FMT1, S/$\overline{M}$, OSR0, OSR1, OSR2, $\overline{RST}$ (Schmitt-trigger input with internal pulldown (51 kΩ typically), 5 V tolerant)
2. Pin 18: SCKI (Schmitt-trigger input, 5 V tolerant)
3. Pins 12, 16–17: BYPAS, BCK/DSDL, LRCK/DSDBCK (in slave mode, Schmitt-trigger input)
4. Pins 15–17, 20, and 21: DATA/DSDR, BCK/DSDL, LRCK/DSDBCK (in master mode), OVFR, OVFL
5. Single rate, f_S = 48 kHz
6. Dual rate, f_S = 96 kHz
7. Quad rate, f_S = 192 kHz

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		PCM1804DB			UNIT
				MIN	TYP	MAX	
DYNAMIC PERFORMANCE (see Note 8)							
THD+N	Total harmonic distortion plus noise	V_{IN} = –0.5 dB	f_S = 48 kHz, System clock = 256 f_S		–102	–95	dB
		V_{IN} = –60 dB			–49		
		V_{IN} = –0.5 dB	f_S = 96 kHz, System clock = 256 f_S		–101		
		V_{IN} = –60 dB			–47		
		V_{IN} = –0.5 dB	f_S = 192 kHz, System clock = 128 f_S		–101		
		V_{IN} = –60 dB			–47		
		V_{IN} = –0.5 dB	DSD mode		–100		
	Dynamic range (A-weighted)	V_{IN} = –60 dB	f_S = 48 kHz, System clock = 256 f_S	106	112		dB
			f_S = 96 kHz, System clock = 256 f_S		112		
			f_S = 192 kHz, System clock = 128 f_S		112		
		DSD mode			112		
	SNR (A-weighted)	f_S = 48 kHz,	System clock = 256 f_S	105	111		dB
		f_S = 96 kHz,	System clock = 256 f_S		111		
		f_S = 192 kHz,	System clock = 128 f_S		111		
		DSD mode			111		
	Channel separation	f_S = 48 kHz,	System clock = 256 f_S	97	109		dB
		f_S = 96 kHz,	System clock = 256 f_S		107		
		f_S = 192 kHz,	System clock = 128 f_S		107		
ANALOG INPUT							
	Input voltage	Differential input			±2.5		V
	Center voltage				2.5		VDC
	Input impedance	Single end			10		kΩ
DIGITAL FILTER PERFORMANCE							
	Pass-band edge	Single rate, dual rate				0.453 f_S	Hz
	Stop-band edge	Single rate, dual rate		0.547 f_S			Hz
	Pass-band ripple	Single rate, dual rate				±0.005	dB
	Stop-band attenuation	Single rate, dual rate		–100			dB
	Pass-band edge (–0.005 dB)	Quad rate				0.375 f_S	Hz
	Pass-band edge (–3 dB)	Quad rate				0.49 f_S	Hz
	Stop-band edge	Quad rate		0.77 f_S			Hz
	Pass-band ripple	Quad rate				±0.005	dB
	Stop-band attenuation	Quad rate		–135			dB
	Group delay				37/f_S		s
	HPF frequency response	–3 dB			f_S/48000		Hz

NOTE 8: f_{IN} = 1 kHz, using Audio Precision's System II, RMS mode with 20-kHz LPF and 400-Hz HPF in calculation for single rate, with 40-kHz LPF for dual and quad rate in calculation.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	PCM1804DB			UNIT
			MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS						
V_{CC}	Supply voltage range		4.75	5	5.25	VDC
V_{DD}			3	3.3	3.6	
I_{CC}	Supply current	V_{CC} = 5 V, See Notes 5, 6, and 7		35	45	mA
I_{DD}		V_{DD} = 3.3 V, See Notes 5 and 9		15	20	
		V_{DD} = 3.3 V, See Notes 6 and 9		27		
		V_{DD} = 3.3 V, See Notes 7 and 9		18		
P_D	Power dissipation	Operation, V_{CC} = 5 V, V_{DD} = 3.3 V, See Notes 5 and 9		225	290	mW
		Operation, V_{CC} = 5 V, V_{DD} = 3.3 V, See Notes 6 and 9		265		
		Operation, V_{CC} = 5 V, V_{DD} = 3.3 V, See Notes 7 and 9		235		
		Power down, V_{CC} = 5 V, V_{DD} = 3.3 V		5		
TEMPERATURE RANGE						
	Operation temperature		–10		70	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

NOTES: 5. Single rate, f_S = 48 kHz
6. Dual rate, f_S = 96 kHz
7. Quad rate, f_S = 192 kHz
9. Minimum load on DATA/DSDR (pin 15)

TYPICAL CHARACTERISTICS

single rate

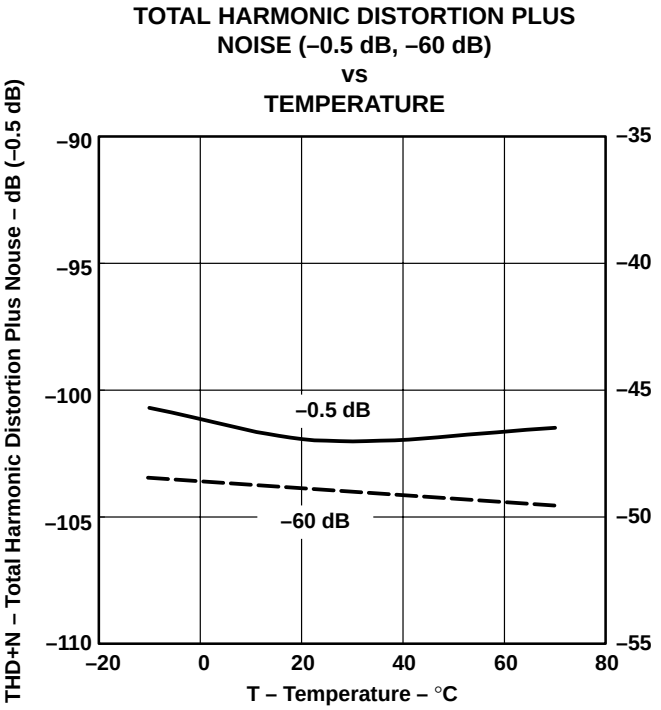


Figure 1

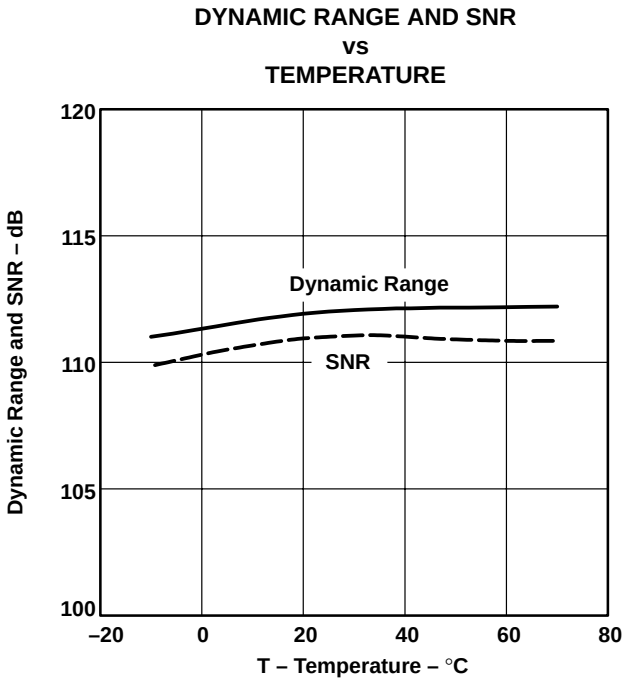


Figure 2

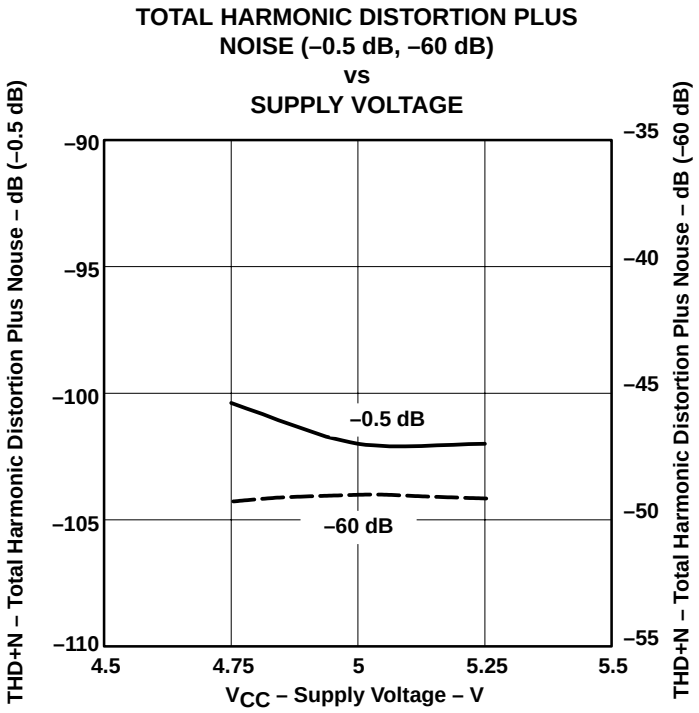


Figure 3

† All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

TYPICAL CHARACTERISTICS

single rate (continued)

DYNAMIC RANGE AND SNR vs SUPPLY VOLTAGE

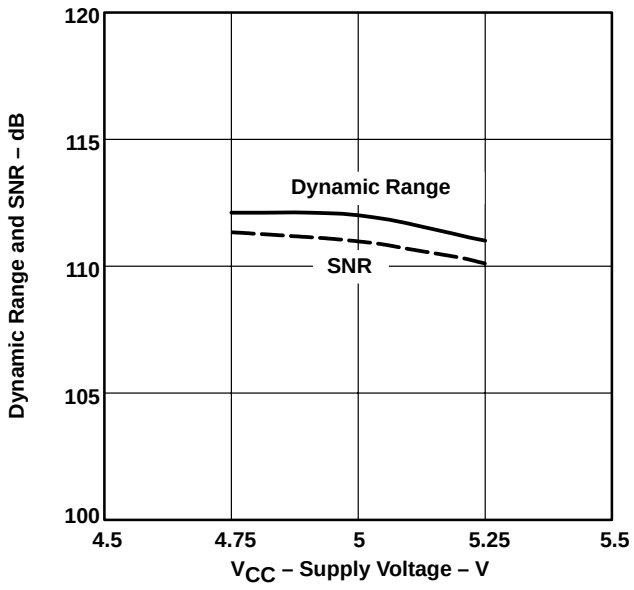


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE (–0.5 dB, –60 dB) vs SAMPLING FREQUENCY

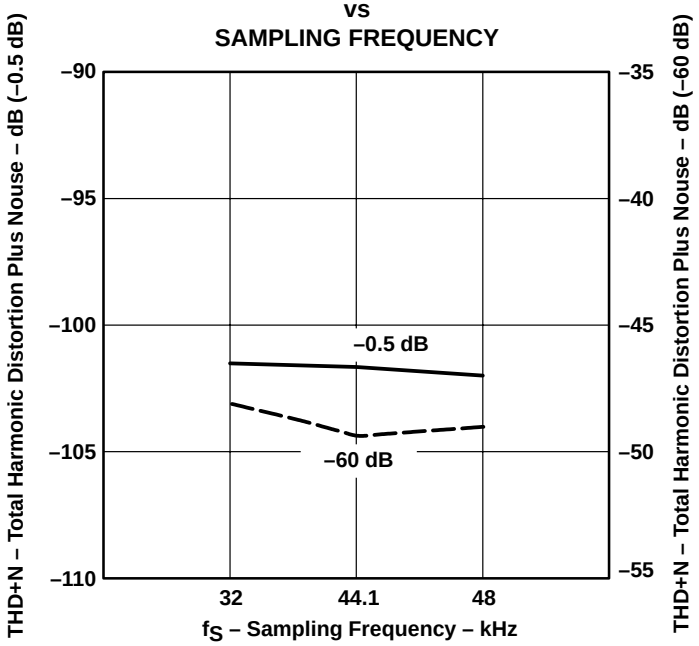


Figure 5

† All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

TYPICAL CHARACTERISTICS

single rate (continued)

DYNAMIC RANGE AND SNR vs SAMPLING FREQUENCY

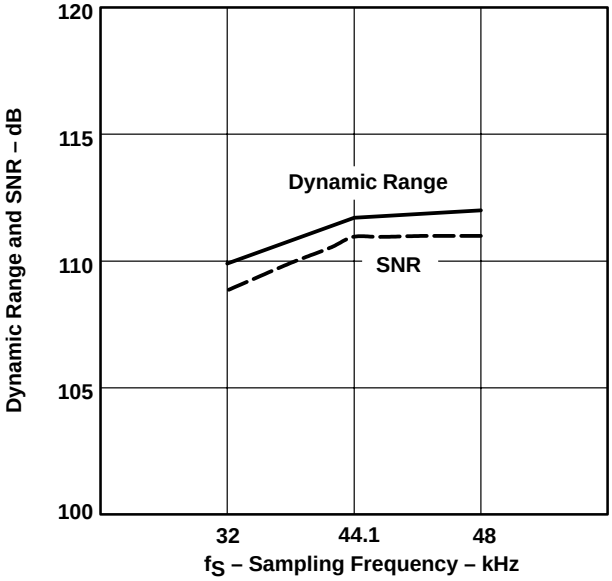


Figure 6

AMPLITUDE vs FREQUENCY

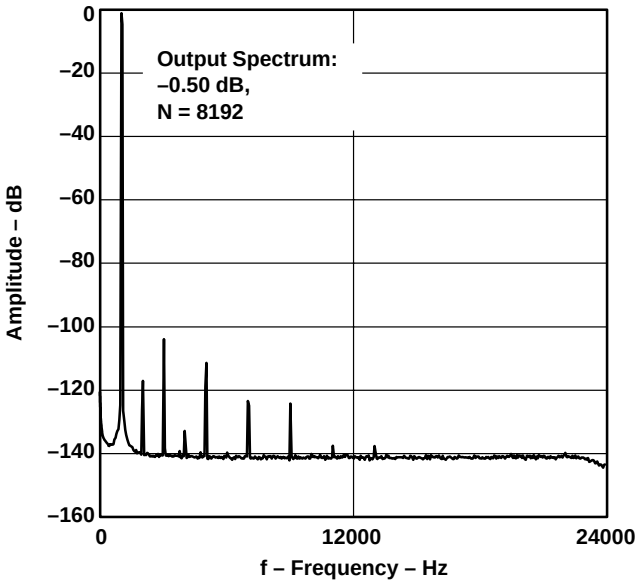


Figure 7

AMPLITUDE vs FREQUENCY

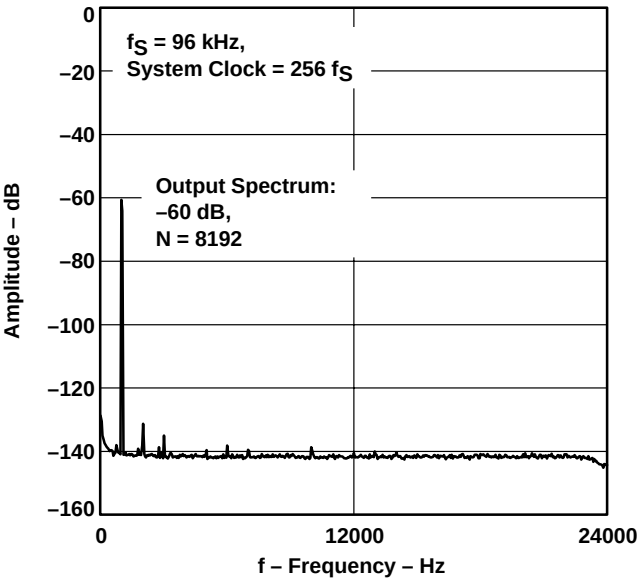


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs SIGNAL LEVEL

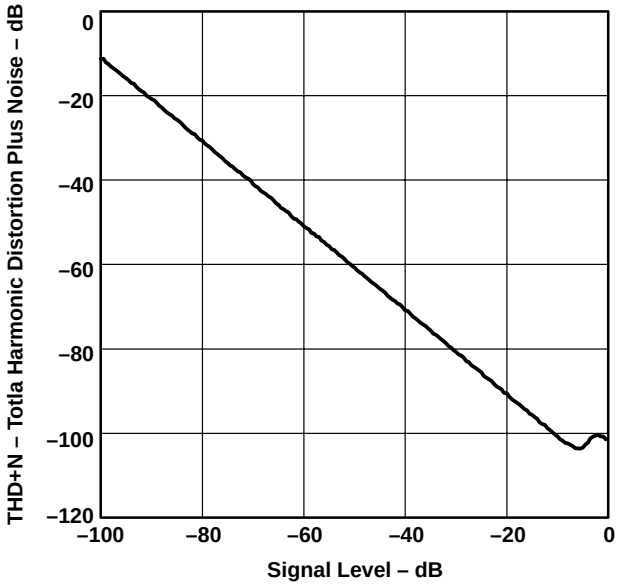


Figure 9

† All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data, unless otherwise noted.

TYPICAL CHARACTERISTICS

dual rate

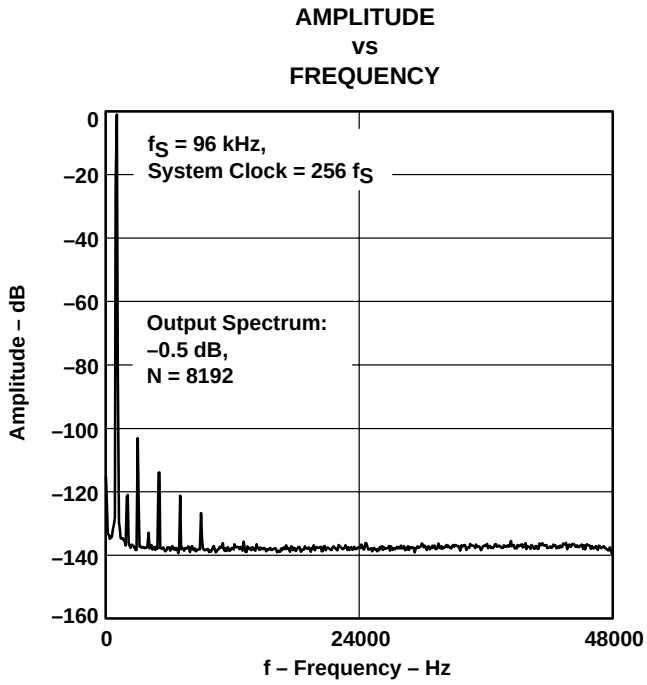


Figure 10

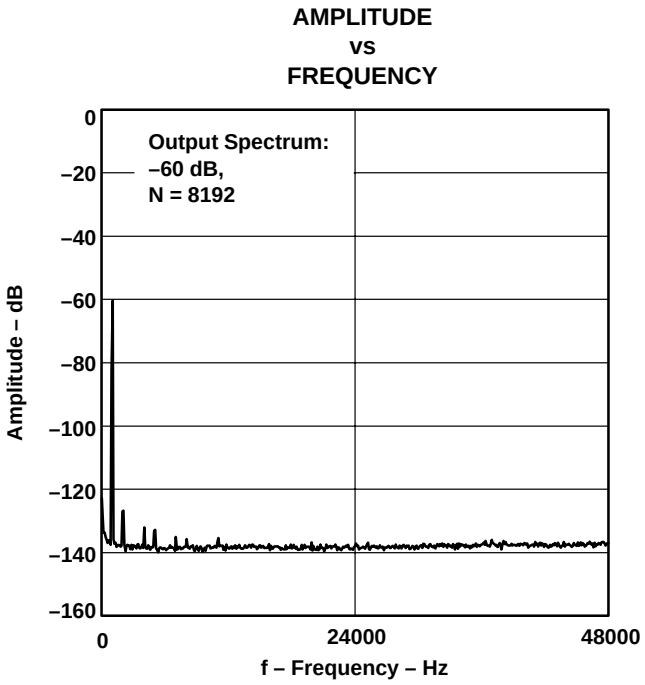


Figure 11

quad rate

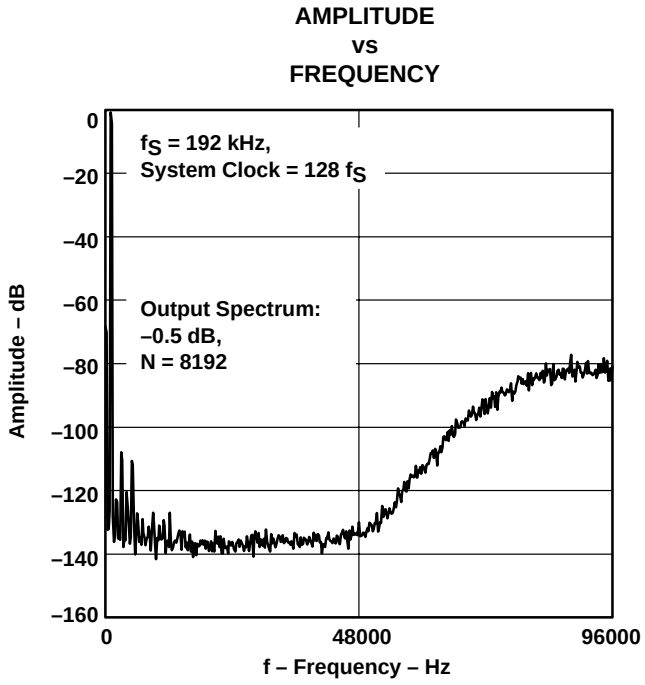


Figure 12

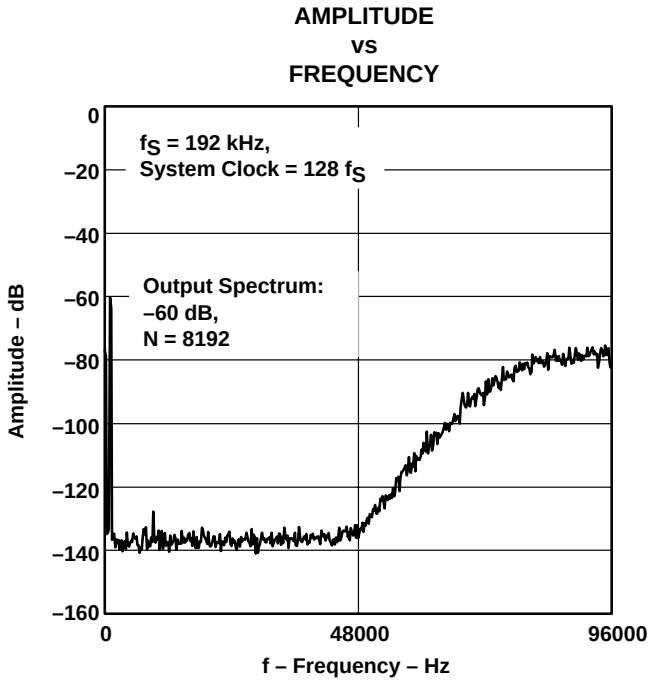


Figure 13

† All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, 24-bit data, unless otherwise noted.

TYPICAL CHARACTERISTICS

DSD mode

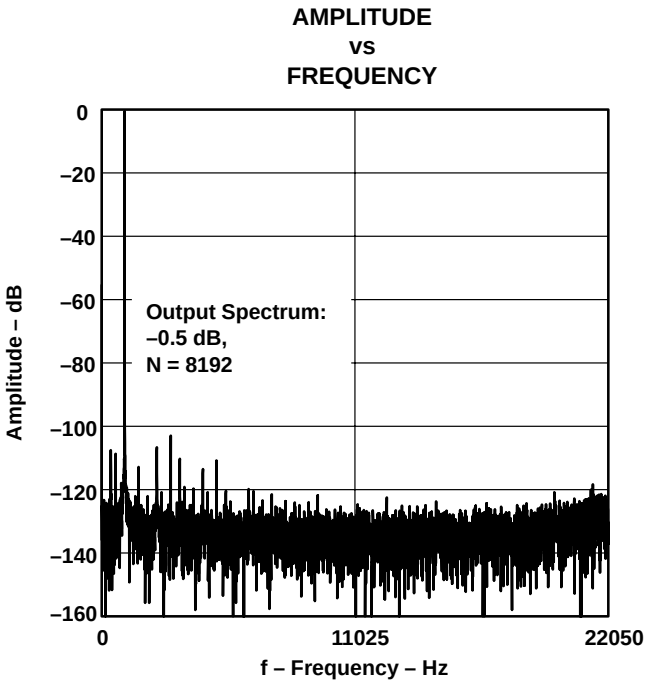


Figure 14

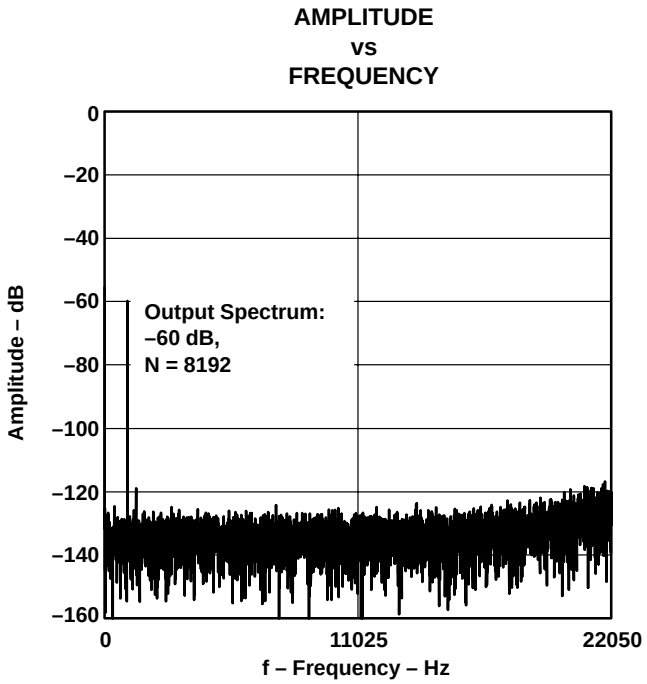


Figure 15

† All specifications at T_A = 25°C, V_{CC} = 3.3 V, V_{DD} = 5 V, master mode, f_S = 44.1 kHz, system clock = 16.9344 MHz, unless otherwise noted.

linear phase antialias digital filter frequency response

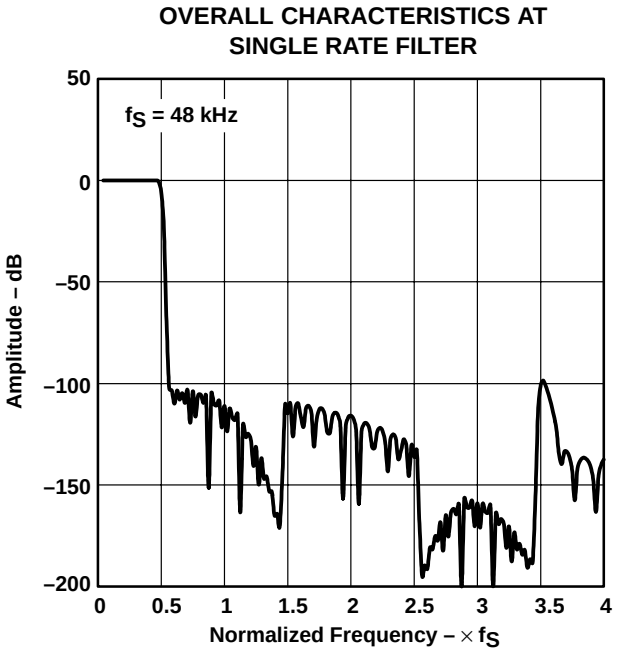


Figure 16

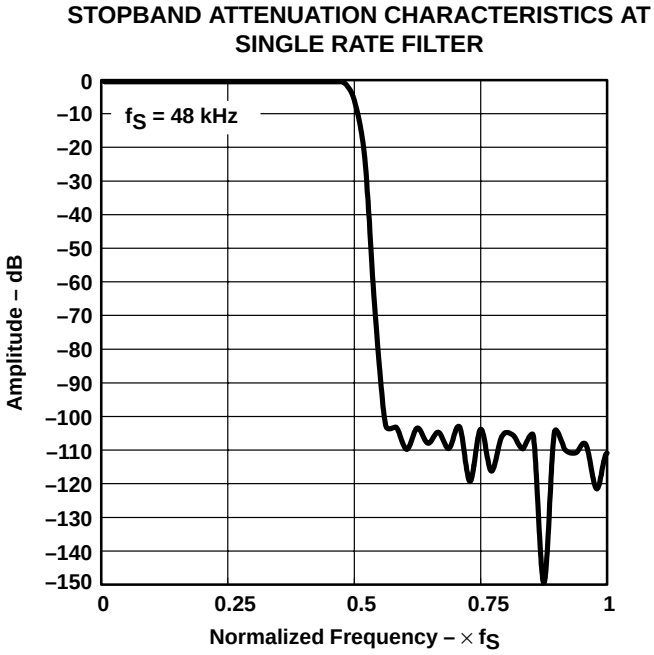


Figure 17

TYPICAL CHARACTERISTICS

linear phase antialias digital filter frequency response (continued)

PASSBAND RIPPLE CHARACTERISTICS AT SINGLE RATE FILTER

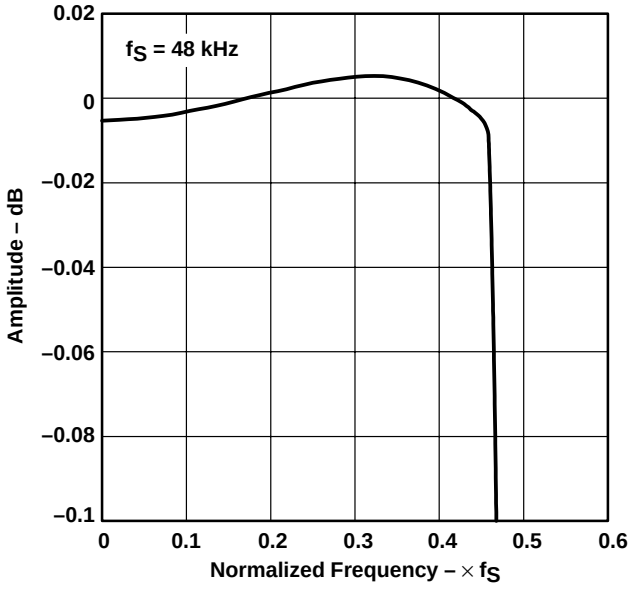


Figure 18

TRANSIENT BAND CHARACTERISTICS AT SINGLE RATE FILTER

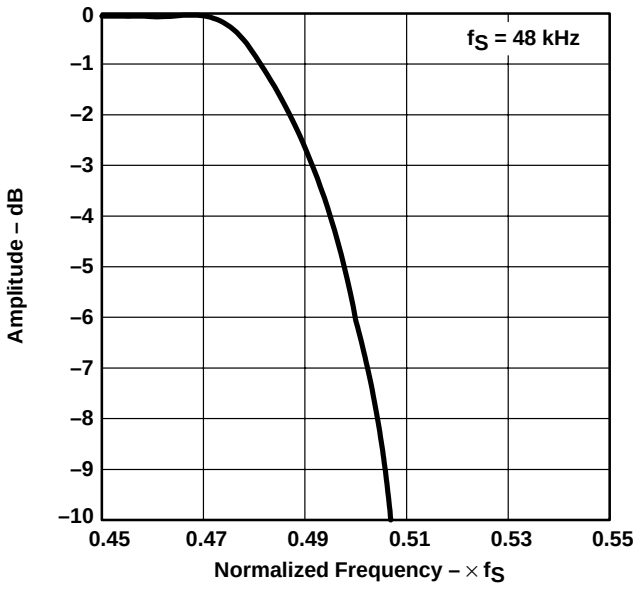


Figure 19

OVERALL CHARACTERISTICS AT DUAL RATE FILTER

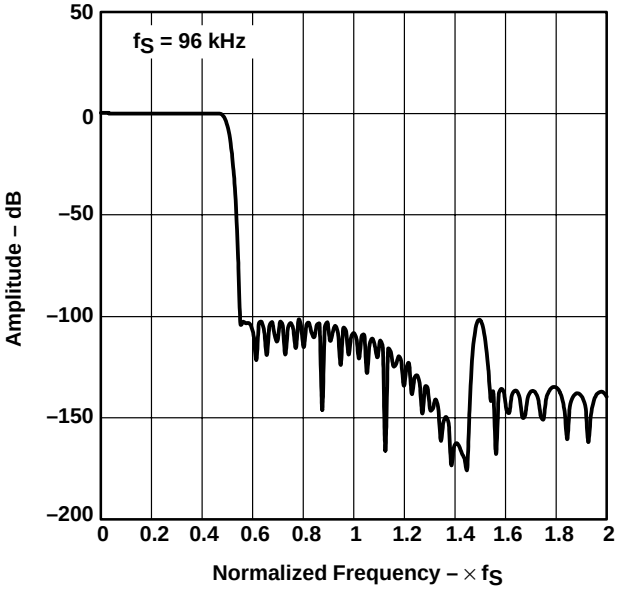


Figure 20

STOPBAND ATTENUATION CHARACTERISTICS AT DUAL RATE FILTER

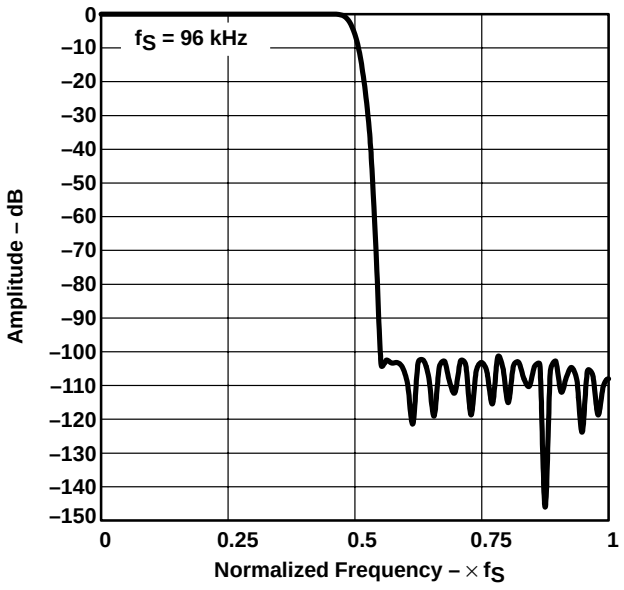


Figure 21

TYPICAL CHARACTERISTICS

linear phase antialias digital filter frequency response (continued)

PASSBAND RIPPLE CHARACTERISTICS AT DUAL RATE FILTER

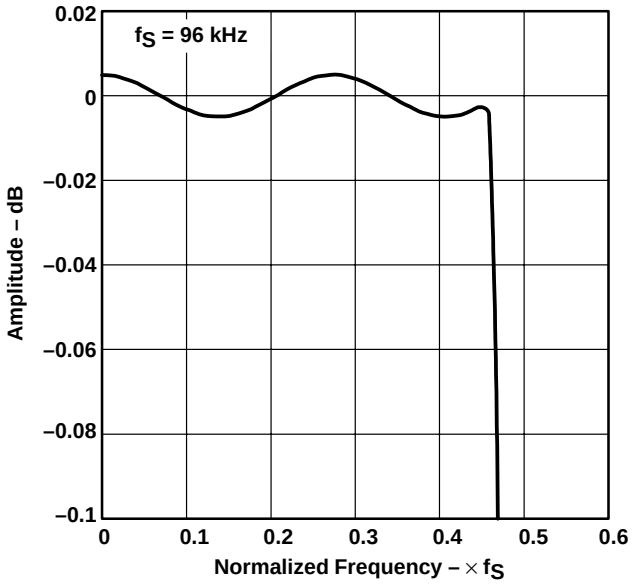


Figure 22

TRANSIENT BAND CHARACTERISTICS AT DUAL RATE FILTER

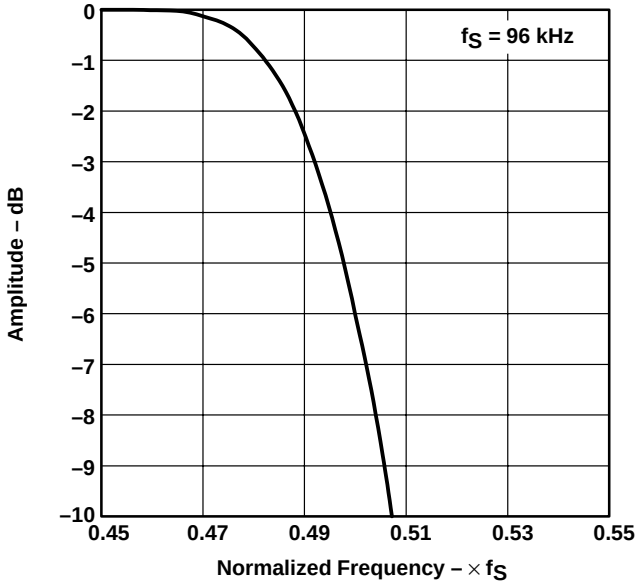


Figure 23

OVERALL CHARACTERISTICS AT QUAD RATE FILTER

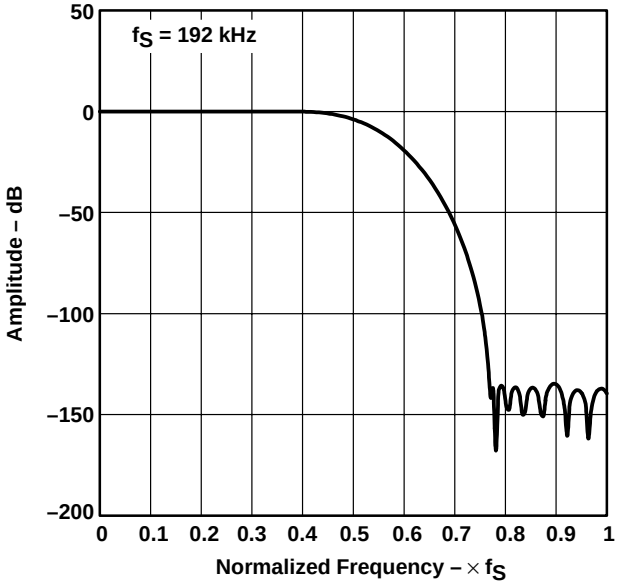


Figure 24

STOPBAND ATTENUATION CHARACTERISTICS AT QUAD RATE FILTER

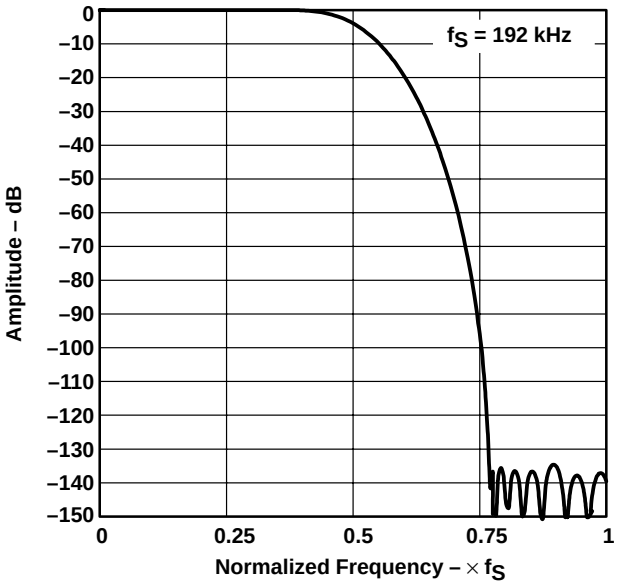


Figure 25

TYPICAL CHARACTERISTICS

linear phase antialias digital filter frequency response (continued)

PASSBAND RIPPLE CHARACTERISTICS AT QUAD RATE FILTER

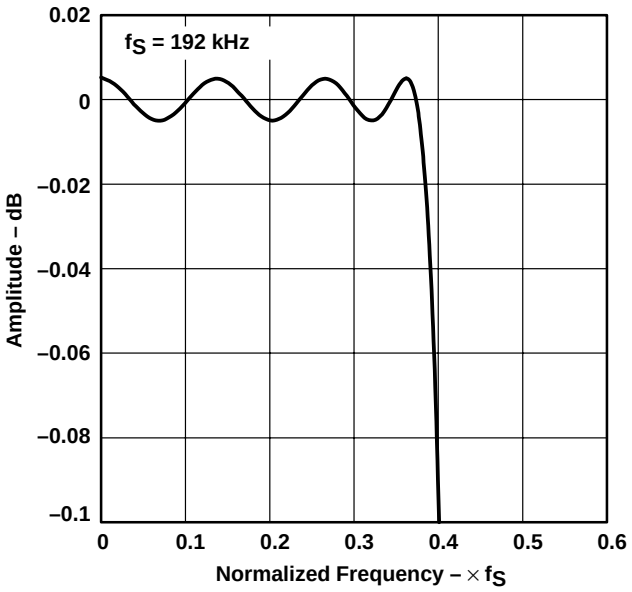


Figure 26

TRANSIENT BAND CHARACTERISTICS AT QUAD RATE FILTER

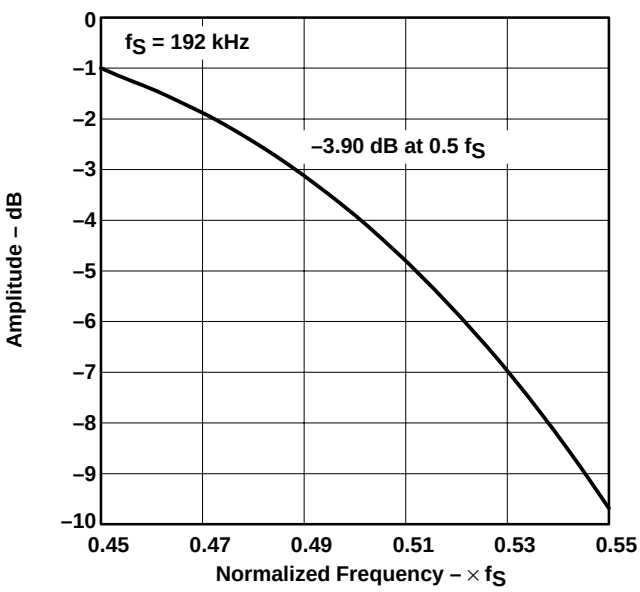


Figure 27

HPF (low-cut filter) frequency response

STOPBAND CHARACTERISTICS

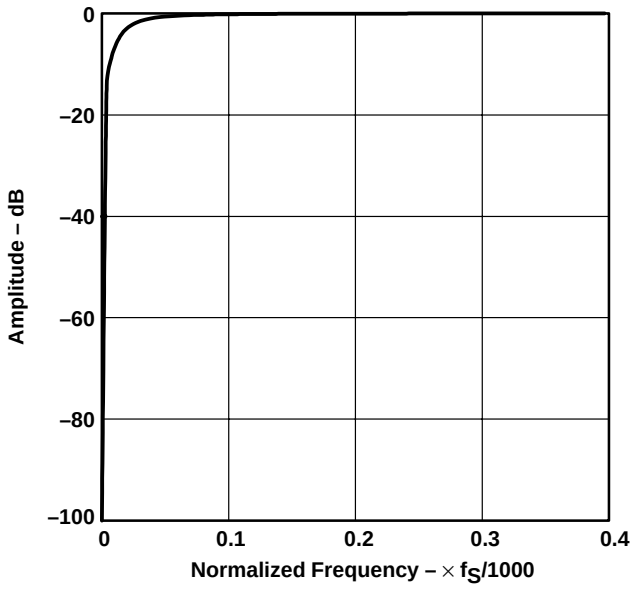


Figure 28

PASSBAND CHARACTERISTICS

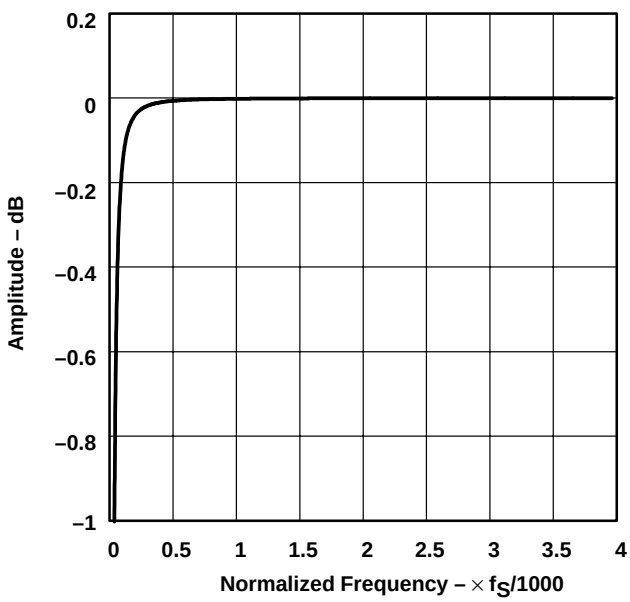


Figure 29

PRINCIPLES OF OPERATION

theory of operation

The PCM1804 consists of a band-gap reference, a delta-sigma modulator with full differential architecture for L-channel and R-channel respectively, a decimation filter with a low-cut filter, and a serial interface circuit. Figure 1 illustrates the total architecture of the PCM1804. An on-chip high-precision reference with 10-μF external capacitor(s) provides all the reference voltage needed in the PCM1804, and it defines the full-scale voltage range of both channels. Full differential architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at ×128, ×64, and ×32 oversampling rate for oversampling ratio. The single rate, dual rate, and quad rate eliminate the external sample-hold amp. Figure 31 illustrates how the PCM1804 for each oversampling ratio decimates the modulator output down to PCM data when the modulator is running at 6.144 MHz. The delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The oversampled data stream from the delta-sigma modulator is converted to a 1 f_S, 24-bit digital signal, while removing high-frequency noise components by a decimation filter. The dc components of the signal are removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats and master/slave modes. The PCM1804 also has a DSD output mode. The PCM1804 can output directly the signal from the modulators to the DSDL (pin 16) and the DSDR (pin 15).

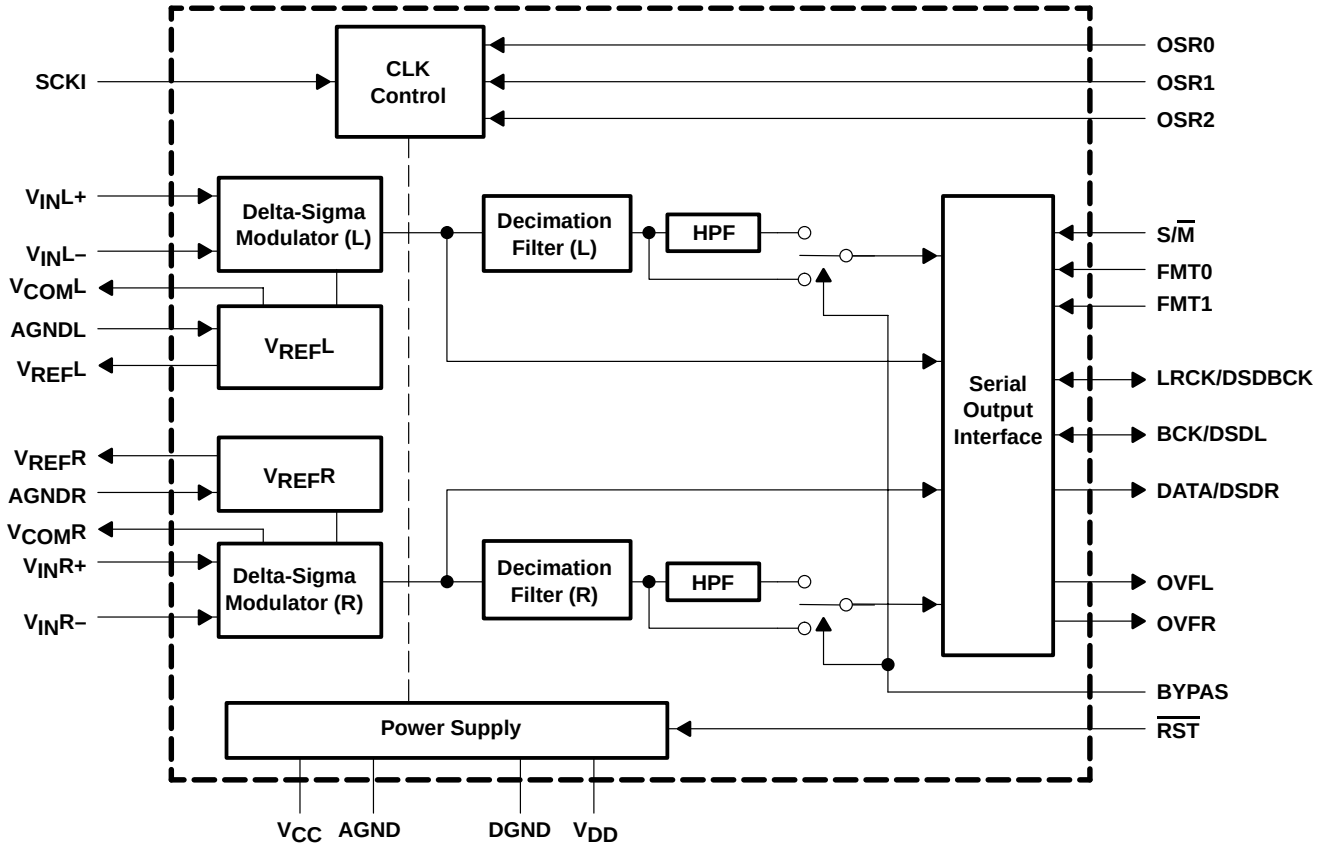


Figure 30. Total Block Diagram of PCM1804

PRINCIPLES OF OPERATION

theory of operation (continued)

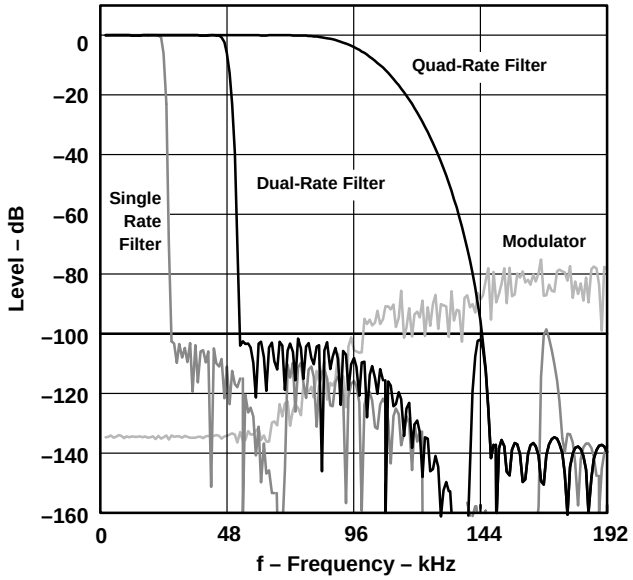
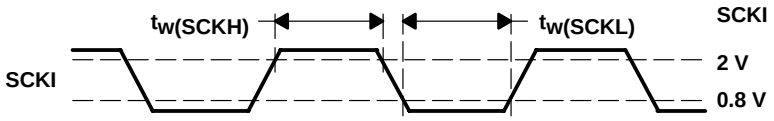


Figure 31. Spectrum of Modulator Output and Decimation Filter

system clock input

The PCM1804 supports 128 f_S, 192 f_S (only master mode at quad rate), 256 f_S, 384 f_S, 512 f_S, and 768 f_S as a system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 18). Table 1 shows the relationship of typical sampling frequency and the system clock frequency, and Figure 32 shows system clock timing. In master mode, the system clock rate is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in Table 1. In slave mode, the system clock rate is automatically detected. In DSD mode, OSR2 (pin 11), OSR1 (pin 10), OSR0 (pin 9), and the system clock frequency are fixed as shown in Table 1 and 3.



PARAMETER	MIN	UNIT
System clock pulse width high, $t_{W(SCKH)}$	11	ns
System clock pulse width low, $t_{W(SCKL)}$	11	ns

Figure 32. System Clock Input Timing

PRINCIPLES OF OPERATION

power-on and reset functions

The PCM1804 has both an internal power-on reset circuit and an $\overline{RST}$ (pin 19). For internal power-on reset, initialize (reset) is done automatically at the timing the power supply V_{DD} exceeds 2 V (typ) and V_{CC} exceeds 4 V (typ). $\overline{RST}$ accepts external forced reset, and a low level on $\overline{RST}$ initiates the reset sequence. As the internal pull-down resistor terminates $\overline{RST}$, no connection of $\overline{RST}$ is equal to the low-level input. As the system clock is used as a clock signal of the reset circuit, the system clock has to be supplied as soon as power is supplied; more specifically, at least three system clocks are required prior to $V_{DD} > 2$ V, $V_{CC} > 4$ V and $\overline{RST}$ = high. During either $V_{DD} < 2$ V (typ), $V_{CC} < 4$ V (typ), or $\overline{RST}$ = low, and $1/f_S$ (max) count after $V_{DD} > 2$ V (typ), $V_{CC} > 4$ V (typ) and $\overline{RST}$ = high, the PCM1804 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of $1116/f_S$ is passed. Figure 33 and Figure 34 illustrate the internal power on reset and external reset timing. Figure 35 illustrates the digital output for power on reset and control. The PCM1804 needs $\overline{RST}$ = low when SCKI, LRCK, BCK (in slave mode), and control pins are changed.

power-down function

The PCM1804 has a power-down feature that is controlled by the $\overline{RST}$ (pin 19). Entering the power-down mode is done by keeping the $\overline{RST}$ low-level input for over $65536/f_S$. In the master mode, the SCKI (pin 18) is used as the clock signal of the power-down counter. While in the slave mode, the SCKI (pin 18) and the LRCK (pin 17) are used as the clock signal. The clock(s) has to be supplied until the power-down sequence completes. As soon as $\overline{RST}$ goes high, the PCM1804 starts the reset-release sequence described in the *power-on and reset functions* section.

oversampling ratio

Oversampling ratio is selected by OSR2 (pin 11), OSR1 (pin 10) and OSR0 (pin 9) as shown in Table 1 and Table 2. The PCM1804 needs $\overline{RST}$ = low when OSR2, OSR1, and OSR0 pins are changed.

Table 1. Oversampling Ratio in Master Mode

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate ($\times$ 128 f_S)	768 f_S
Low	Low	High	Single rate ($\times$ 128 f_S)	512 f_S
Low	High	Low	Single rate ($\times$ 128 f_S)	384 f_S
Low	High	High	Single rate ($\times$ 128 f_S)	256 f_S
High	Low	Low	Dual rate ($\times$ 64 f_S)	384 f_S
High	Low	High	Dual rate ($\times$ 64 f_S)	256 f_S
High	High	Low	Quad rate ($\times$ 32 f_S)	192 f_S†
High	High	High	Quad rate ($\times$ 32 f_S)	128 f_S
High	Low	Low	DSD mode ($\times$ 64 f_S)	384 f_S
High	Low	High	DSD mode ($\times$ 64 f_S)	256 f_S

† Only master mode at quad rate

PRINCIPLES OF OPERATION

Table 2. Oversampling Ratio in Slave Mode

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate ($\times$ 128 f_S)	Automatically detected
Low	Low	High	Dual rate ($\times$ 64 f_S)	Automatically detected
Low	High	Low	Quad rate ($\times$ 32 f_S)	Automatically detected
Low	High	High	Reserved	–
High	Low	Low	Reserved	–
High	Low	High	Reserved	–
High	High	Low	Reserved	–
High	High	High	Reserved	–

Table 3. Sampling Frequency and System Clock Frequency

OVERSAMPLING RATIO	SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (MHz)					
		128 f_S	192 f_S†	256 f_S	384 f_S	512 f_S	768 f_S
Single rate (see Note 10)	32 kHz	—	—	8.192	12.288	16.384	24.576
	44.1 kHz	—	—	11.2896	16.9344	22.5792	33.8688
	48 kHz	—	—	12.288	18.432	24.576	36.864
Dual rate (see Note 11)	88.2 kHz	—	—	22.5792	33.8688	—	—
	96 kHz	—	—	24.576	36.864	—	—
Quad rate (see Note 12)	176.4 kHz	22.5792	33.8688		—	—	—
	192 kHz	24.576	36.864	—	—	—	—
DSD mode (see Note 11)	44.1 kHz	16.9344 for 384 f_S, 11.2896 for 256 f_S					

† Only master mode

NOTES: 10. Modulator is running at 128 f_S
11. Modulator is running at 64 f_S
12. Modulator is running at 32 f_S

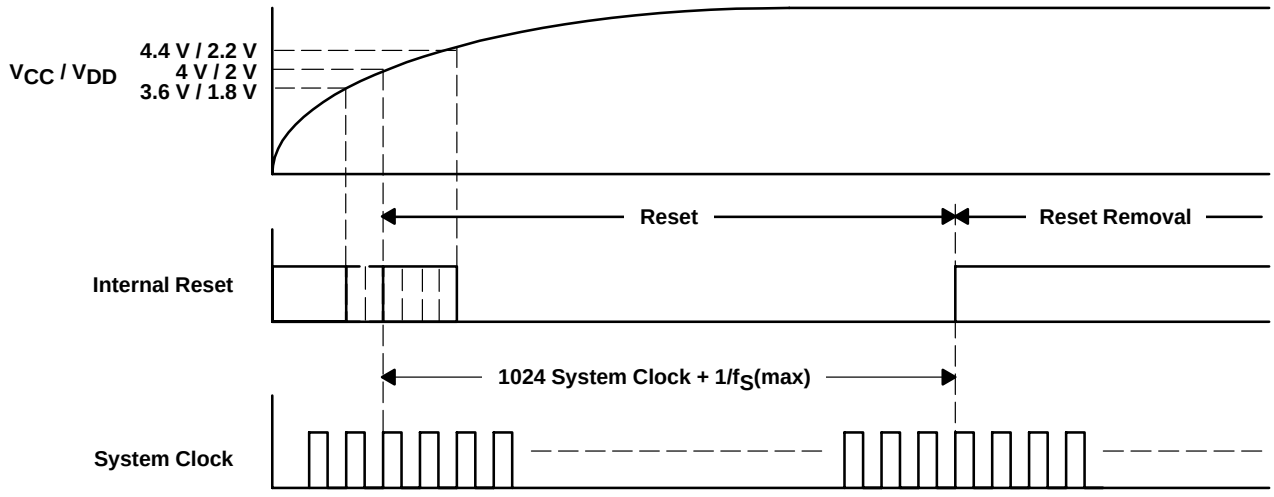


Figure 33. Internal Power-On Reset Timing

PRINCIPLES OF OPERATION

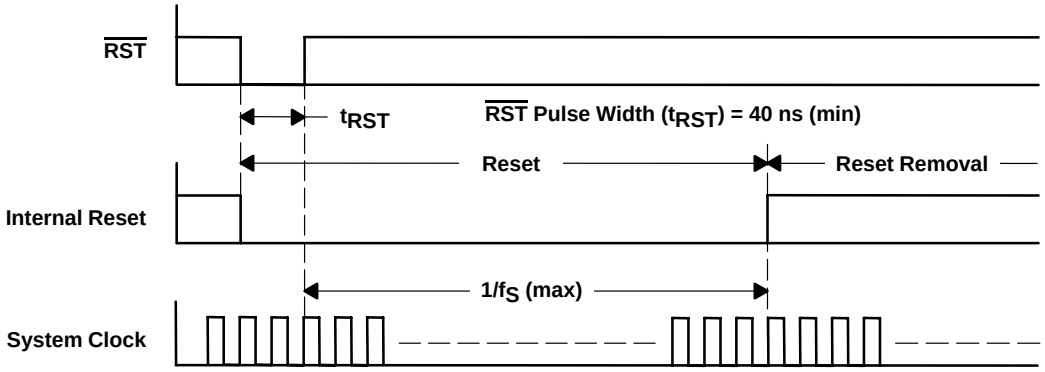
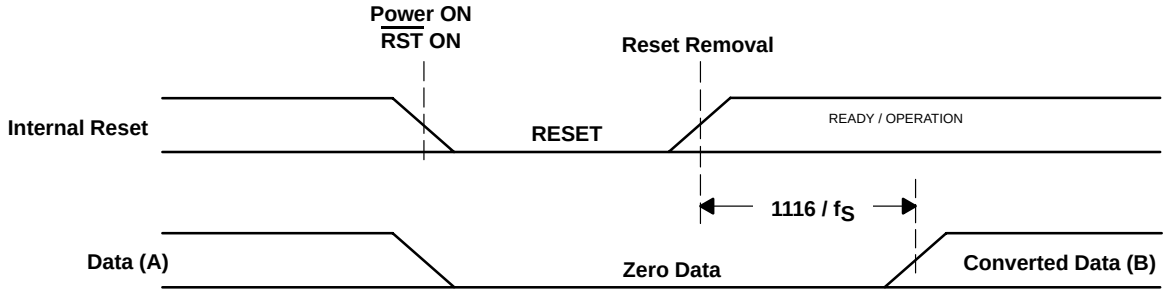


Figure 34. External Reset Timing



NOTES: A. In case of DSD mode, DSDL is also controlled like DSDR.
B. The HPF transient response appears initially.

Figure 35. ADC Digital Output for Power-On Reset and $\overline{RST}$ Control

audio data interface

The PCM1804 interfaces the audio system through BCK/DSDL (pin 16), LRCK/DSDBCK (pin 17), and DATA/DSDR (pin 15). The PCM1804 needs $\overline{RST}$ = low when in the interface mode and/or the data format are changed.

interface mode

The PCM1804 supports master mode and slave mode as interface modes, which are selected by S/$\overline{M}$ (pin 8) as shown in Table 4. In master mode, the PCM1804 provides the timing of the serial audio data communications between the PCM1804 and the digital audio processor or external circuit. While in slave mode, the PCM1804 receives the timing of data transfer from an external controller. Slave mode is not available for DSD.

Table 4. Interface Mode

S/$\overline{M}$	MODE
Low	Master mode
High	Slave mode

PRINCIPLES OF OPERATION

data format

The PCM1804 supports four audio data formats in both of master and slave mode, and these data formats are selected by the FMT0 (pin 6) and FMT1 (pin 7) as shown in Table 5.

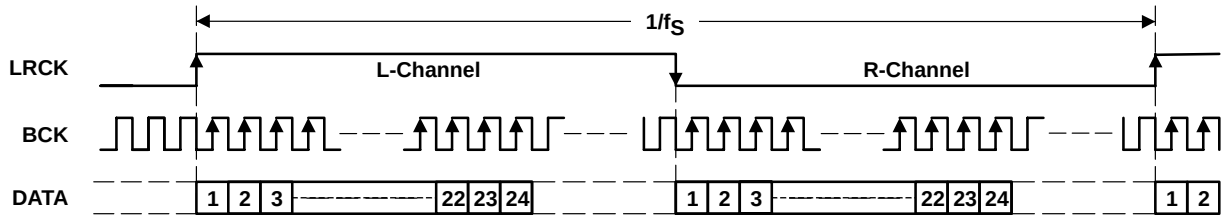
Table 5. Data Format

FMT1	FMT0	FORMAT	MASTER	SLAVE
Low	Low	PCM, Left justified, 24 bit.	Yes	Yes
Low	High	PCM, I^2S, 24 bit.	Yes	Yes
High	Low	PCM, Standard, 24 bit	Yes	Yes
High	High	DSD	Yes	—

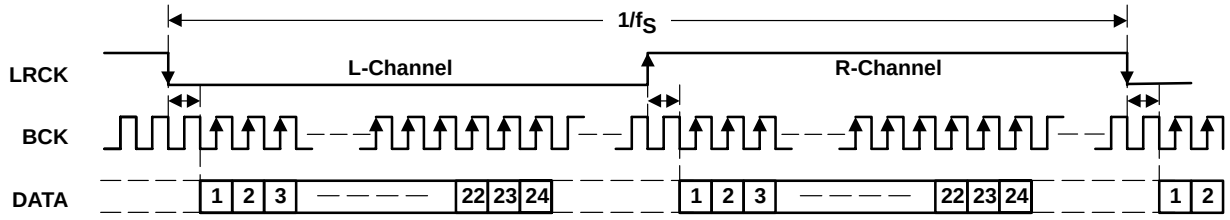
interface timing for PCM

Figure 36 through Figure 38 illustrate the interface timing for PCM.

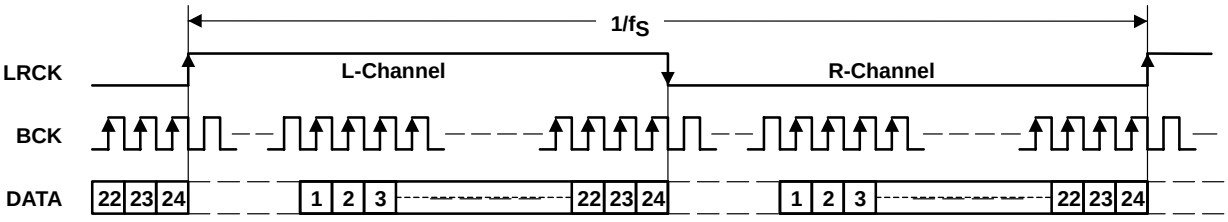
(1) Left-Justified Data Format; L-Channel = High, R-Channel = Low



(2) I^2S Data Format; L-Channel = Low, R-Channel = High



(3) Standard Data Format; L-Channel = High, R-Channel = Low

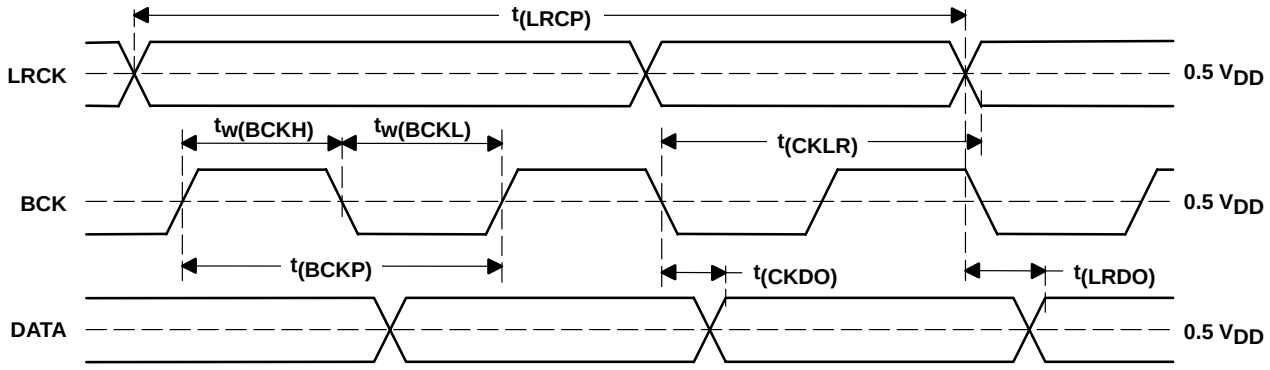


NOTE: LRCK and BCK work as outputs at master mode, inputs at slave mode, respectively.

Figure 36. Audio Data Format for PCM

PRINCIPLES OF OPERATION

interface timing for PCM (continued)



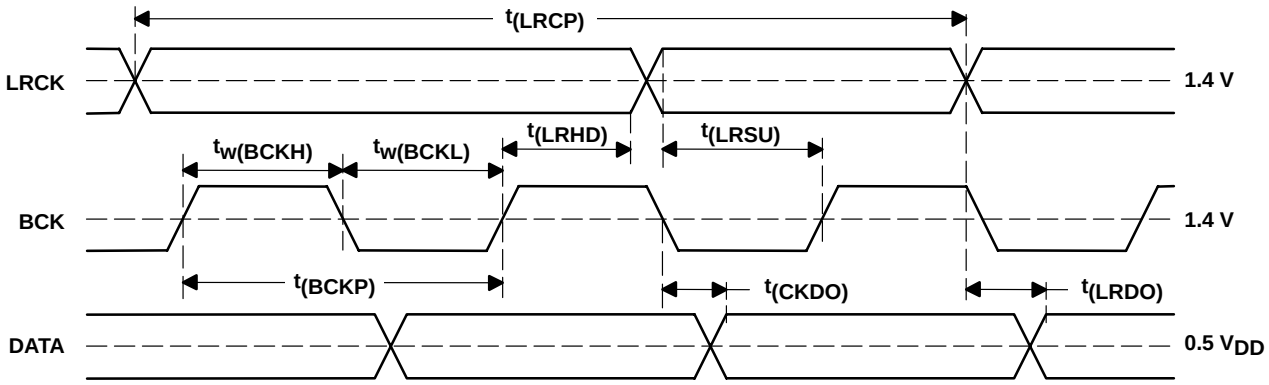
PARAMETERS	MIN	TYP	MAX	UNIT
BCK period, $t_{(BCKP)}$		$1/(64\ f_S)$		
BCK pulse width high, $t_{w(BCKH)}$	32			ns
BCK pulse width low, $t_{w(BCKL)}$	32			ns
Delay time BCK falling edge to LRCK valid, $t_{(CKLR)}$	–5		15	ns
LRCK period, $t_{(LRCP)}$		$1/f_S$		
Delay time BCK falling edge to DATA valid, $t_{(CKDO)}$	–5		15	ns
Delay time LRCK edge to DATA valid, $t_{(LRDO)}$	–5		15	ns
Rising time of all signals, t_r			10	ns
Falling time of all signals, t_f			10	ns

NOTES: A. Rising and falling time is measured from 10% to 90% of IN/OUT signals swing.
B. Load capacitance of all signals are 10 pF.
C. $t_{(BCKP)}$ is fixed at $1/(64\ f_S)$ in case of master mode.

Figure 37. Audio Data Interface Timing for PCM (Master Mode: LRCK and BCK Work as Outputs)

PRINCIPLES OF OPERATION

interface timing for PCM (continued)



PARAMETERS	MIN	TYP	MAX	UNIT
BCK period, $t_{(BCKP)}$	1/(64 f_S)	1/(64 f_S)	1/(48 f_S)	
BCK pulse width high, $t_{W(BCKH)}$	32			ns
BCK pulse width low, $t_{W(BCKL)}$	32			ns
LRCK setup time to BCK rising edge, $t_{(LRSU)}$	12			ns
LRCK hold time to BCK rising edge, $t_{(LRHD)}$	12			ns
LRCK period, $t_{(LRCP)}$		1/f_S		
Delay time BCK falling edge to DATA valid, $t_{(CKDO)}$	5		25	ns
Delay time LRCK edge to DATA valid, $t_{(LRDO)}$	5		25	ns
Rising time of all signals, t_r			10	ns
Falling time of all signals, t_f			10	ns

NOTES: A. Rising and falling time is measured from 10% to 90% of IN/OUT signals swing.
B. Load capacitance of DATA/DSDR signal is 10 pF.

Figure 38. Audio Data Interface Timing for PCM (Slave Mode: LRCK and BCK Work as Inputs)

interface timing for DSD

Figure 39 and Figure 40 illustrate the interface timing for DSD.

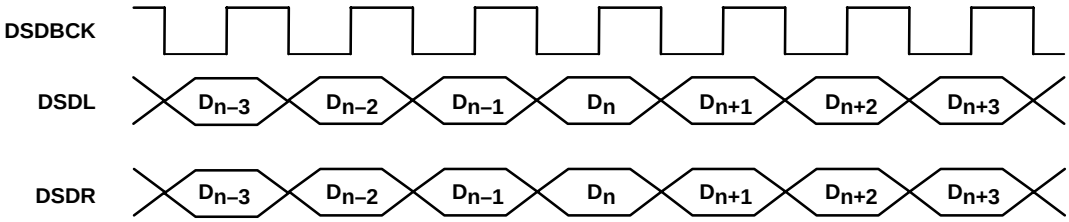
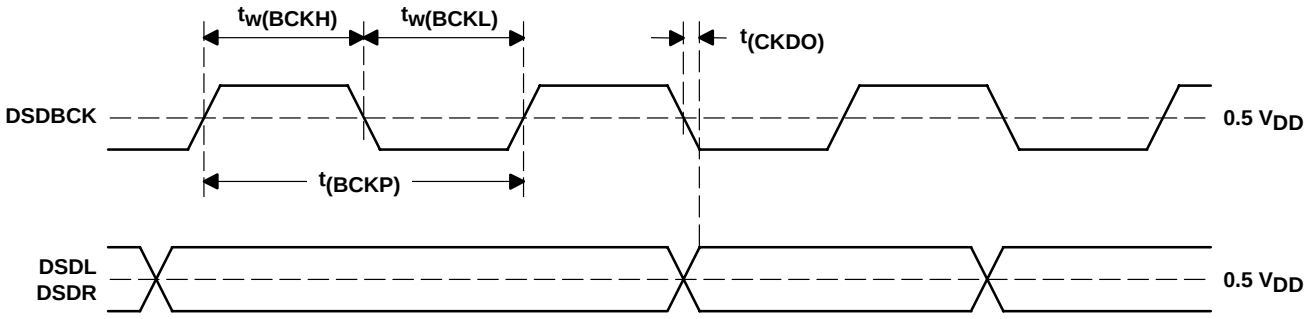


Figure 39. Audio Data Format

PRINCIPLES OF OPERATION

interface timing for DSD (continued)



PARAMETERS	MIN	TYP	MAX	UNIT
DSDBCK period, $t_{(BCKP)}$		354.308		ns
DSDBCK pulse width high, $t_{W(BCKH)}$		177.154		ns
DSDBCK pulse width low, $t_{W(BCKL)}$		177.154		ns
Delay time DSDBCK falling edge to DSDL, DSDR valid, $t_{(CKDO)}$	–5		15	ns
Rising time of all signals, t_r			10	ns
Falling time of all signals, t_f			10	ns

NOTES: A. Rising and falling time is measured from 10% to 90% of IN/OUT signals swing.
B. Load capacitance of DSDBCK/DSDL/DSDR signal is 10 pF.

Figure 40. Audio Data Interface Timing for DSD (Mast Mode Only)

synchronization with digital audio system for PCM

In slave mode, the PCM1804 operates under LRCK synchronized with the system clock SCKI. The PCM1804 does not need specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCK during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced into BPZ code until resynchronization between LRCK and SCKI is completed.

In case of changes less than ±5 BCK, resynchronization does not occur and above digital output control and discontinuity does not occur.

Figure 41 illustrates ADC digital output for loss of synchronization and resynchronization. During undefined data, it may generate some noise in the audio signal. Also, the transitions of normal to undefined data and undefined or zero data to normal make a discontinuity of data on the digital output. This may generate noise in the audio signal. In master mode, synchronization loss never occurs.

HPF (low-cut filter) bypass control for PCM

The built-in function for dc component rejection can be bypassed by BYPAS (pin 12) control. In bypass mode, the dc component of the input analog signal and the internal dc offset are also converted and output in the digital output data.

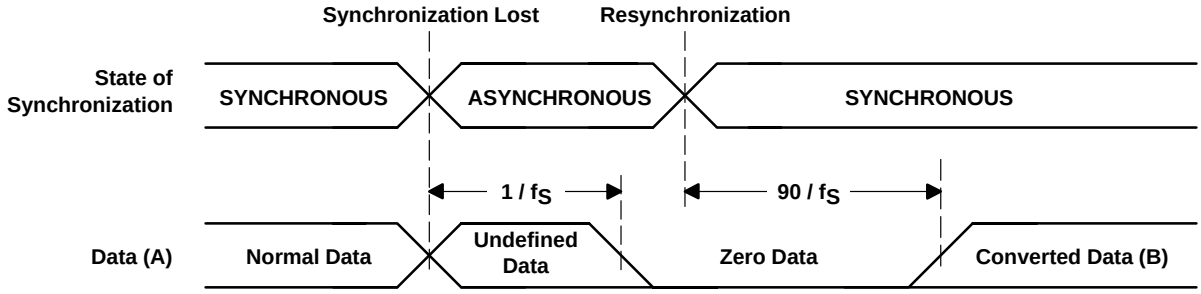
Table 6. HPF Bypass Control

BYPASS	LPF (HIGH-PASS FILTER) MODE
Low	Normal (dc cut) mode
High	Bypass (through) mode

PRINCIPLES OF OPERATION

overflow flag for PCM

The PCM1804 has two overflow flag pins, OVFR (pin 20) and OVFL (pin 21). The pins go to high as soon as the analog input goes across the full-scale range. The high level is held for 1.016 s at maximum, and returns to low if the analog input does not go across the full-scale range for the period.



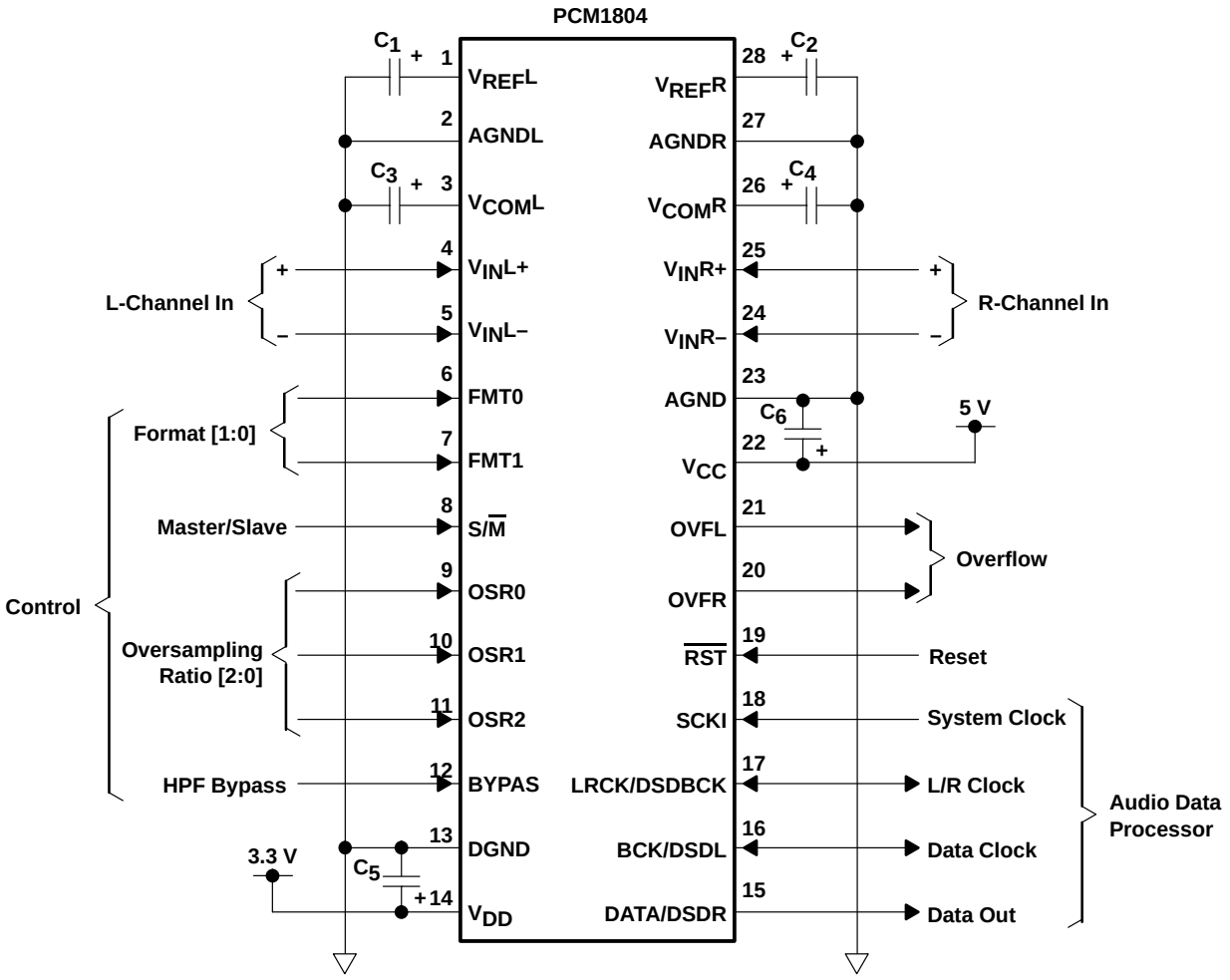
NOTES: A. Applies only for slave mode, the loss of synchronization never occurs in master mode.
B. The HPF transient response appears initially.

Figure 41. ADC Digital Output for Lost of Synchronization and Resynchronization

PRINCIPLES OF OPERATION

typical circuit connection diagram

Figure 42 illustrates a typical circuit connection diagram in the PCM data format operation.



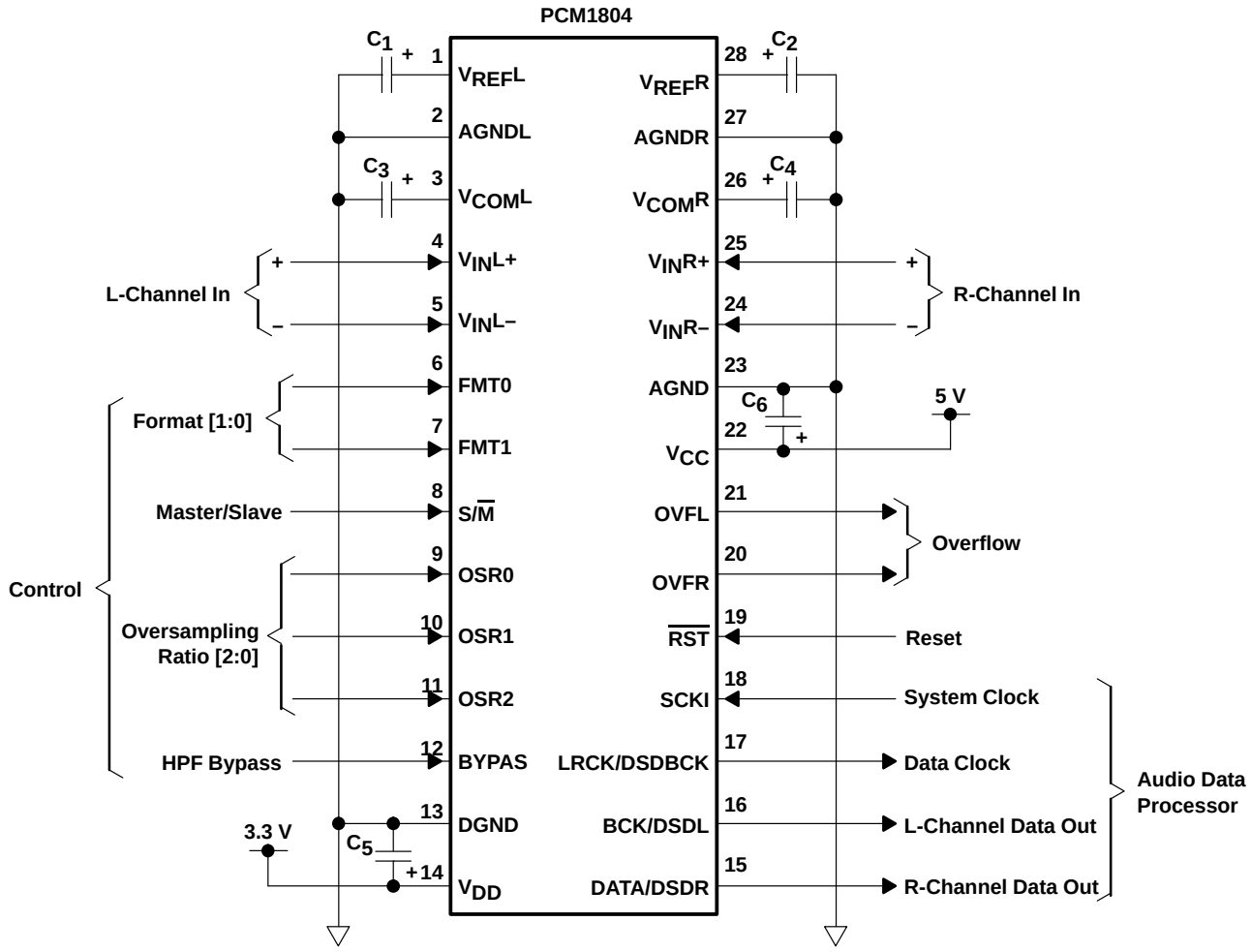
NOTES: A. C1, C2, C5, and C6: Bypass capacitor 0.1-μF ceramic and 10-μF tantalum, depends on layout and power supply.
B. C3, C4: Bypass capacitor 0.1-μF tantalum, depends on layout and power supply.

Figure 42. Typical Circuit Connection Diagram at PCM

PRINCIPLES OF OPERATION

typical circuit connection diagram (continued)

Figure 43 illustrates a typical circuit connection diagram in the DSD data format operation.



NOTES: A. C1, C2, C5, and C6: Bypass capacitor 0.1-µF ceramic and 10-µF tantalum, depends on layout and power supply.
B. C3, C4: Bypass capacitor 0.1-µF tantalum, depends on layout and power supply.

Figure 43. Typical Circuit Connection Diagram at DSD

APPLICATION INFORMATION

board design and layout considerations

V_{CC}, V_{DD} pins

The digital and analog power supply lines to the PCM1804 should be bypassed to the corresponding ground pins with 0.1-μF ceramic and 10-μF tantalum capacitors placed as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1804 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply trouble like latch-up or power-supply sequence.

V_{IN} pins

Use 100-pF ceramic capacitors between $V_{IN}L+$, $V_{IN}L-$, $V_{IN}R+$, $V_{IN}R-$, and AGND, and 0.022-μF ceramic capacitors between $V_{IN}L+$ and $V_{IN}L-$, $V_{IN}R+$, and $V_{IN}R-$ to remove higher-frequency noise at the delta-sigma input section.

V_{REFX}, V_{COMX} inputs

Use 0.1-μF ceramic and 10-μF tantalum capacitors between $V_{REF}L$, $V_{REF}R$, and corresponding AGNDx, to insure low-source impedance at ADC references. Use 0.1-μF tantalum capacitors between $V_{COM}L$, $V_{COM}R$ and corresponding AGNDx to insure low-source impedance of common voltage. These capacitors should be located as close as possible to the $V_{REF}L$, $V_{REF}R$, $V_{COM}L$, and $V_{COM}R$ pins to reduce dynamic errors on references and common voltage. The dc voltage level of these pins is 2.5 V.

DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK pins

The DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK pins in master mode have large load drive capability. Locating the buffer near the PCM1804 and minimizing the load capacitance, minimizes the digital analog crosstalk and maximizes the dynamic performance of the ADC.

system clock

The quality of the system clock may influence dynamic performance, as the PCM1804 operates based on system clock. In that case, it may be required to consider the system clock duty, jitter, and the time difference between system clock transition and BCK/DSDL or LRCK/DSDBCK transition in slave mode.

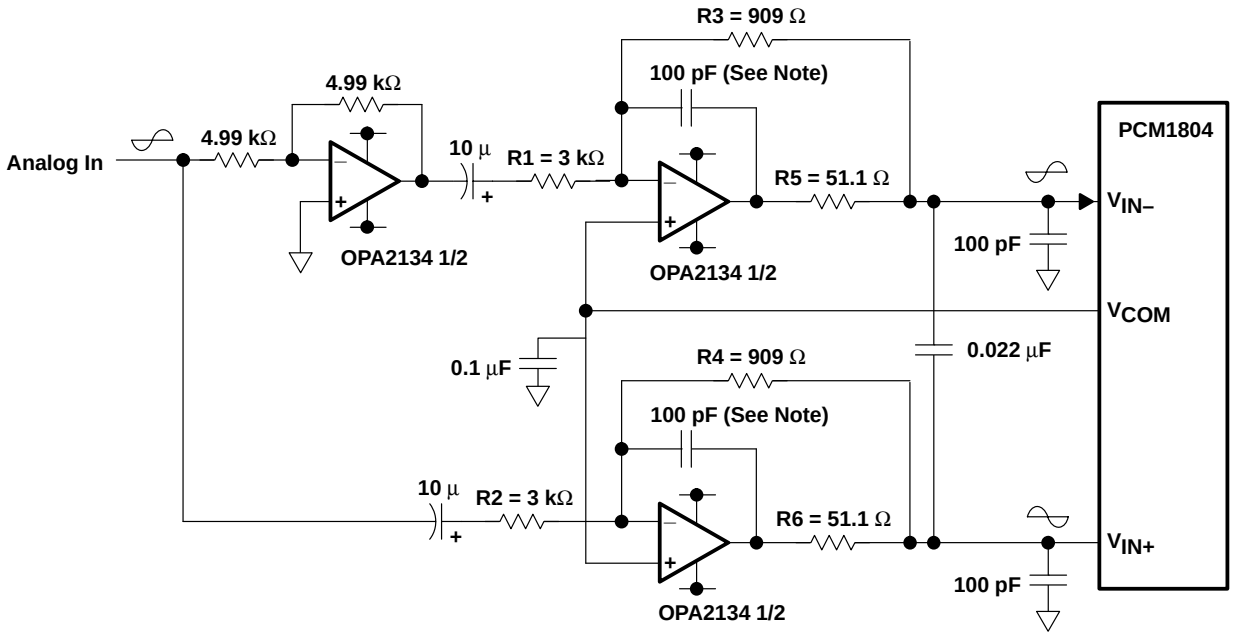
reset control

If capacitors larger than 10 μF are used on $V_{REF}L$ and $V_{REF}R$, the external reset control with a delay time corresponding to the $V_{REF}L$ and $V_{REF}R$ response is required. Also, it works as a power-down control.

application circuit for single-end input

An application circuit for a single-end input circuit is shown in Figure 44. The maximum signal input voltage and differential gain of this circuit is designed as Vinmax = 8.28 Vpp, A = 0.3. Differential gain (Ad) is given by R3/R1(R4/R2) as normal inverted gain amp. Resistor R5 (R6) in the feedback loop gives low-impedance drive operation and noise filtering for analog input of the PCM1804. The circuit technique R5 (R6) is recommended.

APPLICATION INFORMATION



NOTE: 3300 pF is recommended if the input signal level is more than –6 dB of FS at 100 kHz is applied in DSD mode.

Figure 44. Application Circuit for Single-Ended Input Circuit (PCM)

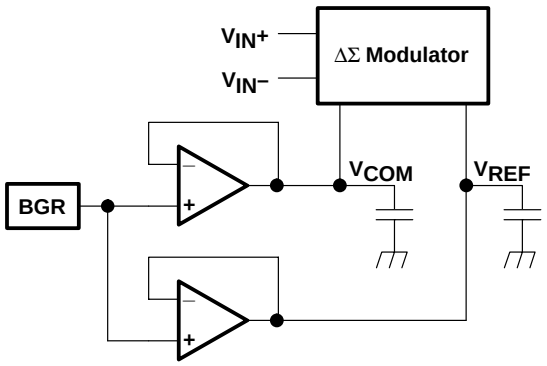
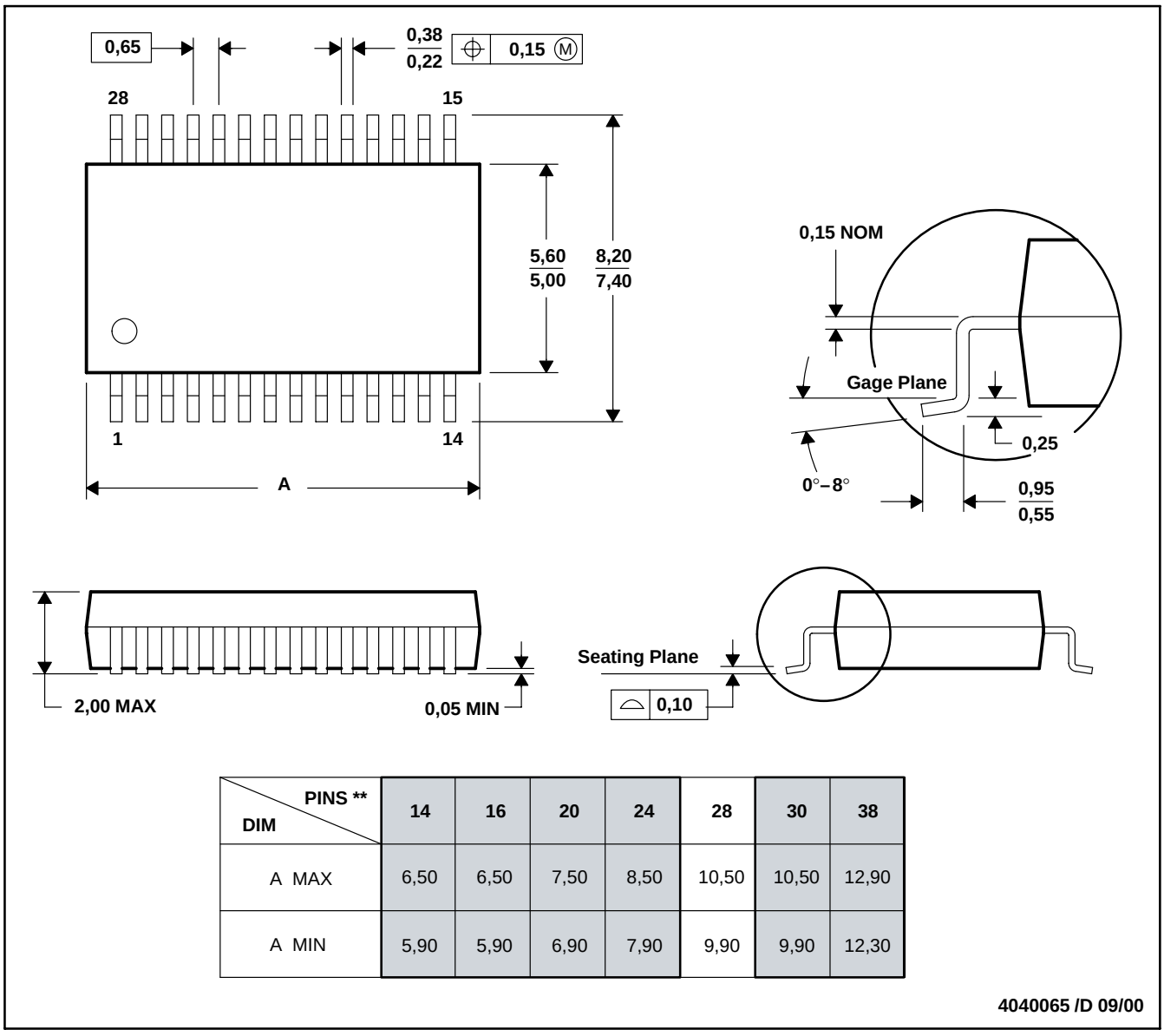


Figure 45. Equivalent Circuit of Internal Reference (V_{COM}, V_{REF})

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /D 09/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15 mm.
D. Falls within JEDEC MO-150

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