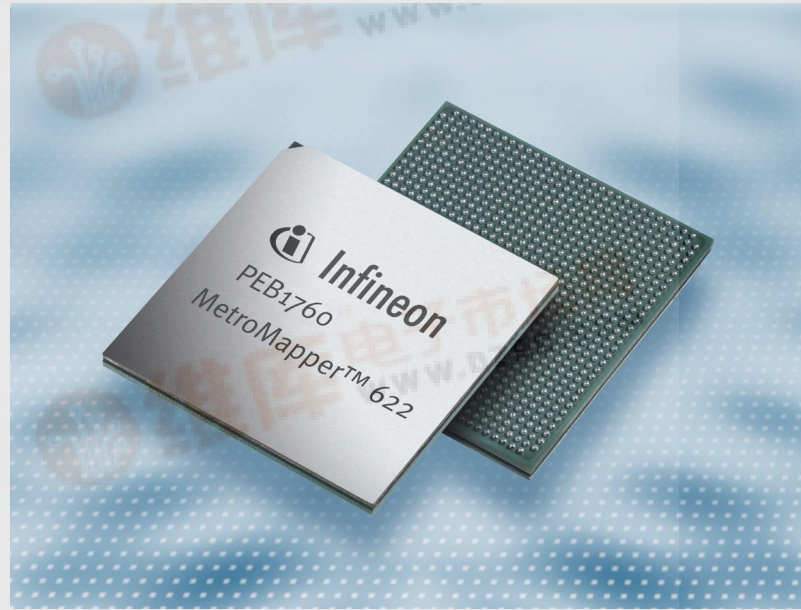


## Mapper/Framer for STM-4/STS-12 and STM-1/STS-3

The MetroMapper™ 622 is a mapper/framer capable of mapping datacom traffic into SONET/SDH transport payloads. On the line side, the MetroMapper™ 622 supports protected STS-12/STM-4 and STS-3/STM-1 interfaces. On the client side, up to sixteen Ethernet interfaces (10/100 Mbps), two 1 GE and one OIF SPI-3 interface with up to 64 logical channels are provided. The Ethernet traffic or the packets coming from the SPI-3 interface are encapsulated by either the GFP-F, LAPS (X.85/.86) or PPP mapping scheme. Low-order and high-order virtual concatenation (VCAT) with Link Capacity Adjustment Schemes (LCAS) for up to 64 virtual concatenated channels is supported. MetroMapper™ 622 provides Ethernet IEEE802.1q VLAN operations and enables Ethernet over MPLS.



### Applications

- Access / edge aggregation
- MSP
- ADM
- Mapper mode: packets are mapped between Ethernet and SDH/SONET interfaces
- Packet mode: packets from the SPI-3 interface are forwarded to SDH/SONET and Ethernet interfaces, and vice versa

### Features

#### Framer

- Multi-Rate SONET/SDH framer with STS/AU and VT/TU pointer processing capabilities
- Processes a single STS-12/STM-4 or a quad STS-3/STM-1
- Supports 1+1 line protection
- Payload Pointer interpretation and generation
- Fully SONET/SDH compliant

- Provides full performance monitoring for high- and low-order paths
- Provides high-order and low-order virtual concatenation according to ITU-T G.707
- Supports up to 64 virtual concatenated groups (VCG)
- Flexible concatenation of up to 12 high-order paths and up to 64 low-order paths into any virtual concatenation group
- Supports up to 336 VT1.5 or 252 TU12 low-order paths
- Provides following mapping schemes:
  - AU-4 / VC-4 / TUG-3
  - AU-3 / VC-3 or STS-1 / STS-SPE
- External buffer for up to 48 ms differential delay compensation
- Different VCG group types are defined:
  - $N \times VC-12$ ,  $N \times VC-11$ ,  $N \times VT1.5$  SPE,  $N \times VT2$  SPE ( $N \leq 64$ )

- $N \times VC-3$ ,  $N \times STS1$  SPE ( $N \leq 12$ )
- $N \times VC-4$ ,  $N \times STS3c$  SPE ( $N \leq 4$ )
- Provides flexible mapping of any VCG into any VC-4/STS-3
- Fully integrated support for the Link Capacity Adjustment Scheme (LCAS) protocol according to ITU-T G. 7042
- Provides hitless increase and decrease of multiple members VCG

#### SPI-3 Interface

- 64 logical channels each of them running in 32-bit mode
- Packet mode with variable block length

# MetroMapper™ 622

## PEB1760



## Features (cont'd)

### Encapsulation/Decapsulation

- Provides GFP-F mapping according to T1X1.5 / ITU-T G. 7041
- PPP processing according to IETF RFC 1662
- LAPS processing according to ITU-T X.85+X.86
- 64 logical channels, each of them can be independently configured to operate in one of the three encapsulation protocols
- PPP protocol support: MPLS Unicast & IP Version 4/6
- LAPS protocol support: Ethernet and IP Version 4/6
- FCS generation/checking
- Optional payload scrambling
- Idle frame insertion/deletion
- GFP Client management frame insertion/detection
- Comprehensive statistic counters for packets
- Packet import/export from/to CPU interface

### Layer 2

- Supported on both SDH and Ethernet ports
- IEEE802.1q VLAN tag operations per port/VLAN pair
- Up to 4096 port/VLAN pairs in total

- VLAN update include tag, retag and replace of VLAN IDs
- 0 or 1 VLAN can be inserted/removed
- Supports VLAN double tagging
- IETF Ethernet Martini MPLS label encapsulation per port/VLAN pair
- Supports IP/MPLS and Ethernet packets
- Per port tunneling mode
- Per port Ethernet MAC termination mode with packet classification as Ethernet, IP, MPLS or Layer-2 control packets

### Ethernet

- Two Gigabit Ethernet MACs with TBI Interfaces
- Sixteen Ethernet/Fast Ethernet with integrated SS-SMII Interfaces
- Per port MIB statistic counter per direction
- MAC pause frame control per port via:
  - Flexible leaky bucket implementation
  - Current RxFIFO threshold level
  - Under software control
- Flow control makes use of external memory for both directions
- Fixed Rx Buffer size: 32 kB for FE and 256 kB for GE ports
- Received flow control frames are passed through or discarded
- Jumbo packets supported

- All Ethernet ports may operate in MAC or PHY mode:
  - PHY mode allows glueless connections to another MAC/Ethernet switch
- Each Ethernet port maps to a single VCG

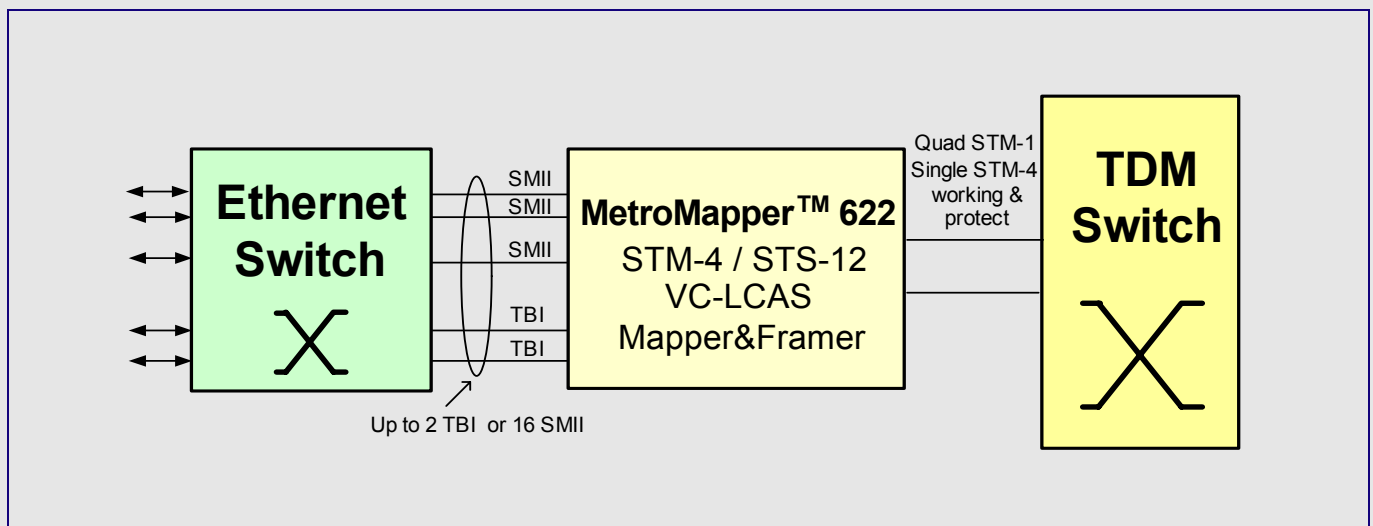
### Diagnostics

- Various loop back modes for system debugging implemented
  - Per SDH/SONET port Rx to Tx
  - Per Ethernet port in to out
  - SPI-3 input to SPI-3 output

### Interfaces

- Source synchronous STS-12/STM-4 or quad STS-3/STM-1 interfaces for working and protected links operating at 155 MHz I/Os
- OIF compliant SPI-3 interface
- Two TBI interfaces for GE
- 16 SS-SMII interfaces for FE
- Depending on application, up to 5 SRAM interfaces 32/36 bits data bus
- 66 MHz CPU interface
- IEEE 1149.1 JTAG boundary scan interface
- 1.5 V Core
- 2.5 V and 3.3 V I/Os
- 1020 pin FCBGA package

## Application Example



## Ethernet over SDH/SONET

How to reach us:  
<http://www.infineon.com>

Published by  
 Infineon Technologies AG,  
 St.-Martin-Strasse 53,  
 D-81669 München

© Infineon Technologies AG 2003. All Rights Reserved.

### Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office.

### Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.