

PHP20N06T; PHB20N06T

N-channel TrenchMOS™ transistor

Rev. 01 — 22 February 2001

Product specification

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:
PHP20N06T in SOT78 (TO-220AB)
PHB20N06T in SOT404 (D²-PAK).

2. Features

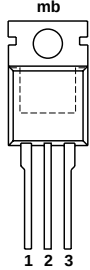
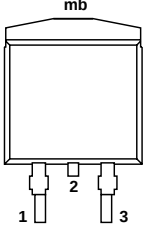
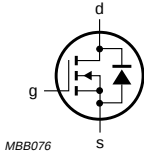
- Very low on-state resistance
- Fast switching.

3. Applications

- Switched mode power supplies
- DC to DC converters.

4. Pinning information

Table 1: Pinning - SOT78, SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 MBK106 SOT78 (TO-220AB)	 MBK116 SOT404 (D²-PAK)
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		
			 MBB076

[1] It is not possible to make connection to pin 2 of the SOT404 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.



5. Quick reference data

Table 2: Quick reference data

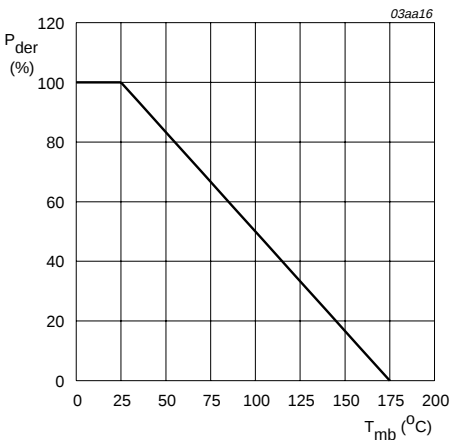
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	–	55	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	–	20.3	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	–	62	W
T_j	junction temperature		–	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A			
		$T_j = 25$ °C	64	75	mΩ
		$T_j = 175$ °C	–	150	mΩ

6. Limiting values

Table 3: Limiting values

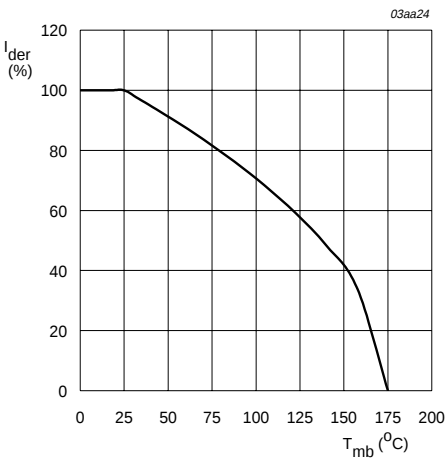
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		–	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20$ kΩ	–	55	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	20.3	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; Figure 2	–	14.3	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	81	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	62	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25$ °C	–	20.3	A
I_{DRM}	pulsed reverse drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	81	A
Avalanche ruggedness					
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 11$ A; $V_{DS} \leq 55$ V; $V_{GS} = 10$ V; $R_{GS} = 50$ Ω; starting $T_{mb} = 25$ °C	–	30.3	mJ



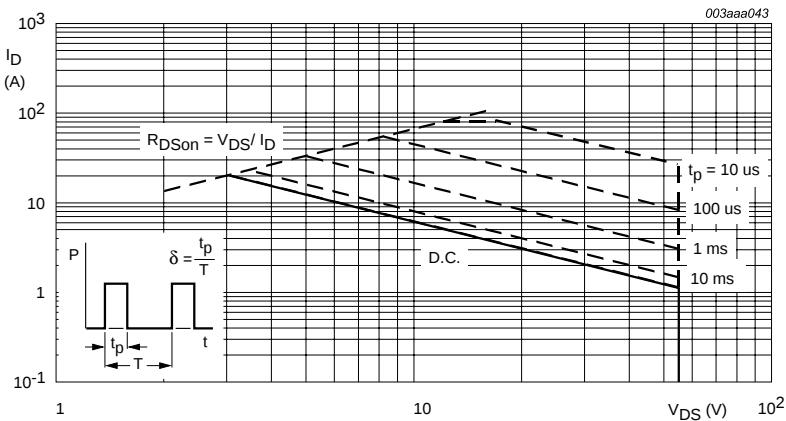
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 4.5 \text{ V}$$
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	60	K/W
		mounted on printed circuit board; minimum footprint; SOT404 package	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	2.4	K/W

7.1 Transient thermal impedance

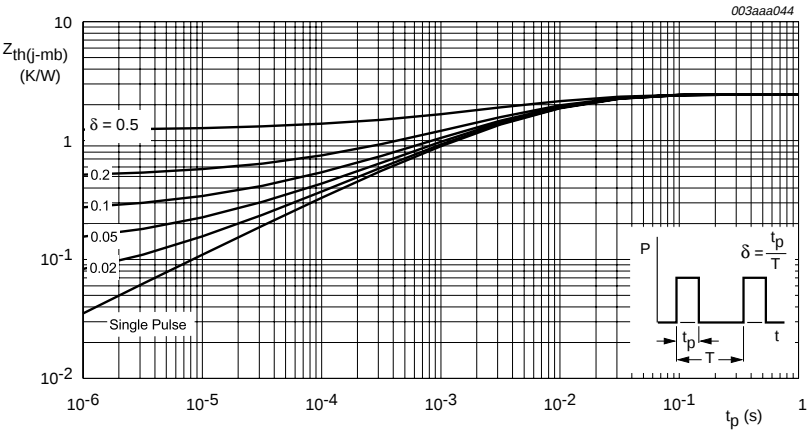


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

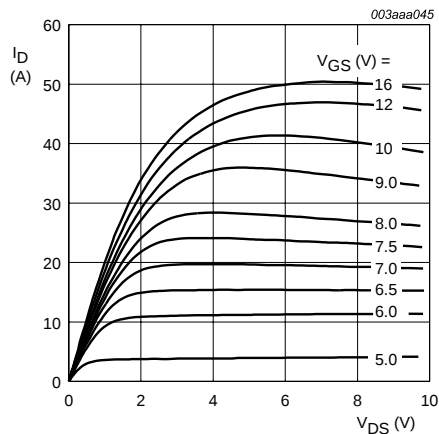
8. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	55	–	–	V
		$T_j = -55\text{ °C}$	50	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	–	–	V
		$T_j = -55\text{ °C}$	–	–	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	–	0.05	10	μA
		$T_j = 175\text{ °C}$	–	–	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	–	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	–	64	75	m Ω
		$T_j = 175\text{ °C}$	–	–	150	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DD} = 44\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 14	–	11	–	nC
Q_{gs}	gate-source charge		–	3	–	nC
Q_{gd}	gate-drain (Miller) charge		–	6	–	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 12	–	320	483	pF
C_{oss}	output capacitance		–	92	113	pF
C_{rss}	reverse transfer capacitance		–	64	90	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$;	–	10	–	ns
t_r	rise time		–	50	–	ns
$t_{d(off)}$	turn-off delay time		–	70	–	ns
t_f	fall time		–	40	–	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	–	4.5	–	nH
		from contact screw on mounting base to centre of die SOT78	–	3.5	–	nH
		from upper edge of drain mounting base to centre of die SOT404	–	2.5	–	nH
L_s	internal source inductance	from source lead to source bond pad	–	7.5	–	nH

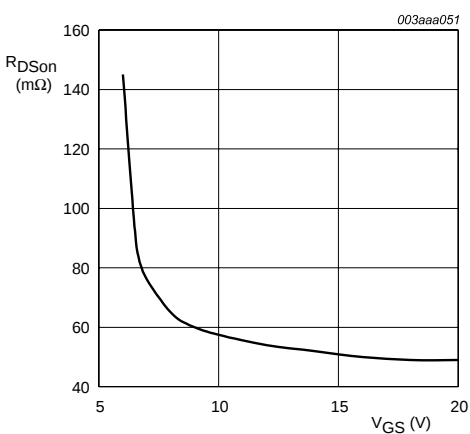
Table 5: Characteristics...continued
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 15	–	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = –100 A/μs	–	32	–	ns
Q _r	recovered charge	V _{GS} = –10 V; V _{DS} = 30 V	–	120	–	nC



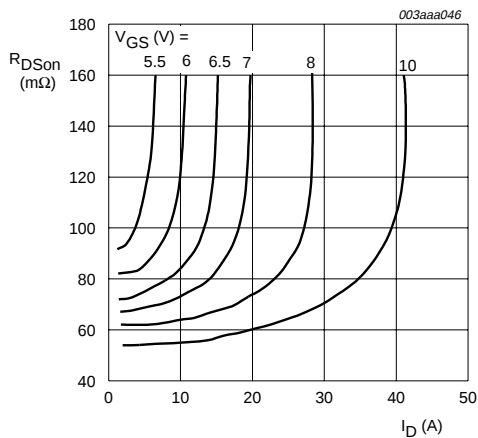
T_j = 25 °C; t_p = 300 μs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



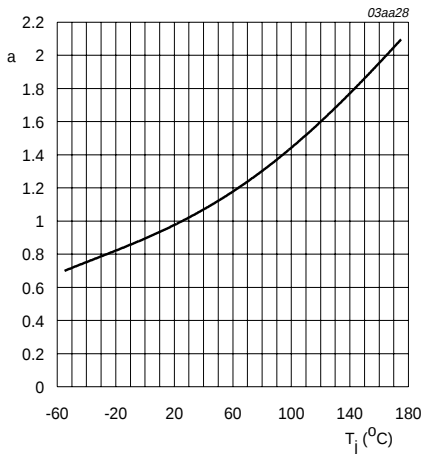
T_j = 25 °C; I_D = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



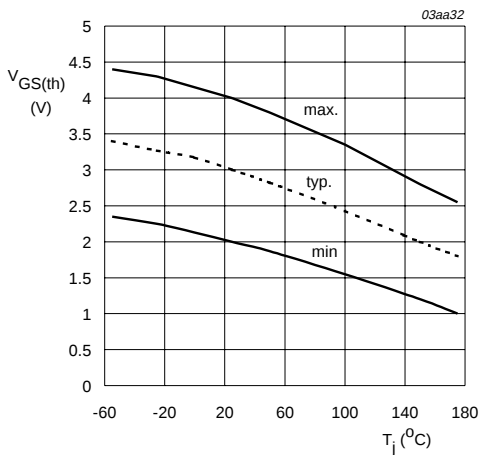
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



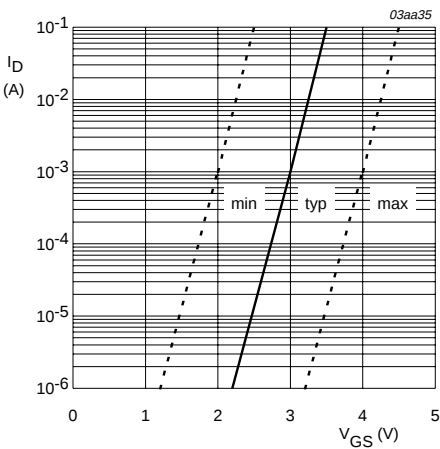
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



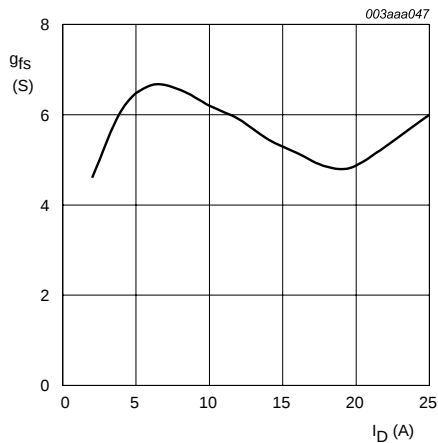
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



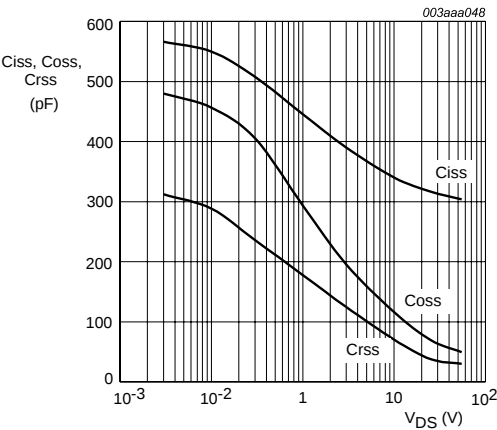
$T_j = 25 \text{ °C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



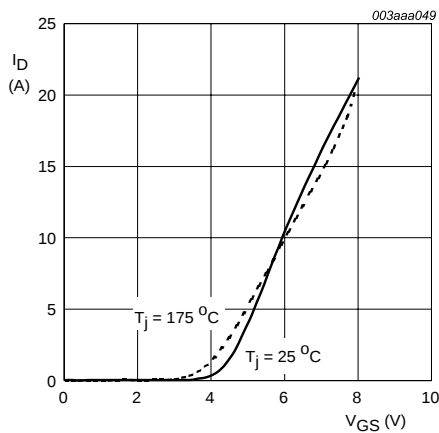
$T_j = 25 \text{ °C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



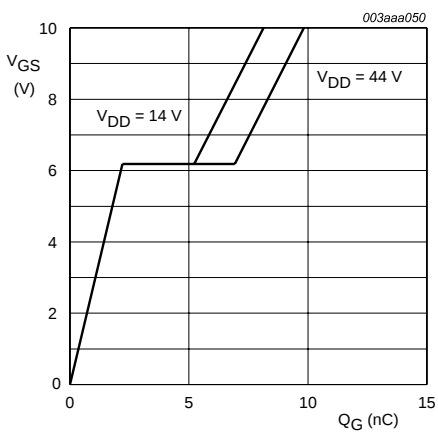
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



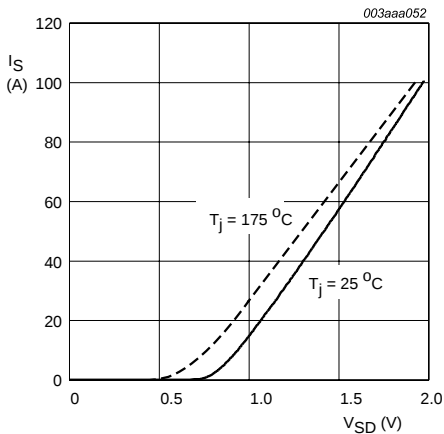
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_J = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



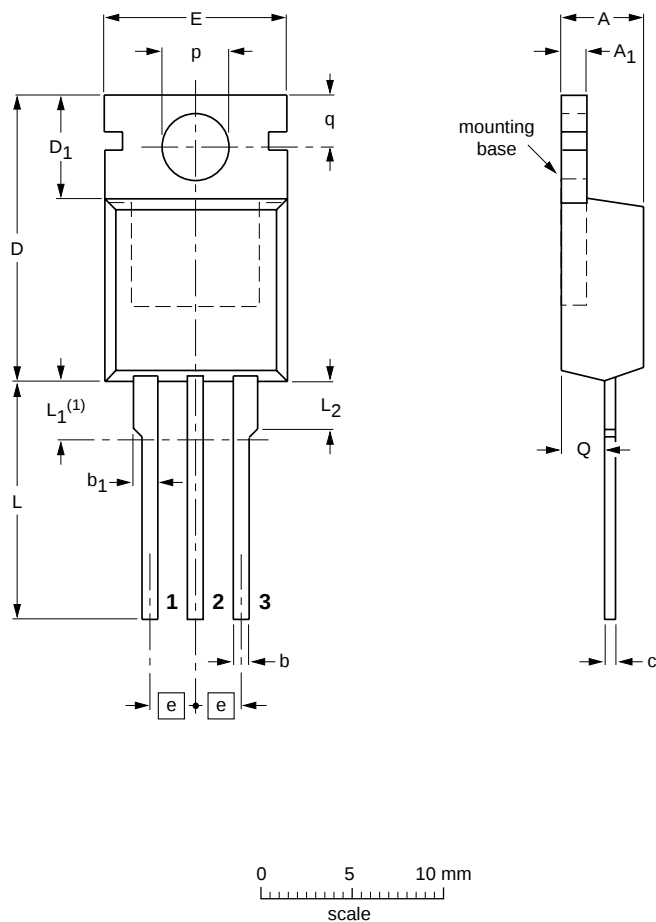
$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

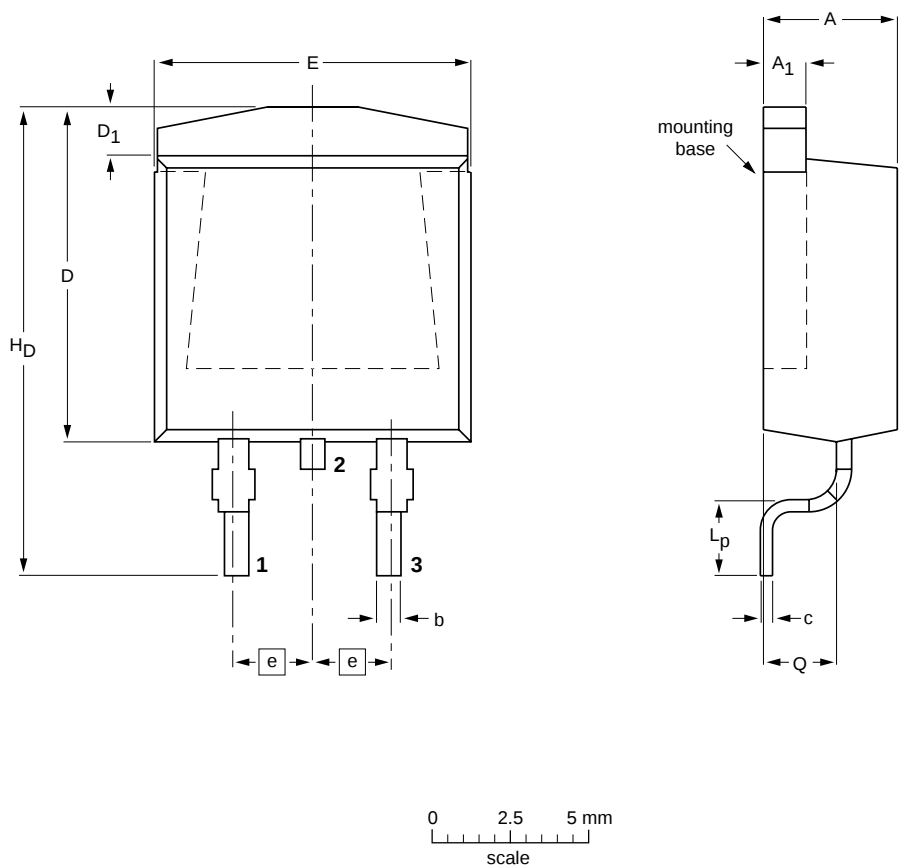
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07 01-02-16

Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						99-06-25 01-02-12

Fig 17. SOT404 (D²-PAK).

10. Soldering

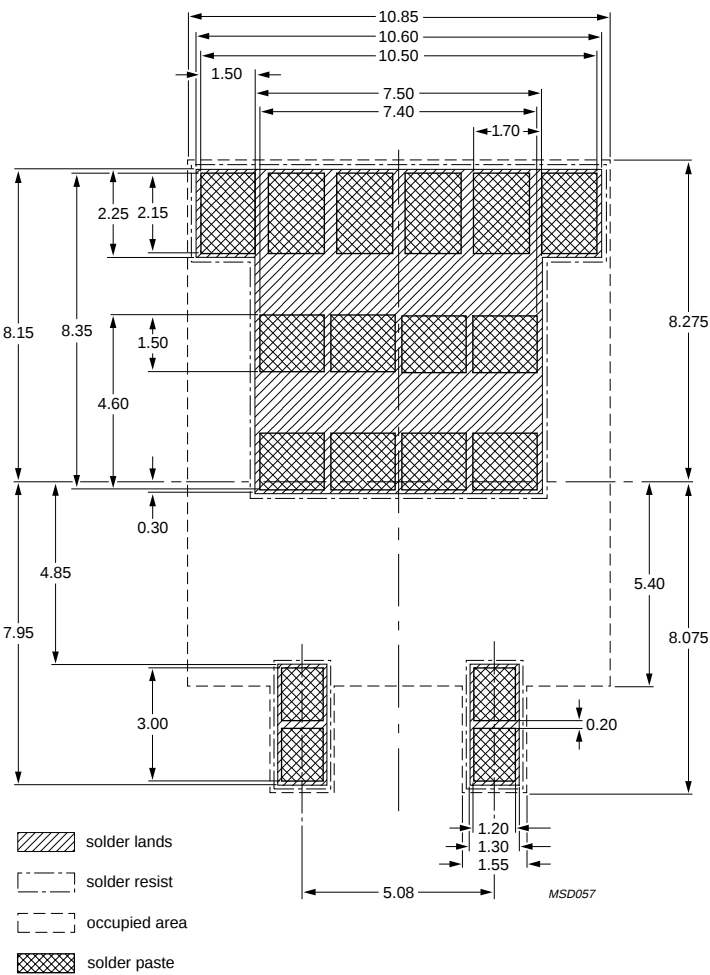


Fig 18. Reflow soldering footprint for SOT404.

11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010222	-	Product specification; initial version

12. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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(SCA71)

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