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PM5313

SPECTRA-622

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER FOR 622 MBIT/S

DATA SHEET

PROPRIETARY AND CONFIDENTIAL

PRODUCTION

ISSUE 6: SEPTEMBER 2000

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Issue No.	Issue Date	Details of Change
Issue 6	Sept 2000	• Remove support of in-band G1 reporting on DROP bus • Improve RAD Timing diagram (Fig 60) • Pointer justification not generated in PAIS on DROP bus • Specify that the jitter tolerance is according to the 1995 Bellcore spec. • Remove the K1 and K2 bytes from the RAD. • Specify that a RESET_PATH command will also clear the performing monitor counters of the section/line TSBs.Update AC and DC Characeristic sections according to its final report.. • V1 pulse is always outputted on the DROP bus when the RTAL FIFO is bypassed • Add the RESET sequence to enable the TX line interface and the OUTDATA bit in the CRSI. • Specify TFPO timing in serial mode • CRU and CSU will track REFCLK while in ROOL • Describe RX and TX bypass mode limitations • SDLE and RBYP mode can not be set at the same time. • Fix number of bits before a DOOL is declared from 80 to 96. • Bit 7 of register 0090H is now X vs 0. • Write to the PMON counter registers will also trigger a count transfer. • SS bits are always 00 when the DPGM is in autonomous mode. • Add WANS programming section • Update the RAD and TFPI timing diagrams. • Update rev of CRU, GPGM and TTOC. • Update the methodology Tools table.
Issue 5	May 2000	• Added STM1-CONCAT register bits in RPPS and TPPS configuration. • Extend the timing for output pins RSUC, RSOW, ROH and TDO.

		• Remove support for the tandem connection • Removed RESBYP and TESBYPASS register bits in RPPS and TPPS configuration. Bypass is no longer programmable per slice but for all RPPS or TPPS slices via the RESBYP and TESBYP bits found in DROP and ADD BUS configuration registers. • Fix RASE filtering spec to 8 frames • Correct DLL, APGM and DPGM register bits description • Describe use of ATSI bit in APGM autonomous mode. • Remove support of 12c when both autonomous mode and DTMODE are use. • Specify that FOOF affect only one frame • Add TS_{TAD} DC spec. • Add power supply filtering and PECL I/O diagrams • Revise RPOH timing diagrams • Add BYPASS Rx and TX mode description and limitation. No support for TUAIS, tx dual mode and pointer generation by STALs. • Specify that activity on the AC1J1V1, ADP and APL pins can not be detected if ADP is tied high or low.
Issue 4		• Revised RPPS alarm bit names, register 0n1C • Revised National bit description in the TTOC register 00C1 • Revised signal mapping in register 0009 SPECTRA 622 Section Alarm Control #2 • Added pin description of the Transmit Ring Control Port • Fixed polarity for bit 7, register 0102 • Added TPIP is held in reset in DS3 mode only • Revised TPAIS and DPAIS frame slots to correctly correspond to slice order • Clarified precedence of TOH Overhead port over TSOW, TSUC, and TLOW • Removed some DLL registers

		• ADD DLL does not exist • Clarified description of SSTB/SPTB write trigger register • Revised TTOH, TTOHEN set-up time • Clarified SENB bit description in register 0030 • Clarified bit DC1 description in register 00B4 • Clarified APGM/DPGM register information • Clarified register 1102 description • BIP calculation not supported by TPIP • Added REFCLK required when generating DS3ROCLK internally • Added pin description for FPIN and TPL • Revised RASE description and register definitions • Revised bit 6 Path Reset description, register 0000 • Clarified Protection Switch Byte Failures detection description • Added updates based on preps • Remove STS-6c/9c support • Fix register bits definitions • Fix Tx Ring Control Port definiton • Remove B3 verification from ADD bus • Revised Recommended BERM settings
Issue 3	July 1999	• Added FPPOS bit in register 0003 • Added Register 0016 • Added SCPII bit in register 000B • Uncovered EXT bit in register 1151 • Added pin number • Added boundary scan chain information
Issue 2	April 1999	• Removed DS-3 framers • Block diagram updated • TTOC and RTOC registers added • Swapped RASE and SSTB register blocks
Issue 1	Sep 1998	Document created

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1 FEATURES

1.1 General

- Monolithic SONET/SDH PAYLOAD EXTRACTOR/ALIGNER for use in STS-12 (STM-4/AU3 or STM-4/AU4) or STS-12c (STM-4-4c) interface applications, operating at serial interface speeds of up to 622.08 Mbit/s.
- Provides integrated clock and data recovery and clock synthesis for direct connection to optical modules.
- Supports a duplex byte-serial 77.76 Mbyte/s STS-12 (STM-4/AU3 or STM-4/AU4) or STS-12c (STM-4-4c) line side interface for use in applications where by-passing clock recovery, clock synthesis, and serializer-deserializer functionality is desired.
- Supports clock recovery bypass for use in applications where external clock recovery is desired.
- Complies with Bellcore GR-253-CORE jitter tolerance (1995 issue), jitter transfer and intrinsic jitter criteria.
- Provides control circuitry to comply with Bellcore GR-253-CORE WAN clocking requirements related to wander transfer, holdover and long term stability when using an external VCXO.
- Provides termination for SONET Section and Line, SDH Regenerator Section and Multiplexer Section transport overhead, and path overhead of twelve STS-1 (STM-0/AU3) paths, four STS-3/3c (STM-1/AU3/AU4) paths or a single STS-12c (STM-4-4c) path.
- De-multiplexes an STM-4 receive stream to four STM-1 Telecom DROP bus streams.
- Multiplexes four STM-1 Telecom ADD bus streams to an STM-4 transmit stream.
- Maps twelve STS-1 (STM-0/AU3) payloads, four STS-3/3c (STM-1/AU3/AU4) payloads or a single STS-12c (STM-4-4c) payload to system timing reference, accommodating plesiochronous timing offsets between the references through pointer processing.
- Maps twelve DS3 bit streams into an STS-12 (STM-4/AU3) frame.

- Provides Time Slot Interchange (TSI) function at the Telecom ADD and DROP buses for grooming twelve STS-1 (STM-0/AU3) paths or four STS-3/3c (STM-1/AU3/AU4) paths.

- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from a Telecom ADD bus interface to a Telecom DROP bus interface.

- Supports OC-48(STM-16) applications by providing parallel receive and transmit line side ports used to connect to front-end OC-48 devices.

- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.

- Low power 3.3V CMOS with TTL compatible digital inputs and CMOS/TTL digital outputs. PECL inputs and outputs are 3.3V and 5V compatible.

- Industrial temperature range (-40°C to +85°C).

- 520 pin Super BGA package.

1.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the STS-12 (STM-4) receive stream and inserts the framing bytes (A1, A2) and the STS identification byte (J0) into the transmit stream; descrambles the received stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the Z2 (M1) growth byte based on received B2 errors.

- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.

- Extracts and serializes the order wire channels (E1, E2), the data communication channels (D1-D3, D4-D12) and the section user channel (F1) from the received stream, and inserts the corresponding signals into the transmit stream.

- Extracts and serializes the automatic protection switch (APS) channel (K1, K2) bytes, filtering and extracting them into internal registers for the receive stream. Inserts the APS channel into the transmit stream.

- Extracts and filters the synchronization status message (Z1/S1) byte into an internal register for the receive stream. Inserts the synchronization status message (Z1/S1) byte into the transmit stream.

- Extracts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the receive stream. Detects an unstable section trace message or mismatch with an expected message, and optionally inserts Line and Path AIS on the system DROP side upon either of these conditions. Inserts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the transmit stream. Provides access to the accepted message via the microprocessor port.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms on the receive stream. Optionally returns line RDI in the transmit stream.

- Provides a transmit and receive ring control port, allowing alarm and maintenance signal control and status to be passed between mate SPECTRA-622s for ring-based add drop multiplexer and line multiplexer applications.

- Configurable to force Line AIS in the transmit stream.

1.3 SONET Path / SDH High Order Path

- Accepts a multiplex of twelve STS-1 (STM-0/AU3) streams, four STS-3/3c (STM-1/AU3/AU4) streams or a single STS-12c (STM-4-4c) stream, interprets the STS (AU) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.

- Constructs a byte serial multiplex of twelve STS-1 (STM-0/AU3) streams or four STS-3/3c (STM-1/AU3/AU4) stream on the transmit side.

- Detects loss of pointer (LOP), loss of tributary multiframe (LOM), path alarm indication signal (PAIS) and path (auxiliary and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.

- Extracts and serializes the entire path overhead from the twelve STS-1 (STM-0/AU3), four STS-3/3c (STM-1/AU3/AU4) or the single STS-12c (STM-4-4c) receive streams. Inserts the path overhead bytes in the twelve STS-1 (STM-0/AU3), four STS-3/3c (STM-1/AU3/AU4) or single STS-12c (STM-4-4c) stream for the transmit stream. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input stream. Path overhead insertion may also be disabled.

- Extracts the received path signal label (C2) byte into an internal register and detects for path signal label unstable and for signal label mismatch with the expected signal label that is downloaded by the microprocessor. Inserts the path signal label (C2) byte from an internal register for the transmit stream.

- Extracts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable path trace message or mismatch with an expected message, and inserts Path RAI upon either of these conditions. Inserts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the transmit stream. Provides access to the accepted message via the microprocessor port.

- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.

- Counts received path remote error indications (REIs) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) basis on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block bases independent of the accumulation of BIP-8 errors.

- Maintains the existing tributary multiframe sequence on the H4 byte until a new phase alignment has been verified.

- Provides a serial alarm port communication of path REI and path RDI alarms to the transmit stream of a mate SPECTRA-622 in the returning direction.

1.4 System Side Interfaces

- Supports Telecombus interfaces by indicating/accepting the location of the STS identification byte (C1), optionally the path trace byte(s) (J1), optionally the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes in the byte serial stream.

- Configurable to support four 19.44 MHz byte Telecombus interfaces or a single 77.76 MHz byte Telecombus interface.
- For Telecombus interface, accommodates phase and frequency differences between the receive/transmit streams and the DROP/ADD busses via pointer adjustments.
- Supports bit serial DS3 interfaces for mapping into and out of the 12 possible STS-1 SPE's in an STS-12 (STM-4/AU3).
- For the DS3 interface, provides optional insertion of DS3 AIS in both the ADD and DROP directions.
- Configurable to support a mix of traffic from the DS-3 interface and the Telecombus interface selectable on an STS-1 basis.
- Provides TSI function to interchange or groom twelve STS-1 (STM-0/AU3) paths or four STS-3/3c (STM-1/AU3/AU4) paths at the Telecom ADD and DROP buses. For STS-3 (STM-1/AU3) paths, grooming can be performed at the STS-1 (STM-0/AU3) level.

2 APPLICATIONS

- SONET/SDH Add Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers

3 REFERENCES

- American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1995.
- American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring, T1X1.3/93-005R1, April 1993.
- Bell Communications Research - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2 Revision 2, January, 1999.
- Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996.
- ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January, 1996.
- ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.
- ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.
- ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.
- ITU Recommendation G.781, - “Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH)”, January, 1994.
- ITU Recommendation G.783, “Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks”, 28 October, 1992.
- ITU Recommendation O.151, “Error Performance measuring Equipment Operating at the Primary Rate and Above”, October, 1992.
- ITU Recommendation I.432, “ISDN User Network Interfaces”, March 93.

4 DEFINITIONS

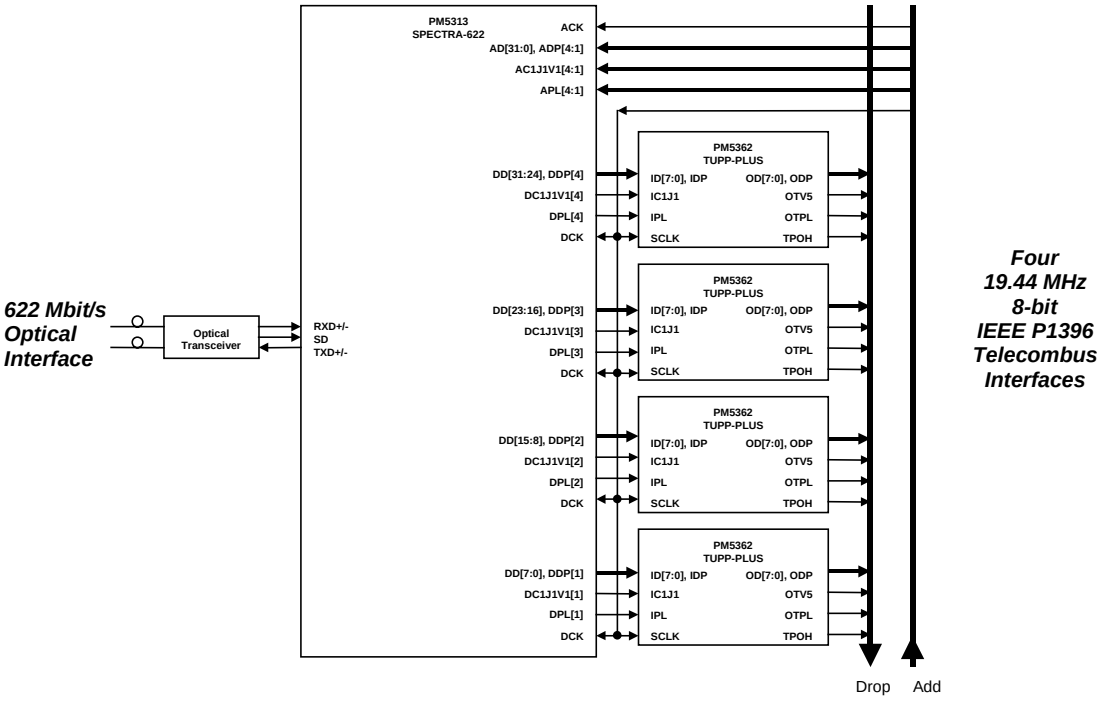
The following table defines the abbreviations for the SPECTRA-622.

APGM	ADD Bus PRBS Generator/Monitor
CRSI	CRU and SIPO
CRU	Clock Recovery Unit
CSPI	CSU and PISO
CSU	Clock Synthesis Unit
DPGM	DROP Bus PRBS Generator/Monitor
D3MA	DS3 Mapper ADD Side
D3MD	DS3 Mapper DROP Side
PISO	Parallel to Serial Converter
PRBS	Pseudo Random Bit/Byte Sequence
RASE	Receive APS, Synchronization Extractor and Bit Error Monitor
RLOP	Receive Line Overhead Processor
RTOC	Receive Transport Overhead Controller
RPOP	Receive Path Overhead Processor
RSOP	Receive Section Overhead Processor
RTAL	Receive Telecom Aligner
TSI	Timeslot Interchange
SIPO	Serial to Parallel Converter
SPTB	SONET/SDH Path Trace Buffer
SSTB	SONET/SDH Section Trace Buffer
TLOP	Transmit Line Overhead Processor
TTOC	Transmit Transport Overhead Controller
TPOP	Transmit Path Overhead Processor
TSOP	Transmit Section Overhead Processor
TTAL	Transmit Telecom Aligner
WANS	Wide Area Network Synchronization Controller
RPPS	Receive Path Processing Slice
TPPS	Transmit Path Processing Slice

5 APPLICATION EXAMPLES

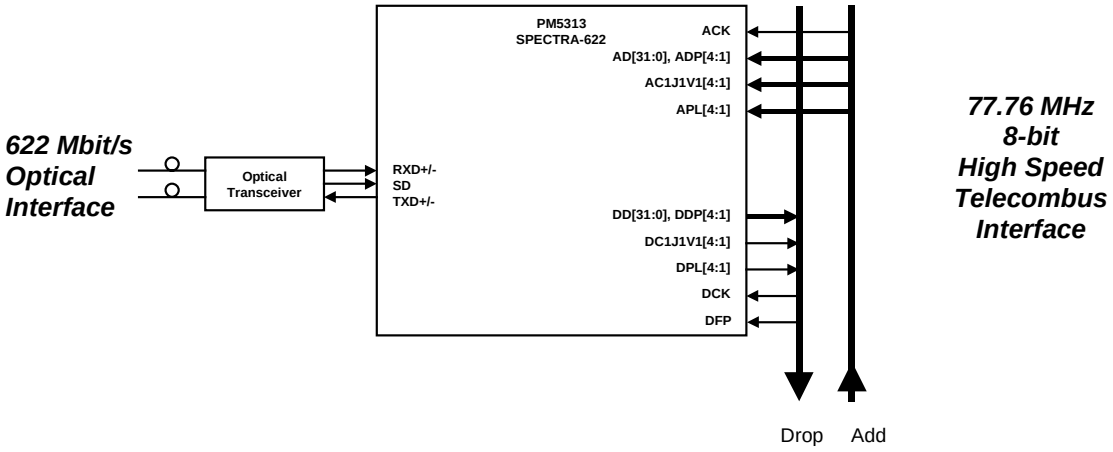
The SPECTRA-622 can be used in SONET/SDH network elements including switches, terminal multiplexers, and add-drop multiplexers. In such applications, the SPECTRA-622 line interface typically interfaces directly to electrical optical modules. On the system side interface, the SPECTRA-622 connects directly to a Telecombus. Figure 1 shows how the SPECTRA-622 is used to implement a 622 Mbit/s aggregate interface. In this application, the SPECTRA-622 performs SONET/SDH section, line and path termination and the PM5362 TUPP-PLUS performs tributary pointer processing and performance monitoring.

Figure 1 -STS-12 (STM-4/AU-3), STS-12 (STM-4/AU-4) or STS-12c (STM-4-4c) Application with 19.44 MHz Byte Telecombus Interface



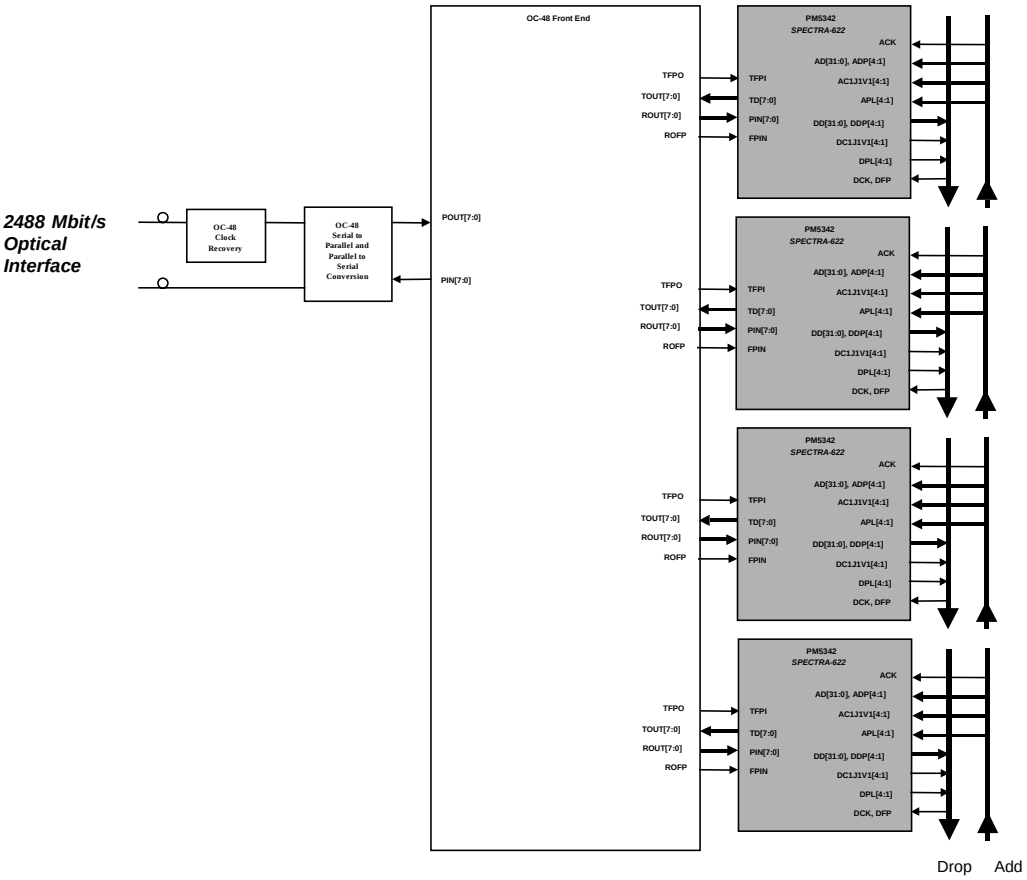
The system side interface of the SPECTRA-622 can also be configured to have a 77.76 MHz byte Telecombus interface. Figure 2 shows how the SPECTRA-622 is used to implement a 622 Mbit/s aggregate interface using the high-speed Telecombus on the system side interface. In this application, the SPECTRA-622 performs SONET/SDH section, line and path termination.

Figure 2 -STS-12 (STM-4/AU-3), STS-12 (STM-4/AU-4) or STS-12c (STM-4-4c) Application with 77.76 MHz Byte Telecombus Interface



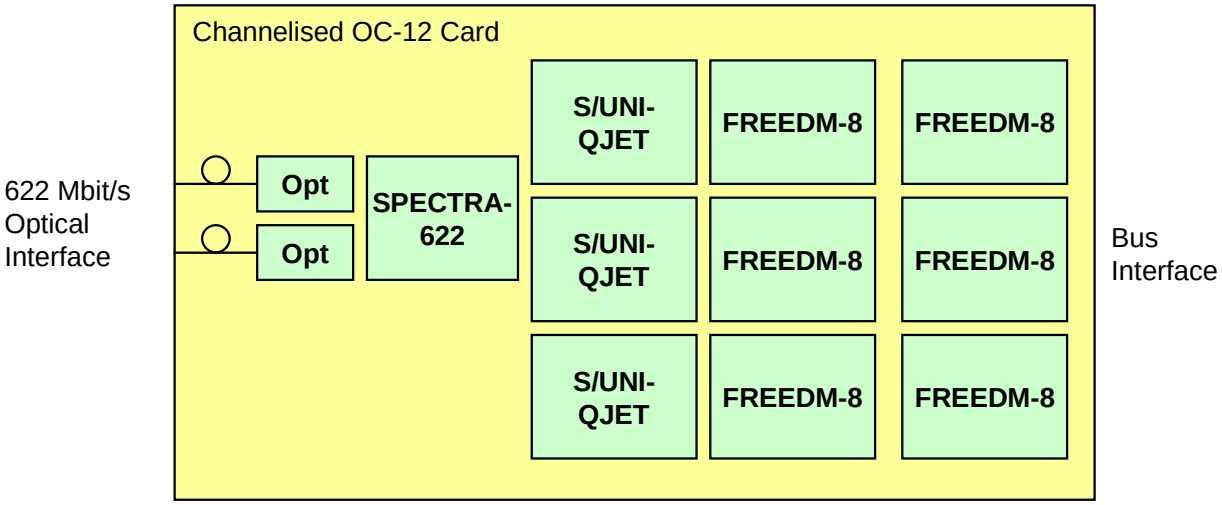
Four SPECTRA-622 devices can be connected to an OC-48 front end transceiver device to implement a STS-48 (STM-16) aggregate interface. Figure 3 shows a block diagram for the STS-48 (STM-16) application. In this application, the OC-48 transceiver performs SONET/SDH section and line processing and the SPECTRA-622 devices perform SONET/SDH path processing, line rate decoupling, and pointer processing.

Figure 3 -STS-48 (STM-16) Application



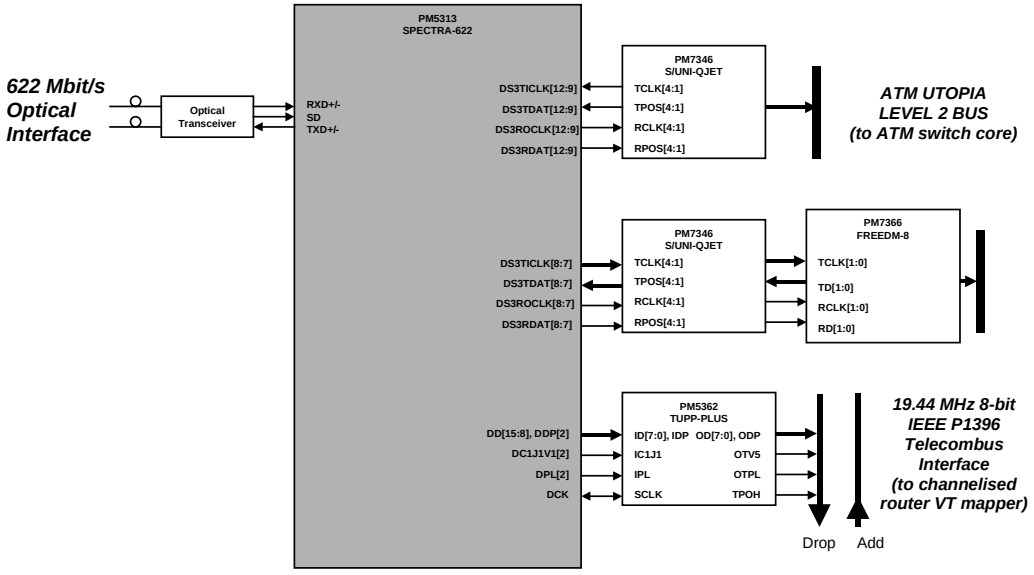
SPECTRA-622 can be used to implement OC-12 interfaces on channelised high speed IP switches and routers. For OC-12 interfaces with DS-3 channelisation, the SPECTRA-622 has on-chip DS-3 mappers to facilitate direct connection to the PM7346 S/UNI-QJET for DS-3 framing. The circuit shown inFigure 4 implements a channelised OC-12 interface for the high speed router. The PCI bus connects directly to the IP switch/router backplane.

Figure 4 -OC-12 Channelised DS-3 Interface for High Speed IP Switches/Routers

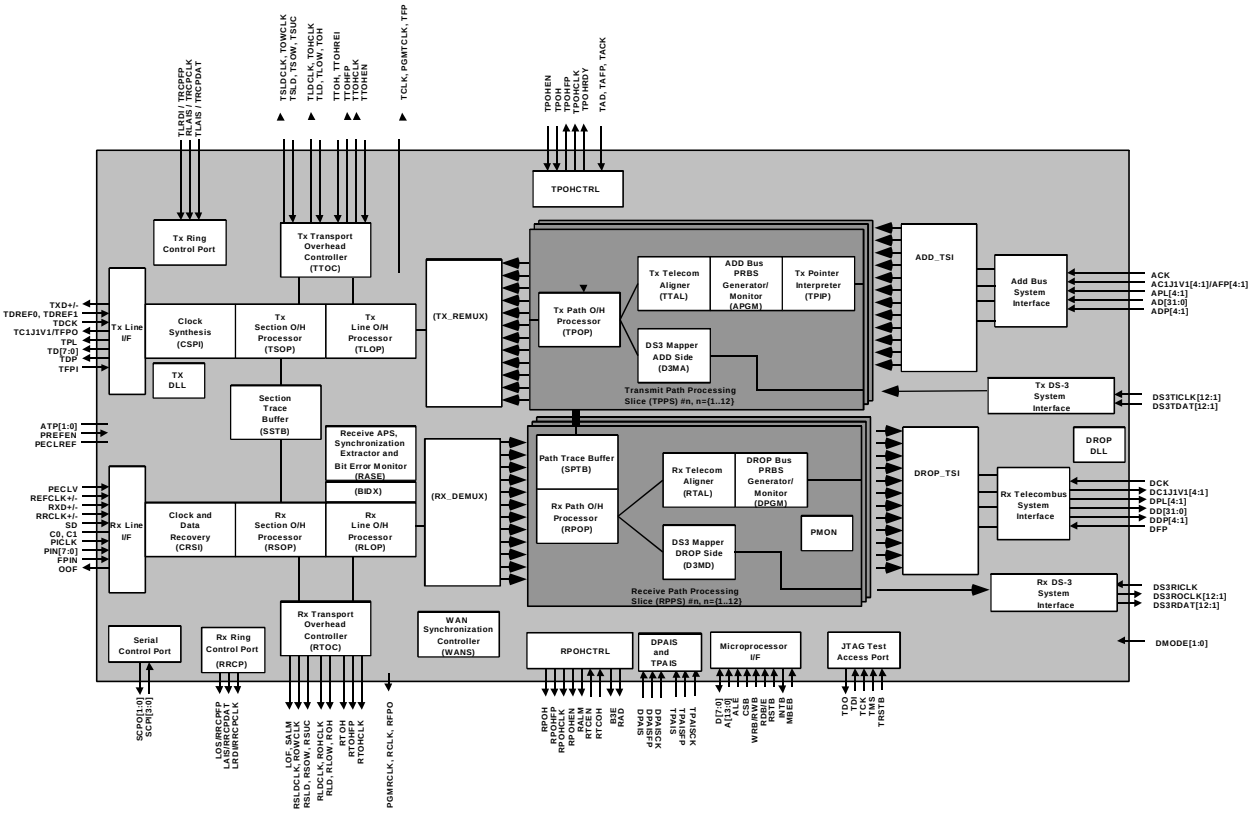


SPECTRA-622 allows simultaneous access to system-side DS-3 interface and the system-side telecom bus interface. DS-3 access is selectable on an STS-1 basis. The SPECTRA-622 can be used to aggregate OC-12 traffic on a platform that supports ATM, Frame Relay, IP, and TDM traffic. Figure 5 shows the implementation of a multi-service channelised OC-12 interface using the SPECTRA-622.

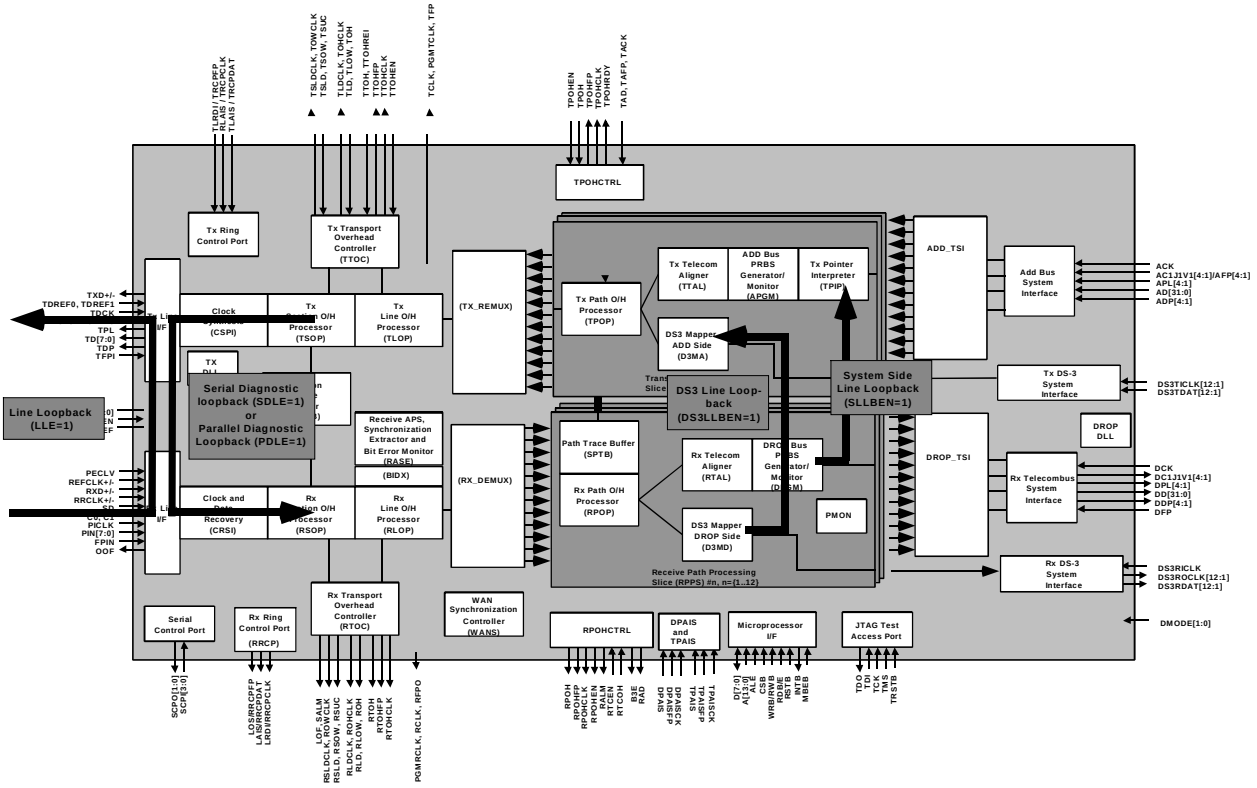
Figure 5 -Multi-service Channelised OC-12 Aggregate Interface for High Speed IP Switches/Routers



6 BLOCK DIAGRAM



7 LOOPBACK MODES



8 DESCRIPTION

The PM5313 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER (SPECTRA-622) terminates the transport and path overhead of STS-12 (STM-4/AU3 or STM-4/AU4) and STS-12c (STM-4-4c) streams at 622.08 Mbit/s. The SPECTRA-622 implements significant functions for a SONET/SDH compliant line interface, as well as DS3 mapping.

The SPECTRA-622 receives SONET/SDH frames via a bit serial interface, recovers clock and data, and terminates the SONET/SDH section (regenerator section), line (multiplexer section), and path. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-622 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3), monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result and extracts the synchronous payload envelope (virtual container). All transport and path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is placed on a Telecom DROP bus and optionally serialized into DS3 streams. For Telecombus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. For the DS3 application, the SPECTRA-622 demaps the DS3s from the STS-12 (STM-4/AU3/AU4) SPE and provides serialized bit streams with derived clocks. Both the Telecom and DS3 DROP buses can be active at the same time supporting a mixed use de-multiplexer function on the system DROP side.

The SPECTRA-622 transmits SONET/SDH frames, via a bit serial interface, and formats section (regenerator section), line (multiplexer section), and path overhead appropriately. The SPECTRA-622 provides transmit path origination for a SONET/SDH STS-12 (STM-4/AU3 or STM-4/AU4) or STS-12c (STM-4-4c) stream. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. Line remote error indications (M1) are

optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the SPECTRA-622 generates the transmit payload pointers (H1, H2), creates and inserts the path BIP, optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1). In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-622 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPECTRA-622 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and BIP errors, which are useful for system diagnostics and tester applications.

The inserted SPE (VC) is either sourced from a Telecombus ADD stream or from DS3 serial streams. For Telecombus applications, the SPECTRA-622 maps the SPE from a Telecom ADD bus into the transmit stream. Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD bus are accommodated by pointer adjustments in the transmit stream. For the DS3 application, the SPECTRA-622 maps the DS3s into an STS-12 (STM-4/AU3/AU4) SPE. Both the Telecom and DS3 ADD buses can be active at the same time supporting a mixed use multiplexer function on the system ADD side.

The SPECTRA-622 supports Time-Slot Interchange (TSI) on the Telecom ADD and DROP buses. On the DROP side, the TSI views the receive stream as twelve independent time-division multiplexed columns of data (i.e. twelve constituent STS-1 (STM-0/AU3) or equivalent streams or time-slots or columns). Any column can be connected to any time-slot on the DROP bus. Both column swapping and broadcast are supported. Time-Slot Interchange is independent of the underlying payload mapping formats. Similarly, on the ADD side, data from the ADD bus is treated as twelve independent time-division multiplexed columns. Assignment of data columns to transmit time-slots (STS-1 (STM-0/AU3) or equivalent streams) is arbitrary.

The transmitter and receiver are independently configurable to allow for asymmetric interfaces. Ring control ports are provide to pass control and status information between mate transceivers. The SPECTRA-622 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The SPECTRA-622 is implemented in low power, +3.3 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 520 pin SBGA package.

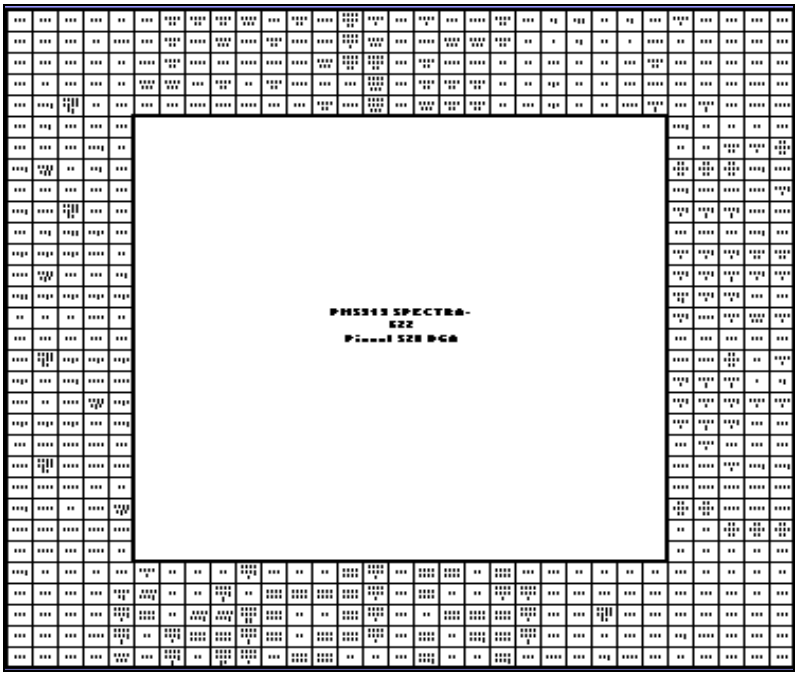
9 PIN DIAGRAMS

The SPECTRA-622 is available in a 520 pin SBGA package having a body size of 40 mm by 40 mm and a ball pitch of 1.27 mm.

Section views of the SPECTRA-622 Pin diagram follow Figure 6

Figure 6 -Full View of SPECTRA-622 diagram

A31-T31 A1-T17



AL18-U31 UL-AL17

Bottom View

Figure 7 -Section View of SPECTRA-622 Pin diagram, A1-T17

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
RSVD2	GND	RSVD1	B3E	DPAIS	DPAISP	GND	D[1]	A[11]	A[6]	A[1]	GND	TRSTB	GND	GND	GND	VDD	A
PGMTCLK	GND	RPOH	TPOHRDY	TPOHCLK	DPAISCK	D[4]	D[0]	A[10]	A[5]	A[0]	RDB/E	TDI	TCK	GND	VDD	GND	B
TLRDI/TRCPFP	VDD	RPOHEN	TPOH	TPAIS	D[7]	D[3]	INTB	A[9]	A[4]	CSB	WRB/RWB	TDO	VDD	VDD	GND	GND	C
TLAIS/TRCPDAT	VDD	RPOHFP	TPOHEN	TPAISFP	D[6]	D[2]	A[13]	A[8]	A[3]	ALE	RSTB	TMS	VDD	VDD	SCPO[0]	GND	D
RLAIS/R	VDD	RPOHLK	TPOHFP	TPAISCK	D[5]	VDD	A[12]	A[7]	A[2]	MBEB	VBIAS[1]	VDD	SCPO[1]	SCPI[0]	SCPI[2]	SCPI[3]	E
Bottom View												SCPI[1]	N/C	N/C	N/C	GND	F
												N/C	N/C	PREFEN	PECLV	N/C ANALOG	G
												N/C ANALOG	N/C ANALOG	N/C ANALOG	AVD[10]	AVS[9]	H
												AVS[10]	AVD[9]	AVS[8]	AVD[8]	AVS[12]	J
												AVD[12]	AVS[11]	AVD[11]	SAVS[0]	QAVS[0]	K
												VDD	QAVD[0]	ATP0	ATP1	GND	L
												PBIAS[2]	AVD[14]	AVD[13]	REFCLK+	REFCLK-	M
												AVS[13]	AVS[14]	SAVS[1]	AVD[17]	TDREF0	N
												TDREF1	AVS[17]	AVD[18]	TXD+	TXD-	P
												AVS[18]	PBIAS[0]	SAVS[2]	PECLREF	SAVS[3]	R
												VDD	VDD	VDD	GND	GND	T

Figure 8 -Section View of SPECTRA-622 Pin diagram, U1-AL17

Bottom View												AVD [4]	AVS[4]	N/C ANA LOG	SD	SAVS[4]	**U**
												AVS[16]	QAVS[1]	QAVD [1]	C0	C1	**V**
												AVD [15]	PBIAS [3]	AVD [16]	RRCLK-	RRCLK+	**W**
												SAVS[5]	PBIAS [1]	AVS [15]	RXD+	RXD-	**Y**
												VDD	SAVS [6]	AVS [0]	AVD [0]	GND	**AA**
												AVD [3]	AVD [2]	SAVS [7]	AVS[1]	AVD [1]	**AB**
												AVD [6]	AVD [5]	AVS [5]	AVS [3]	AVS [2]	**AC**
												N/C ANA LOG	N/C ANA LOG	AVD [7]	AVS [7]	AVS [6]	**AD**
												N/C	N/C	N/C ANA LOG	N/C ANA LOG	N/C ANA LOG	**AE**
												N/C	N/C	N/C	N/C	GND	**AF**
DS3ROCLK[8]	VDD	DS3TDAT[4]	DS3TICLK[3]	N/C	DS3RDAT[4]	VDD	TFPI	N/C	N/C	N/C	N/C	VDD	N/C	N/C	N/C	N/C	**AG**
DS3ROCLK[7]	VDD	DS3TDAT[3]	N/C	N/C	DS3ROCLK[4]	DS3ROCLK[3]	TD[6]	TD[2]	OOF	FPIN	PIN[6]	PIN[3]	VDD	VDD	N/C	GND	**AH**
DS3ROCLK[6]	VDD	N/C	DS3TICLK[4]	DS3TICLK[2]	DS3RDAT[3]	DS3ROCLK[2]	TD[7]	TD[3]	TC1J1V1/TFO	PIN[7]	PIN[5]	PIN[2]	VDD	VDD	GND	GND	**AJ**
DS3ROCLK[5]	GND	DS3TDAT[2]	N/C	DS3TICLK[1]	DS3RDAT[2]	DS3ROCLK[1]	TDP	TD[4]	TD[0]	TPL	PIN[4]	PIN[1]	PICLK	GND	VDD	GND	**AK**
N/C	GND	DS3TDAT[1]	N/C	N/C	DS3RDAT[1]	GND	TDCK	TD[5]	TD[1]	TCLK	GND	PIN[0]	GND	GND	GND	VDD	**AL**
17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

Figure 9 -Section View of SPECTRA-622 Pin diagram, AL18-U31

U	APL[3]	AC1J1V1 /AFP [3]	AD[16]	AD[17]	AD[18]									
V	AD[19]	AD[20]	AD[21]	AD[22]	AD[23]									
W	ADP[3]	N/C	DPL[3]	DC1J1V1 [3]	DD[16]									
Y	DD[17]	DD[18]	DD[19]	DD[20]	DD[21]									
AA	GND	DD[22]	DD[23]	DDP[3]	VDD									
AB	APL[4]	AC1J1V1 /AFP [4]	AD[24]	AD[25]	AD[26]									
AC	AD[27]	AD[28]	AD[29]	AD[30]	N/C									
AD	AD[31]	ADP[4]	N/C	DPL[4]	DC1J1V1 [4]									
AE	DD[24]	DD[25]	DD[26]	DD[27]	DD[28]									
AF	GND	DD[29]	DD[30]	DDP[4]	N/C									
AG	DD[31]	N/C	DFP	N/C	VDD	DMODE [0]	N/C	N/C	N/C	DS3RDA T[12]	VDD	N/C	N/C	DS3RDA T[5]
AH	GND	DCK	VDD	VDD	DMODE [1]	DS3TDA T[10]	N/C	N/C	DS3RDA T[11]	N/C	DS3TDA T[8]	DS3TDA T[5]	DS3TICL K[7]	DS3RDA T[6]
AJ	GND	GND	VDD	VDD	DS3TDA T[12]	DS3TDA T[9]	N/C	DS3TICL K[10]	DS3RDA T[10]	DS3ROC LK[11]	DS3TDA T[7]	N/C	N/C	DS3RDA T[7]
AK	GND	VDD	GND	VBIAS [0]	DS3TDA T[11]	N/C	DS3TICL K[12]	DS3TICL K[9]	DS3RDA T[9]	DS3ROC LK[10]	DS3TDA T[6]	N/C	DS3TICL K[6]	DS3RDA T[8]
AL	VDD	GND	GND	GND	DS3RICL K	GND	DS3TICL K[11]	N/C	DS3ROC LK[12]	DS3ROC LK[9]	GND	DS3TICL K[8]	DS3TICL K[5]	N/C
	31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**

Bottom View

Figure 10 -Section View of SPECTRA-622 Pin diagram, A31-T31

	31	30	29	28	27	26	25	24	23	22	21	20	19	18
A	VDD	GND	GND	GND	N/C	GND	TOHCLK	TOWCLK	TTOHREI	RTOHCLK	GND	ROWCLK	RALM	LRDI/RRCPCLK
B	GND	VDD	GND	N/C	TACK	RAD	TTOHFP	TSUC	TSLDCLK	RCLK	ROHCLK	RSOW	RSLD	LOS/RRCPFP
C	GND	GND	VDD	VDD	N/C	TAFP	TTOHEN	TLOW	TLD	RFPO	RTOH	RSUC	RSLDCLK	LAIS/RRCPDAT
D	GND	N/C	VDD	VDD	N/C	PGMRCLK	TTOHCLK	TOH	TLDCLK	N/C	RTOHFP	RLOW	RLD	LOF
E	ACK	APL[1]	AC1J1V1/AFP[1]	AD[0]	VDD	TFP	TAD	TTOH	TSOW	TSLD	VDD	ROH	RLDCLK	SALM
F	GND	AD[1]	AD[2]	AD[3]	AD[4]									
G	AD[5]	AD[6]	AD[7]	ADP[1]	N/C									
H	DPL[1]	DC1J1V1[1]	DD[0]	DD[1]	DD[2]									
J	DD[3]	DD[4]	DD[5]	DD[6]	DD[7]									
K	DDP[1]	APL[2]	AC1J1V1/AFP[2]	AD[8]	AD[9]									
L	GND	AD[10]	AD[11]	AD[12]	VDD									
M	AD[13]	AD[14]	AD[15]	ADP[2]	N/C									
N	DPL[2]	DC1J1V1[2]	DD[8]	DD[9]	DD[10]									
P	DD[11]	DD[12]	DD[13]	DD[14]	DD[15]									
R	N/C	N/C	N/C	DDP[2]	N/C									
T	GND	GND	VDD	VDD	VDD									

Bottom View

10 PIN DESCRIPTION (520)

10.1 Serial Line side Interface Signals

Pin Name	Type	Pin No.	Function
PECLV	Input	G2	The PECL signal voltage select (PECLV) selects between 3.3V PECL or 5V PECL signaling for the PECL inputs. When PECLV is low, the PECL inputs expect a 5V PECL signal. When PECLV is high, the PECL inputs expect a 3.3V PECL signal. The PECL biasing pins PBIAS[3:0] should be set to the appropriate voltage. This input pin is 5 Volt tolerant. Please refer to the Operation section for a discussion of PECL interfacing issues
REFCLK+ REFCLK-	PECL Input	M2 M1	The differential reference clock inputs (REFCLK+/-) must provide a jitter-free 77.76 MHz reference clock. It is used as the reference clock by both clock recovery and clock synthesis circuits. When the WAN Synchronization controller is used, REFCLK+/- is supplied using a VCXO. In that application, the transmit direction can be externally looped timed to the line receiver in order to meet wander transfer and holdover requirements. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
RXD+ RXD-	PECL Input	Y2 Y1	The receive differential data PECL inputs (RXD+/-) contain the STS-12 (STM-4) 622.08 Mbit/s NRZ encoded bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream when clock recovery is not bypassed. RXD+/- is sampled on the rising edge of RRCLK+/- (falling edge may be used by reversing RRCLK+/-) when clock recovery is bypassed. The polarity of the RXD pins can be changed by the RXDINV bit in register 0003H. Clock recovery bypass is selectable using the RBYP bit in the SPECTRA-622 Line Configuration #1 register. Please refer to the Operation section for a discussion of PECL interfacing issues.
RRCLK+ RRCLK-	PECL Input	W1 W2	The receive differential clock inputs (RRCLK+/-) are used when clock recovery is bypassed. RRCLK+/- is nominally a 622.08 MHz 50% duty cycle clock and provides timing for the SPECTRA-622 receive functions. In this case, RXD+/- is sampled on the rising edge of RRCLK+/-. RRCLK+/- is ignored when clock recovery is enabled. Clock recovery bypass is selectable using the RBYP bit in the SPECTRA-622 Line Configuration #1 register. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
SD	PECL Input	U2	The receive signal detect PECL input (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A PECL logic high indicates the presence of valid data. A PECL logic low indicates a loss of signal. In clock recovery mode, when SD is low, the receive serial data is forced to all zeros and the phase locked loop switches to the reference clock (REFCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled. Please refer to the Operation section for a discussion of PECL interfacing issues.
TXD+ TXD-	PECL Output	P2 P1	The transmit differential data outputs (TXD+/-) contain the STS-12 (STM-4) 622.08 Mbit/s NRZ encode bit serial transmit stream. The TXD+/- outputs are driven using the synthesized clock from the CSU or the recovery clock from the CRU when loop timing is enabled. Loop timing is enabled by setting the LOOPT bit in the SPECTRA-622 Line Configuration #1 register to logic one. The TC1J1V1/TFPO output may be used to identify the frame alignment on TXD+/-. It will rising 15 bits (+/- 3 bits) before the first byte of the SPE. Please refer to the Operation section for a discussion of PECL interfacing issues.
SCPO[1] SCPO[0]	Tristate Output	E4 D2	The status and control port outputs (SCPO[1:0]) provides two drive points for controlling auxiliary devices. The signal levels on these outputs correspond to the bit values contained in the SPECTRA-622 Serial Control Port Status and Control register. SCPO[1:0] can be tristate using the SCPO_TS bit in the SPECTRA-622 Serial Control Port Status and Control register. On reset, these outputs will be tristate by default.

Pin Name	Type	Pin No.	Function
SCPI[3] SCPI[2] SCPI[1] SCPI[0]	Input	E1 E2 F5 E3	The status and control port inputs (SCPI[3:0]) are used to monitor the operation of auxiliary devices. An interrupt may be generated when state changes are detected on these monitored signals. State changes and the real-time signal levels on this port are available in the SPECTRA-622 Serial Control Port Status and Control register. Each of the inputs contains an internal pull up resistor.

10.2 Parallel Line Side Interface Signals

Pin Name	Type	Pin No.	Function
PICLK	Input	AK4	The parallel input clock (PICLK) provides timing for SPECTRA-622 receive function when the device is configured for the parallel interface mode of operation. PICLK is a 77.76 MHz nominally 50% duty cycle clock. PIN[7:0] and FPIN are sampled on the rising-edge of PICLK.
PIN[0] PIN[1] PIN[2] PIN[3] PIN[4] PIN[5] PIN[6] PIN[7]	Input	AL5 AK5 AJ5 AH5 AK6 AJ6 AH6 AJ7	The parallel data input (PIN[7:0]) bus carries the byte-serial STS-12 (STM-4) stream when the device is configured for the parallel interface mode of operation. PIN[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). PIN[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). The polarity of the PIN[7:0] pins can be changed by the RXDINV bit in register 0003H. PIN[7:0] is sampled on the rising edge of PICLK.

Pin Name	Type	Pin No.	Function
FPIN	Input	AH7	The active-high framing position input (FPIN) signal indicates the SONET/SDH frame position on the PIN[7:0] bus when the device is configured for the parallel interface mode of operation. The operation of the FPIN input is controlled by the PFPEN bit in the CRSI Configuration and Interrupt register. When PFPEN is set to logic one, FPIN is set high to mark the first synchronous payload envelope byte position after the J0/Z0 bytes on PIN[7:0]. FPIN may also mark the third A2 byte as controlled by FPPOS in SPECTRA-622 Line Configuration #2 register (0003H) When PFPEN is set to logic zero, FPIN is ignored and the SPECTRA-622 will frame to the incoming data on PIN[7:0]. The SPECTRA-622 will frame to the incoming data on PIN[7:0] regardless of the byte alignment or frame alignment of the incoming stream. FPIN is sampled on the rising edge of PICLK.
OOF	Output	AH8	The out of frame (OOF) signal is high while the SPECTRA-622 is out of frame. OOF is set low while the SPECTRA-622 is in-frame. An out of frame declaration occurs when four consecutive errored framing patterns (A1 and A2 bytes) have been received. OOF can be used to enable an upstream framing pattern detector to search for the framing pattern. OOF is updated on the rising edge of RCLK.

Pin Name	Type	Pin No.	Function
TDCK	Input	AL10	The parallel transmit data clock (TDCK) provides timing for SPECTRA-622 transmit function operation when the device is configured for the parallel interface mode of operation only. When both the serial and parallel interfaces are enabled, the parallel input clock is ignored. TDCK is a 77.76 MHz nominally 50% duty cycle clock.
TFPI	Input	AG10	The transmit frame pulse input is an active high pulse identifying the first synchronous payload envelope byte in the STS-12 (STM-4) frame on TD[7:0] bus or TXD+/- outputs. Selection of whether TFPI indicates framing position on the TD[7:0] or the TXD+/- is controlled by the TX_LIFSEL[1:0] bits in the SPECTRA-622 Line Configuration #1 register. If LIFSEL is 01b, TFPI indicates framing position on the TD[7:0] bus. If TX_LIFSEL[1:0] is 00b or 11b, TFPI indicates framing position on the TXD+/- outputs. TFPI should be set high for a single TCLK period every 9720 TCLK cycles. It is not necessary for TFPI to be present at every frame, an internal counter fly-wheels based on the most recent TFPI received. TFPI may be set low if such synchronization is not required. TFPI is sampled on the rising edge of TCLK.
TD[0] TD[1] TD[2] TD[3] TD[4] TD[5] TD[6] TD[7]	Output	AK8 AL8 AH9 AJ9 AK9 AL9 AH10 AJ10	The parallel transmit data (TD[7:0]) bus carries the STS-12 (STM-4) SONET/SDH transmit stream in byte serial format. TD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). TD[7:0] is updated on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TPL	Output	AK7	The transmit payload output (TPL) is an active high signal that indicates when the transmit data bus TD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. TPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. TPL is updated on the rising edge of TCLK.
TC1J1V1/	Output	AJ8	The transmit composite timing signal (TC1J1V1) indicates the frame, payload and tributary multiframe boundaries on the transmit data bus TD[7:0] when the TC1J1V1EN bit in the SPECTRA-622 Transmit Telecom Bus Configuration register is set high. TC1J1V1 pulses high with the transmit payload active signal (TPL) set low to mark the first STS-1 (STM-0/AU3) identification byte (C1). TC1J1V1 pulses high with TPL set high to mark the path trace byte(s) (J1). Optionally, the TC1J1V1 signal pulses high on the V1 byte(s) to indicate tributary multiframe boundaries. TC1J1V1 is updated on the rising edge of TCLK.
TFPO	Output		The transmit frame pulse output (TFPO) is an active-high signal marking the frame alignment on the serial stream TXD+/- or parallel transmit data TD[7:0] when the TC1J1V1EN bit in the SPECTRA-622 Transmit Telecom Bus Configuration register is set low. In parallel mode, TFPO is set high for a single TCLK period during the first SPE (synchronous payload envelope) byte after the J0/Z0 bytes on TD[7:0]. In serial mode, it will rising 15 bits (+/- 3 bits) before the first byte of the SPE on TXD. TFPO is updated on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TDP	Output	AK10	The transmit data parity signal (TDP) indicates the parity of the transmit line interface signals. The transmit data bus (TD[7:0]) is always included in parity calculations. The INCTPL and INCTC1J1V1 register bits in the SPECTRA-622 Transmit Telecom Bus Configuration register control the inclusion of the TPL and TC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. TDP is updated on the rising edge of TCLK.

10.3 Receive and Transmit Clocks

Pin Name	Type	Pin No.	Function
RCLK	Output	B22	The receive clock (RCLK) output provides a timing reference for the SPECTRA-622 receive line interface outputs. RCLK is a nominally 77.76 MHz, 50% duty cycle clock. When clock recovery is enabled, RCLK is a divide by eight version of the recovered clock. When clock recovery is bypassed, RCLK is a divide by eight version of the recovered RRCLK+/- inputs. In parallel interface mode, PGMRCLK is a buffered version of the PICLK input. The RCLK output can be disabled and held low by programming the RCLKEN bit in the SPECTRA-622 Clock Control register. RFPO, SALM, LOF, LOS, OOF, LRDI and LAIS are updated on the rising edge of RCLK. RLAIS is sampled on the rising edge of RCLK.

Pin Name	Type	Pin No.	Function
PGMRCLK	Output	D26	The programmable receive clock (PGMRCLK) output provides a timing reference for the SPECTRA-622 synchronous line and system receive functions. The PGMRCLKSEL register bit in the SPECTRA-622 Clock Control register controls the frequency of the PGMRCLK output. When the PGMRCLKSEL register bit is set to low, PGMRCLK is a nominally 77.76 MHz, 50% duty cycle clock. When clock recovery is enabled, PGMRCLK is a divide by eight version of the recovered clock. When clock recovery is bypassed, PGMRCLK is a divide by eight version of the recovered RRCLK+/- inputs. In parallel interface mode, PGMRCLK is a buffered version of the PICLK input. When PGMRCLKSEL register bit is set to high, PGMRCLK is a nominally 19.44 MHz, 50% duty cycle clock. When clock recovery is enabled, PGMRCLK is a divide by thirty-two version of the recovered clock. When clock recovery is bypassed, PGMRCLK is a divide by thirty-two version of the recovered RRCLK+/- inputs. The PGMRCLK output can be disabled and held low by programming the PGMRCLKEN bit in the SPECTRA-622 Clock Control register.

Pin Name	Type	Pin No.	Function
TCLK	Output	AL7	The transmit byte clock (TCLK) output provides a timing reference for the SPECTRA-622 transmit functions. TCLK is a nominally 77.76 MHz. When the parallel line interface is enabled without the serial interface, TCLK is a buffered version of TDCK. In all modes where the serial line interface is enabled, TCLK is a divide by eight version of the synthesized transmit line clock. TCLK has an arbitrary phase alignment with respect to the synthesized serial 622.06 MHz transmit clock. The TCLK output can be disabled and held low by programming the TCLKEN bit in the SPECTRA-622 Clock Control register. TFP, TC1J1V1/TFPO, TPL, TDP and TD[7:0] are updated on the rising edge of TCLK. TFPI, TLRDI and TLAIS are sampled on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
PGMTCLK	Output	B17	The programmable transmit clock (PGMTCLK) output provides a timing reference for the SPECTRA-622 synchronous line and system transmit functions. When PGMTCLKSEL register bit is set to low, PGMTCLK is a nominally 77.76 MHz, 50% duty cycle clock. When the parallel line interface is enabled without the serial mode interface, PGMTCLK is a buffered version of TDCK. In all modes where the serial line interface is enabled, PGMTCLK is a divide by eight of the synthesized transmit line clock. When PGMTCLKSEL register bit is set to high, PGMTCLK is a nominally 19.44 MHz, 50% duty cycle clock. When the parallel line interface is enabled without the serial mode interface, PGMTCLK is a divide by four of the TDCK. In all modes where the serial line interface is enabled, PGMTCLK is a divide by thirty-two of the synthesized transmit line clock. The PGMTCLKSEL register bit may be found in the SPECTRA-622 Clock Control register The PGMTCLK output can be disabled and held low by programming the PGMTCLKEN bit in the SPECTRA-622 Clock Control register.

10.4 Section/Line Status and Alarms Signals

Pin Name	Type	Pin No.	Function
RFPO	Tristate Output	C22	The receive frame pulse (RFPO) is an 8 kHz signal derived from the receive clock RCLK when the framing alignment has been found and the SPECTRA-622 is in frame (the OOF output and register bit are logic 0). RFPO pulses high for one RCLK cycle every 9720 RCLK cycles (STS-12 / STM-4). RFPO can be tristated using the ROH_TS bit in the RTOC Receive Overhead Control register. RFPO is updated on the rising edge of RCLK.
TFP	Tristate Output	E26	The transmit frame pulse (TFP) is an 8 kHz signal derived from the transmit clock TCLK when the transmit interface is in frame alignment. TFP pulses high for one TCLK cycle every 9720 TCLK cycles (STS-12/STM-4). TFP can be tristated using the TOH_TS bit in the TTOC Transmit Overhead Output Control register. TFP is updated on the rising edge of TCLK.
SALM	Output	E18	The section alarm (SALM) output is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), section trace identifier mismatch (RS-TIM), section trace identifier unstable (RS-TIU), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SPECTRA-622 Section Alarm Output Control #1 and #2 registers. SALM is set low when none of the enabled alarms are active. SALM is updated on the rising edge of RCLK.

Pin Name	Type	Pin No.	Function
LOF	Output	D18	The loss of frame (LOF) signal is set high when an out of frame state persists for 3 ms. LOF is set low when an in frame state persists for 3 ms. LOF is updated on the rising edge of RCLK.
LOS/	Output	B18	Loss of signal (LOS) is active when the ring control port is disabled. Loss of signal (LOS) is set high when a violating period (20 ± 2.5 µs) of consecutive all zeros patterns is detected in the incoming stream. LOS is set low when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. LOS is updated on the rising edge of RCLK.
RRCPFP			The receive ring control port frame position (RRCPFP) signal identifies bit positions in the receive ring control port data (RRCPDAT) when the ring control port is enabled. RRCPFP is set high during the filtered K1 and K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send line AIS and send line RDI bit positions in the RRCPDAT stream. RRCPFP can be connected directly to the TRCPFP input of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. RRCPFP is updated on the falling edge of RRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

Pin Name	Type	Pin No.	Function
LRDI/	Output	A18	The line remote defect indication (LRDI) signal is active when the ring control port is disabled. LRDI is set high when line RDI is detected in the incoming stream. LRDI is declared when the 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LRDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The selection of 3 or 5 consecutive frames is controlled by the LRDIDET bit in the RLOP Control and Status register. LRDI is updated on the rising edge of RCLK.
RRCPCLK			The receive ring control port clock (RRCPCLK) signal provides timing for the receive ring control port when the ring control port is enabled. RRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and can be connected directly to the TRCPCLK input of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

Pin Name	Type	Pin No.	Function
LAIS/	Output	C18	The line alarm indication (LAIS) signal is active when the ring control port is disabled. LAIS is set high when line AIS is detected in the incoming stream. LAIS is declared when the 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The selection of three or five consecutive frames is controlled by the LAISDET bit in the RLOP Control and Status register. LAIS is updated on the rising edge of RCLK.
RRCPDAT			The receive ring control port data (RRCPDAT) signal contains the receive ring control port data stream when the ring control port is enabled. The receive ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send line AIS and send line RDI bit positions, and the line REI bit positions. RRCPDAT can be connected directly to the TRCPDAT input of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. RRCPDAT is updated on the falling edge of RRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

Pin Name	Type	Pin No.	Function
RLAIS/	Input	E17	The receive line AIS insertion (RLAIS) signal controls the insertion of line AIS in the receive outgoing stream, when the ring control port is disabled. When RLAIS is set high, line AIS is inserted in the receive outgoing stream. When RLAIS is set low, line AIS may be optionally inserted automatically upon detection of loss of signal, loss of frame, section trace alarms or line AIS in the incoming stream. RLAIS is sampled on the rising edge of RCLK. The SPECTRA-622 Receive LAIS Control register contains the register bits that control the alarms that are inserted using the RLAIS pin.
TRCPCLK			The transmit ring control port clock (TRCPCLK) signal provides timing for the transmit ring control port when the ring control port is enabled. TRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and can be connected directly to the RRCPCLK output of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

Pin Name	Type	Pin No.	Function
TLRDI/	Input	C17	The active high transmit line remote defect indication (TLRDI) signal controls the insertion of a remote defect indication in the transmit outgoing stream when the ring control port is disabled. When TLRDI is set high, bits 6, 7, and 8 of the K2 byte are set to the pattern 110. When TLRDI is set low, line RDI may also be inserted using the LRDI bit in the TLOP Control register, or upon detection of loss of signal, loss of frame, or line AIS in the receive stream, using the bits in the SPECTRA-622 Line RDI Control register. The TLRDI input takes precedence over the TTOH and TTOHEN inputs. TLRDI is sampled on the rising edge of TCLK.
TRCPFP			The transmit ring control port frame position (TRCPFP) signal identifies bit positions in the transmit ring control port data (TRCPDAT) when the ring control port is enabled. TRCPFP is high during the filtered K1, K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, the send line AIS and the send line RDI bit positions in the TRCPDAT stream. TRCPFP can be connected directly to the RRCPFP output of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. TRCPFP is sampled on the rising edge of TRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

Pin Name	Type	Pin No.	Function
TLAIS/	Input	D17	The active high transmit line alarm indication signal (TLAIS) controls the insertion of line AIS in the transmit outgoing stream when the ring control port is disabled. When TLAIS is set high, the complete frame (except the section overhead or line/regenerator section) is overwritten with the all ones pattern (before scrambling). The TLAIS input takes precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of TCLK.
TRCPDAT			The transmit ring control port data (TRCPDAT) signal contains the transmit ring control port data stream when the ring control port is enabled. The transmit ring control port data consist of the send line AIS, the send line RDI bit positiions and the line REI bit positions.TRCPDAT can be connected directly to the RRCPDAT output of a mate SPECTRA-622 in ring-based add-drop multiplexer applications. TRCPDAT is sampled on the rising edge of TRCPCLK. The enabling and disabling of the ring control port is controlled by the RCPEN bit in the SPECTRA-622 Ring Control register.

10.5 Receive Transport Overhead Extraction Signals

Pin Name	Type	Pin No.	Function
RSLDCLK	Tristate Output	C19	The receive section or line data communication channel (DCC) clock (RSLDCLK) is used to update the received section or line DCC (RSLD). A smooth or gapped version of this clock may be selected. When selecting the smooth clock and clocking the section DCC, RSLDCLK is a 192 kHz clock with nominal 50% duty cycle. When selecting to clock the line DCC, RSLDCLK is a 576 kHz clock with nominal 50% duty cycle. When selecting the gapped clock and clocking the section DCC, RSLDCLK is a 192 kHz clock generated by gapping a 216 kHz clock. When line DCC is selected, RSLDCLK is a 576 kHz clock generated by gapping a 2.16 MHz clock. In all cases, RSLD is updated on the falling edge of RSLDCLK. In gapped clock mode, a gap detector on RSLDCLK is needed to identify the MSB on RSLD. A edge detection of RFPO may also be used. In smooth clock mode, RTOHFP may be sampled high at the same time as the MSB on RSLD. The RTOC Overhead Control register contains the RSLDSEL register bit used to select the section or line DCC. The same register also contains the RX_GAPSEL register bit used to select the smooth or gapped RSLDCLK output clock and the RSLD_TS register bit that can be used to tri-state RSLDCLK and RSLD outputs.

Pin Name	Type	Pin No.	Function
RSLD	Tristate Output	B19	The receive section or line DCC (RSLD) bit serial output signal contains the received section data communication channel (D1-D3) or the line data communication channel (D4-D12). RSLD is updated on the falling edge of RSLDCLK and should be sampled externally on the rising edge of RSLDCLK. The RTOC Overhead Control register contains the RSLDSEL register bit used to select the section or line DCC. The same register also contains the RX_GAPSEL register bit used to select the smooth or gapped RSLDCLK output clock and the RSLD_TS register bit that can be used to tri-state RSLDCLK and RSLD outputs.
RLDCLK	Tristate Output	E19	The receive line data communication channel (DCC) clock (RLDCLK) is used to update the received line DCC (RLD). A smooth or gapped version of this clock may be selected. When selecting the smooth clock, RLDCLK is a 576 kHz clock with nominal 50% duty cycle. When selecting the gapped clock, RLDCLK is a 576 kHz clock, with nominal 66%/33% duty cycle, generated by gapping a 2.16 MHz clock. In all cases, RLD is updated on the falling edge of RLDCLK. In gapped clock mode, a gap detector on RLDCLK is needed to identify the MSB on RLD. A edge detection of RFPO may also be used. In smooth clock mode, RTOHFP may be sampled high at the same time as the MSB on RLD. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped RLDCLK output clock and the RLD_TS register bit that can be used to tri-state RLDCLK and RLD outputs.

Pin Name	Type	Pin No.	Function
RLD	Tristate Output	D19	The receive line DCC (RLD) bit serial output signal contains the received line data communication channel (D4-D12). RLD is updated on the falling edge of RLDCLK and should be sampled externally on the rising edge of RLDCLK. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped RLDCLK output clock and the RLD_TS register bit that can be used to tri-state RLDCLK and RLD outputs.
ROWCLK	Output	A20	The receive order wire clock (ROWCLK) is used to update the received section orderwire, user channel and line orderwire. (RSOW, RSUC and RLOW). A smooth or gapped version of this clock may be selected. When selecting the smooth clock, ROWCLK is a 64 kHz clock with nominal 50% duty cycle. When selecting the gapped clock, ROWCLK is a 64 kHz clock generated by gapping a 72 kHz clock. In all cases, RSOW, RSUC and RLOW are updated on the falling edge of ROWCLK. In gapped clock mode, a gap detector on ROWCLK is needed to identify the MSB on RSOW, RSUC and RLOW. A edge detection of RFPO may also be used. In smooth clock mode, RTOHFP may be sampled high at the same time as the MSB on RSOW, RSUC and RLOW. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped ROWCLK output clock.

Pin Name	Type	Pin No.	Function
RSOW	Output	B20	The receive section order wire (RSOW) bit serial output signal contains the received section order wire(E1). RSOW is updated on the falling edge of ROWCLK and should be externally sampled on the rising edge of ROWCLK. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped ROWCLK output clock.
RSUC	Output	C20	The receive section user channel (RSUC) bit serial output signal contains the received user channel (F1). RSUC is updated on the falling edge of ROWCLK and should be externally sampled on the rising edge of ROWCLK. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped ROWCLK output clock.
RLOW	Output	D20	The receive line order wire (RLOW) bit serial output signal contains the received line order wire(E2). RLOW is updated on the falling edge of ROWCLK and should be externally sampled on the rising edge of ROWCLK. The RTOC Overhead Control register contains the RX_GAPSEL register bit used to select the smooth or gapped ROWCLK output clock.

Pin Name	Type	Pin No.	Function
ROHCLK	Tristate Output	B21	The receive overhead clock (ROHCLK) is used to update the received overhead (ROH) output. A smooth or gapped version of this clock may be selected. When selecting the smooth clock and clocking the section orderwire (E1), user channel (F1) or line order wire (E2), ROHCLK is a 64 kHz clock with nominal 50% duty cycle. When selecting to clock the line APS bytes (K1/K2), ROHCLK is a 128 kHz clock with nominal 50% duty cycle. When selecting the gapped clock and clocking the section orderwire (E1), user channel (F1) or line order wire (E2), ROHCLK is a 64 kHz clock generated by gapping a 72 kHz clock. When selecting to clock the line APS bytes (K1/K2), ROHCLK is a 128 kHz clock generated by gapping a 144 kHz clock. In all cases, ROH is updated on the falling edge of ROHCLK. In gapped clock mode, a gap detector on ROHCLK is needed to identify the MSB on ROH. A edge detection of RFPO may also be used. In smooth clock mode, RTOHFP may be sampled high at the same time as the MSB on ROH. The RTOC Overhead Control register contains the ROHSEL[1:0] register bits used to select the section orderwire, section user channel, line orderwire or line APS bytes. The same register also contains the RX_GAPSEL register bit used to select the smooth or gapped ROHCLK output clock and the ROH_TS register bit that can be used to tri-state ROHCLK and ROH outputs.

Pin Name	Type	Pin No.	Function
ROH	Tristate Output	E20	The receive overhead (ROH) bit serial output signal contains either the received section orderwire (E1), user channel (F1) line order wire (E2) or line APS bytes (K1/K2). ROH is updated on the falling edge of ROHCLK and should be sampled externally on the rising edge of ROHCLK. The RTOC Overhead Control register contains the ROHSEL[1:0] register bits used to select the section orderwire, section user channel, line orderwire or line APS bytes. The same register also contains the RX_GAPSEL register bit used to select the smooth or gapped ROHCLK output clock and the ROH_TS register bit that can be used to tri-state ROHCLK and ROH outputs.
RTOHCLK	Output	A22	The receive transport overhead clock (RTOHCLK) is used to update the received transport overhead outputs (RTOH and RTOHFP). RTOHCLK is nominally a 20.736 MHz clock generated by gapping a 25.92 MHz clock. RTOHCLK has a 33% high duty cycle. RTOHFP and RTOH are updated on the falling edge of RTOHCLK.
RTOH	Output	C21	The receive transport overhead (RTOH) bit serial output signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) from the incoming stream. RTOH is updated on the falling edge of RTOHCLK and should be sampled externally on the rising edge of RTOHCLK.

Pin Name	Type	Pin No.	Function
RTOHFP	Output	D21	The receive transport overhead frame position (RTOHFP) signal is used to locate the most significant bit (MSB) on the RTOH serial stream. RTOHFP is set high when bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. When the RX_GAPSEL register bit is set low in the RTOC Overhead Control register, RTOHFP can be sampled on the rising edges of RSLDCLK, RLDCLK, ROWCLK and ROHCLK to locate the MSB of the RSLD, RLD, RSOW, RSUC, RLOW and ROH serial output streams. In this mode, the generation of these clocks are aligned with the generation of RTOHFP. RTOHFP is updated on the falling edge of RTOHCLK.

10.6 Transmit Transport Overhead Insertion Signals

Pin Name	Type	Pin No.	Function
TSLDCLK	Tristate Output	B23	The transmit section or line data communication channel (DCC) clock (TSLDCLK) is used to clock in the transmit section or line DCC (TSLD). A smooth or gapped version of this clock may be selected. When selecting the smooth clock and clocking the section DCC, TSLDCLK is a 192 kHz clock with nominal 50% duty cycle. When selecting to clock the line DCC, TSLDCLK is a 576 kHz clock with nominal 50% duty cycle. When selecting the gapped clock and clocking the section DCC, TSLDCLK is a 192 kHz clock generated by gapping a 216 kHz clock. When line DCC is selected, TSLDCLK is a 576 kHz clock generated by gapping a 2.16 MHz clock. In all cases, TSLD is sampled on the rising edge of TSLDCLK. In gapped clock mode, a gap detector on TSLDCLK is needed to identify when the most significant bit (MSB) should be present on TSLD. An edge detection on TFP may also be used. In smooth clock mode, TTOHFP may be used to identify the rising edge when the MSB should be present on TSLD. The TTOC Overhead Control register contains the TSLD_SEL register bit used to select the section or line DCC. The same register also contains the TX_GAPSEL register bit used to select the smooth or gapped TSLDCLK output clock and the TSLD_TS register bit that can be used to tri-state the TSLDCLK output.

Pin Name	Type	Pin No.	Function
TSLD	Input	E22	The transmit section or line DCC (RSLD) bit serial input signal contains the section data communication channel (D1-D3) or the line data communication channel (D4-D12) to be transmitted. TSLD is sampled on the rising edge of TSLDCLK. The TTOH and TTOHEN inputs take precedence over TSLD. The TTOC Overhead Control register contains the TSLD_SEL register bit used to select the section or line DCC. The same register also contains the TX_GAPSEL register bit used to select the smooth or gapped TSLDCLK output clock.
TLDCLK	Tristate Output	D23	The transmit line data communication channel (DCC) clock (TLDCLK) is used to clock in the transmit line DCC (TLD). A smooth or gapped version of this clock may be selected. When selecting the smooth clock, TLDCLK is a 576 kHz clock with nominal 50% duty cycle. When selecting the gapped clock, TLDCLK is a 576 kHz clock, with nominal 66%/33% duty cycle, generated by gapping a 2.16 MHz clock. In all cases, TLD is sampled on the rising edge of TLDCLK. In gapped clock mode, a gap detector on TLDCLK is needed to identify the MSB on TLD. An edge detection on TFP may also be used. In smooth clock mode, TTOHFP may be used to identify the rising edge when the MSB should be present on TSLD. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TLDCLK output clock and the TLD_TS register bit that can be used to tri-state the TLDCLK output.

Pin Name	Type	Pin No.	Function
TLD	Input	C23	The transmit line DCC (TLD) bit serial input signal contains the line data communication channel (D4-D12) to be transmitted. TLD is sampled on the rising edge of TLDCLK. The TTOH and TTOHEN inputs take precedence over TLD. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TLDCLK output clock and the TLD_TS register bit that can be used to tri-state the TLDCLK output.
TOWCLK	Output	A24	The transmit order wire clock (TOWCLK) is used to clock in transmit section orderwire, user channel and line orderwire. (TSOW, TSUC and TLOW). A smooth or gapped version of this clock may be selected. When selecting the smooth clock, TOWCLK is a 64 kHz clock with nominal 50% duty cycle. When selecting the gapped clock, TOWCLK is a 64 kHz clock generated by gapping a 72 kHz clock. In all cases, TSOW, TSUC and TLOW are sampled on the rising edge of TOWCLK. In gapped clock mode, a gap detector on TOWCLK is needed to identify the MSB on TSOW, TSUC and TLOW. An edge detection on TFP may also be used. In smooth clock mode, TTOHFP may be used to identify the rising edge when the MSB should be present on TSOW, TSUC and TLOW. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TOWCLK output clock.

Pin Name	Type	Pin No.	Function
TSOW	Input	E23	The transmit section order wire (RSOW) bit serial input signal contains the section order wire (E1) to be transmitted. TSOW is sampled on the rising edge of TOWCLK. By default, the TOH input take precedence over TSOW. The TTOH and TTOHEN inputs has also precedence over TSOW. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TOWCLK output clock.
TSUC	Input	B24	The transmit section user channel (RSUC) bit serial input signal contains the user channel (F1) to be transmitted. TSUC is sampled on the rising edge of TOWCLK. The TOH and the TTOH and TTOHEN inputs take precedence over TSUC. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TOWCLK output clock.
TLOW	Input	C24	The transmit line order wire (TLOW) bit serial input signal contains the line order wire (E2) to be transmitted. TLOW is sampled on the rising edge of TOWCLK. The TOH and the TTOH and TTOHEN inputs take precedence over TLOW. The TTOC Overhead Control register contains the TX_GAPSEL register bit used to select the smooth or gapped TOWCLK output clock.

Pin Name	Type	Pin No.	Function
TOHCLK	Tristate Output	A25	The transmit overhead clock (TOHCLK) is used to clock in the transmit overhead (TOH). A smooth or gapped version of this clock may be selected. When selecting the smooth clock and clocking the section orderwire (E1), user channel (F1) or line order wire (E2), TOHCLK is a 64 kHz clock with nominal 50% duty cycle. When selecting to clock the line APS bytes (K1/K2), TOHCLK is a 128 kHz clock with nominal 50% duty cycle. When selecting the gapped clock and clocking the section orderwire (E1), user channel (F1) or line order wire (E2), TOHCLK is a 64 kHz clock generated by gapping a 72 kHz clock. When selecting to clock the line APS bytes (K1/K2), TOHCLK is a 128 kHz clock generated by gapping a 144 kHz clock. In all cases, TOH is sampled on the rising edge of TOHCLK. In gapped clock mode, a gap detector on TOHCLK is needed to identify the MSB on TOH. An edge detection on TFP may also be used. In smooth clock mode, TTOHFP may be used to identify the rising edge when the MSB should be present on TOH. The TTOC Overhead Control register contains the TOHSEL[1:0] register bits used to select the section orderwire, section user channel, line orderwire or line APS bytes. The same register also contains the TX_GAPSEL register bit used to select the smooth or gapped TOHCLK output clock and the TOH_TS register bit that can be used to tri-state the TOHCLK output.

Pin Name	Type	Pin No.	Function
TOH	Input	D24	The transmit overhead (TOH) bit serial input signal contains either the received section orderwire (E1), user channel (F1) line order wire (E2) or line APS bytes (K1/K2) to be transmitted. TOH is sampled on the rising edge of TOHCLK. The TOH inputs take precedence over the TSOW, TSUC or TLOW inputs and the TTOH and TTOHEN inputs take precedence over TOH. By default the TOH input will overwrite the TSOW input. The TTOC Overhead Control register contains the TOHSEL[1:0] register bits used to select the section orderwire, section user channel, line orderwire or line APS bytes. The same register also contains the TX_GAPSEL register bit used to select the smooth or gapped TOHCLK output clock and the TOH_TS register bit that can be used to tri-state the TOHCLK output.
TTOHCLK	Output	D25	The transmit transport overhead clock (TTOHCLK) is used to clock in transport overhead (TTOH) to be transmitted along with it's enable (TTOHEN). TTOHCLK is nominally a 20.736 MHz clock generated by gapping a 25.92 MHz clock. TTOHCLK has a 33% high duty cycle. TTOHFP is updated on the falling edge of TTOHCLK. TTOH is updated on the falling edge of TTOHCLK.
TTOH	Input	E24	The transmit transport overhead (TTOH) bit serial input signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and errors masks to be applied on the B1, B2, H1 and H2 transmitted bytes. TTOH is sampled on the rising edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHFP	Output	B25	The transmit transport overhead frame position (TTOHFP) signal is used to locate the most significant bit (MSB) on the TTOH serial stream. TTOHFP is set high when bit 1 (the most significant bit) of the first framing byte (A1) should be present on the TTOH stream. When the TX_GAPSEL register bit is set low in the TTOC Overhead Control register, TTOHFP can be sampled on the rising edges of TSLDCLK, TLDCLK, TOWCLK and TOHCLK to locate the MSB of the TSLD, TLD, TSOW, TSUC, TRLOW and TOH serial input streams. In this mode, the generation of these clocks are aligned with the generation of TTOHFP. TTOHFP is updated on the falling edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHEN	Input	C25	The transmit transport overhead insert enable (TTOHEN) signal controls the source of the transport overhead data which is inserted in the outgoing stream. When TTOHEN is high during the most significant bit of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). While TTOHEN is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. The overhead byte enabled by the TTOHEN input takes precedence over TOH input. When TTOHEN is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH, the sampled TOH byte is logically XOR'ed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH byte allows the incoming bit to go through while a bit set to logic high will toggle the incoming bit. A low level on TTOHEN during the MSB of the TOH byte disables the error forcing for the entire byte. When the transmit trace enable (TREN) bit in the TTOC Transport Overhead Byte Control register is a logic 1, the J0 byte contents are sourced from the section trace buffer, regardless of the state of TTOHEN. TTOHEN is sampled on the rising edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHREI	Input	A23	The transmit transport overhead REI (TTOHREI) serial input signal contains the REI count to be transmitted into the M1 byte. TTOHREI is sampled on the rising edge of TTOHCLK and increments an 8 bit counter for each TTOHREI sampled high. On the TTOHCLK rising edge identified by TTOHFP, the counter's value is transferred into a holding register and the counter reset to zero or one if the TTOHREI is sampled high during the cycle. This ensures that all TTOHREI pulses will be counted. The transferred count value is inserted into M1 byte. This input can be used when multiple SPECTRA-622's are configured to process a demultiplexed STS-48(STM16) stream. TTOHREI is sampled on the rising edge of TTOHCLK. The TTOH and TTOHEN inputs take precedence over TTOHREI.

10.7 Receive Path Status and Overhead Signal

Pin Name	Pin Type	PIN No.	Function
RPOHCLK	Output	E15	The receive path overhead clock (RPOHCLK) provides timing to process the B3E signal, the receive alarm port (RAD) and to sample the extracted path overhead for the twelve STS-1 (STM-0/AU3) streams or the four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. RPOHCLK is a nominally 12.96 MHz, 50% duty cycle clock. B3E, RALM, RPOH and RPOHFP are updated on the falling edge of the RPOHCLK signal. RAD is updated on the falling edge of RPOHCLK.

Pin Name	Pin Type	PIN No.	Function
RPOHFP	Output	D15	The receive path overhead frame position signal (RPOHFP) may be used to locate the individual path overhead bits of an STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) in the path overhead data stream on RPOH. RPOHFP signal is logic 1 when bit 1 (the most significant bit) of the path trace byte (J1) of the first STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) is present in the RPOH stream. RPOHFP may be used to locate the BIP error count and path RDI indication bits on the receive alarm port data signal (RAD). RPOHFP is logic 1 when the first of eight BIP error positions from the first STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) stream is present on the receive alarm data signal (RAD). RPOHFP signal is updated on the falling edge of the RPOHCLK signal.
RPOH	Output	B15	The receive path overhead data signal (RPOH) contains the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the path overhead of the twelve STS-1 (STM-0/AU3) streams or the four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. The corresponding RPOHEN signal is set high to identify the valid overhead bytes that are presented. RPOH is updated on the falling edge of RPOHCLK.

Pin Name	Pin Type	PIN No.	Function
RPOHEN	Output	C15	The receive path overhead enable signal (RPOHEN) indicates the validity of the path overhead bytes extracted to the RPOH from the path overhead of the twelve STS-1 (STM-0/AU3) streams or the four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. When RPOHEN signal is set high, the corresponding path overhead byte presented on the RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on the RPOH is invalid. RPOHEN is updated on the falling edge of RPOHCLK.
B3E	Output	A14	The bit interleaved parity error signal (B3E) carries the path BIP-8 error detected for each STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) and STS-12c (STM-4-4c) in the receive stream. It is set high for one RPOHCLK period for each path BIP-8 error detected (up to eight per frame) or when errors are treated on a block basis, is set high for only one RPOHCLK period if any of the path BIP-8 bits are in error. Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed BIP-8 for the previous frame. B3E is updated on the falling edge of RPOHCLK.
RALM	Output	A19	The Receive Alarm (RALM) signal is a multiplexed output of individual alarms of the receive STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) and STS-12c (STM-4-4c) streams. Each alarm represents the logical OR of the LOS/LOF/LAIS, LOP, PAIS, PRDI, PERDI, LOM, LOPCON, PAISCON, UNEQ, PSLU, PSLM, TIU-P, TIM-P status of the corresponding stream. The selection of alarms to be reported is controlled by the SPECTRA-622 RPPS RALM Output Control #1 and #2 registers. RALM is updated on the falling edge of RPOHCLK. • The LOS/LOF/LAIS signal indicates the loss of signal (LOS), loss of frame (LOF) or line AIS (LAIS) in the STS-12 (STM-4) SONET/SDH

Pin Name	Pin Type	PIN No.	Function
			stream. • The loss of pointer signal (LOP) indicates the loss of pointer state in the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. LOP is set high when invalid pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the stream. • The path alarm indication signal (PAIS) indicates the path AIS state of the corresponding STS-1 (STM-0/AU3)), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. PAIS is set high when an all ones pattern is observed in the pointer bytes (H1 and H2) for three consecutive frames in the stream. • The path remote defect indication signal (PRDI) indicates the path remote state of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. PRDI is set high when the path RDI alarm bit (bit 5) of the path status (G1) byte is set high for five or ten consecutive frames. The RDI10 bit in the RPOP Pointer MSB register controls whether five or ten consecutive frames will cause a PRDI indication. • The path enhanced remote defect indication signal (PERDI) indicates the path enhanced remote state of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. PERDI is set high when the path ERDI alarm code (bits 5,6,7) of the path status (G1) byte is set to the same alarm codepoint for five or ten consecutive frames. The RDI10 bit in the RPOP Pointer MSB register controls whether five or ten consecutive frames will cause a PRDI indication.

Pin Name	Pin Type	PIN No.	Function
			• The loss of multiframe signal (LOM) indicates the tributary multiframe synchronization status of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. LOM is set high if a correct four frame sequence is not detected in eight frames. • The loss of pointer concatenation and path AIS concatenation signals (LOPCON and PAISCON) are the concatenated alarms for STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. • The receive path unequipped status (UNEQ) indicates the unequipped status of the path signal label of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. UNEQ is set high when the filtered path signal label indicates unequipped and is dependent on the selected UNEQ mode. • The receive path signal label unstable status (PSLU) reports the stable/unstable status (mode 1) of the path signal label in the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. PSLU is set high when the current received C2 byte differs from the previous C2 byte for five consecutive frames. • The receive path signal label mismatch (PSLM) status reports the match/mismatch status (mode 1 and mode 2) for the path signal label of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. In mode 1, PSLM is set high when the accepted PSL differs from the expected PSL written by the microprocessor. In mode 2, PSLM is set high when 5 consecutive mismatches have been declared • The receive path trace identifier unstable status (TIU-P) reports the stable/unstable status

Pin Name	Pin Type	PIN No.	Function
			(mode 1 and mode 2) of the path trace identifier framer of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. In mode 1, TIU is set high when the current message differs from its immediate predecessor for eight consecutive frames. In mode 2, TIU is set high when three consecutive 16 byte windows of trace bytes are detected to have errors. TIU2 is set low when the same trace byte is received in forty-eight consecutive SONET/SDH frames. • The receive path trace identifier mismatch (TIM-P) status reports the match/mismatch status (mode 1) of the path identifier message framer of the corresponding STS-1 (STM-0/AU3), STS-3c (STM-1/AU4) or STS-12c (STM-4-4c) SONET/SDH stream. TIM-P is set high when the accepted identifier message differs from the expected message written by the microprocessor. Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm.
RSVD1	Input	A15	This pin must be connected to ground.
RSVD2	Input	A17	This pin must be connected to ground
RAD	Output	B26	The receive alarm port data signal (RAD) contains the path BIP error count and the path remote alarm indication status of the twelve receive STS-1 (STM-0/AU3) streams or the four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. RAD is updated on the falling edge of RPOHCLK.

10.8 Transmit Path Overhead Signals

Pin Name	Pin Type	PIN No.	Function
TPOHCLK	Output	B13	The transmit path overhead clock (TPOHCLK) provides timing for the path overhead stream. TPOHCLK is a nominally 12.96 MHz, 50% duty cycle clock. TPOH and TPOHEN are sampled on the rising edge of the TPOHCLK. TPOHFP is updated on falling edge of TPOHCLK. TPOHRDY is updated on rising edge of TPOHCLK.
TPOHFP	Output	E14	The path overhead frame position signal (TPOHFP) may be used to locate the individual path overhead bits in the overhead data stream, TPOH. TPOHFP is set high when bit 1 (the most significant bit) of the Path Trace byte (J1) of the first STS-1 (STM-0/AU3), STS-3c (STM-1/AU3) or STS-12c (STM-4-4c) shall be present in the TPOH stream. TPOHFP is updated on the falling edge of the TPOHCLK.
TPOH	Input	C14	The transmit path overhead data signal (TPOH) contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) and error mask for the B3 and H4 bytes. The overhead bytes may be inserted into the path overhead byte positions in the twelve STS-1 (STM-0/AU3) streams or the four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. The error masks may be used to insert path BIP and multiframe sequence bit errors into the outgoing streams. A path overhead byte is accepted for transmission when the external source indicates a valid byte (TPOHEN set high) and the SPECTRA-622 indicates ready (TPOHRDY set high). The SPECTRA-622 will ignore the byte on TPOH when TPOHEN is set low. The TPOHRDY is set low to indicate SPECTRA-622 is not ready, and the byte must be re-presented at the next opportunity. TPOH is sampled on the rising edge of the TPOHCLK output.

Pin Name	Pin Type	PIN No.	Function
TPOHEN	Input	D14	The transmit path overhead insert enable signal (TPOHEN) indicates the availability of a valid path overhead byte on TPOH. TPOHEN shall be set high during the most significant bit of a TPOH byte to indicate valid data on the TPOH input. This byte will be accepted for transmission if TPOHRDY is also set high. If TPOHRDY is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on the TPOH input are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH is ignored when TPOHEN is set low during the most significant bit position. The TPOHEN input takes precedence over TAD. When the byte at the B3 or H4 byte position on TPOH is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XOR'ed with the corresponding B3 or H4 byte before it is transmitted. TPOHEN is sampled on the rising edge of the TPOHCLK.

Pin Name	Pin Type	PIN No.	Function
TPOHRDY	Output	B14	The transmit path overhead insert ready signal (TPOHRDY) indicates whether the SPECTRA-622 is ready to accept the byte currently on TPOH. TPOHRDY is set high during the most significant bit of a TPOH byte to indicate readiness to accept the byte on the TPOH input. This byte will be accepted if TPOHEN is also set high. If TPOHEN is set low, the byte is invalid and is ignored. TPOHRDY is set low to indicate that the SPECTRA-622 is unable to accept the byte on TPOH, and expects the byte to be re-presented at the next opportunity. Accepted bytes sampled on the TPOH input are inserted or masked into the corresponding path overhead byte positions (for the J1, *B3*, C2, G1, F2, *H4*, Z3, Z4, and Z5 bytes). TPOHRDY is updated on the rising edge of the TPOHCLK.
TAD	Input	E25	The transmit alarm port data signal (TAD) contains the path REI count and the path RDI status of the twelve receive STS-1 (STM-0/AU3) streams or four STS-3/3c (STM-1/AU3/AU4) streams or the single STS-12c (STM-4-4c) stream. In addition, the TAD input can contain the K1 and K2 bytes. TTOHEN takes precedence over TAD. TAD is sampled on the rising edge of TACK.
TAFP	Input	C26	The transmit alarm port frame pulse signal (TAFP) marks the first bit of the transmit alarm message in each SONET/SDH frame. TAFP is pulsed high to mark the first path REI bit location of the first STS-1 (STM-0/AU3) stream or the first path REI bit location of the first STS-3c (STM-1/AU4) stream or the first path REI bit location of the single STS-12c (STM-4-4c) stream. TAFP is sampled on the rising edge of TACK.

Pin Name	Pin Type	PIN No.	Function
TACK	Input	B27	The transmit alarm port clock (TACK) provides timing for transmit alarm port. TACK is nominally a 12.96 MHz, 50% duty cycle clock. Inputs TAD and TAFP are sampled on the rising edge of TACK.

10.9 Drop and Transmit Path AIS Control Signals

Pin Name	Pin Type	PIN No.	Function
DPAISCK	Input	B12	The DROP bus path alarm indication clock signal (DPAISCK) provides timing for system DROP side path or DS3 AIS assertion. DPAISCK is a clock of arbitrary phase and frequency within the limits specified in the A.C. Timing section of this document. Inputs DPAIS and DPAISFP are sampled on the rising edge of DPAISCK.
DPAISFP	Input	A12	The active high DROP bus path alarm indication frame pulse signal (DPAISFP) marks the first path or DS3 AIS assertion request for the DROP bus SONET/SDH streams. DPAISFP is set high to mark the path or DS3 AIS assertion request of the first DROP bus STS-1 (STM-0/AU3) stream. It also marks the path AIS assertion request of the first DROP bus STS-3c (STM-1/AU4) stream or the single DROP bus STS-12c (STM-4-4c) stream. DPAISFP is sampled on the rising edge of DPAISCK.

Pin Name	Pin Type	PIN No.	Function
DPAIS	Input	A13	The active high DROP bus path alarm indication signal (DPAIS) is a timeslot multiplexed signal that controls the insertion of path or DS3 AIS in the DROP bus (DD[31:24], DD[23:16], DD[15:8], DD[7:0]) and the DS3 DROP interface (DS3RDAT[12:1]) on a per STS (AU) basis. A high level on DPAIS during a specific timeslot forces the insertion of the all ones pattern into the corresponding SPE and the payload pointer bytes (H1, H2, and H3) presented on the DROP bus. A DS3 AIS is simultaneously inserted in the corresponding DS3 DROP interface. Path AIS or DS3 AIS can also be inserted via register access or in response to receive alarms. DPAIS is sampled on the rising edge of DPAISCK.
TPAISCK	Input	E13	The Transmit path alarm indication clock signal (TPAISCK) provides timing for system ADD side path or DS3 AIS assertion. TPAISCK is a clock of arbitrary phase and frequency within the limits specified in the A.C. Timing section of this document. Inputs TPAIS and TPAISFP are sampled on the rising edge of TPAISCK.
TPAISFP	Input	D13	The active high Transmit path alarm indication frame pulse signal (TPAISFP) marks the first path or DS3 AIS assertion request for the transmit SONET/SDH streams. TPAISFP is set high to mark the path or DS3 AIS assertion request of the first transmit STS-1 (STM-0/AU3) stream. It also marks the path AIS assertion request of the first transmit STS-3c (STM-1/AU4) stream or the single transmit STS-12c (STM-4-4c) stream. TPAISFP is sampled on the rising edge of TPAISCK.

Pin Name	Pin Type	PIN No.	Function
TPAIS	Input	C13	The active high Transmit path alarm indication signal (TPAIS) is a timeslot multiplexed signal that controls the insertion of path or DS3 AIS in the transmit stream on a per STS (AU) basis. A high level on TPAIS during one of the timeslots forces the insertion of the all ones pattern into the corresponding SPE and the payload pointer bytes (H1, H2, and H3). However, if the SPE carries a DS3 stream, as configured by the SPECTRA-622 TPPS Path and DS3 Configuration register, then a DS3 AIS is inserted instead of a path AIS. Path AIS insertion can also be inserted via register access or in response to ADD bus path alarms. Similarly, DS3 AIS insertion can be performed via register access. TPAIS is sampled on the rising edge of TPAISCK.

10.10 Drop Bus Interface Configuration

Pin Name	Pin Type	PIN No.	Function
DMODE[0] DMODE[1]	Input	AG26 AH27	The DROP bus mode select (DMODE[1:0]) inputs are used to select the operation of the DROP Bus system side interface when the DMODE[1:0] bits in the SPECTRA-622 Drop Bus Configuration register is set to 00b. The interface may be configured as Telecom mode only, DS3 mode only or Dual Telecom and DS3 mode. In Telecom mode, only the Telecom DROP bus interface is active. The DROP DS3 blocks are held in reset and the DS3 interface output signals are forced low. In DS3 mode, only the DS3 DROP bus interface is active. The DS3 Telecom blocks are held in reset and the Telecom interface output signals are forced low. In Dual mode, both the DROP Telecom and DS3 interfaces are enabled and all DROP blocks are functioning. The DROP bus mode may also be set via the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register. The DMODE[1:0] register bits override the mode set via the input pins when the register bits are programmed to other than 00b. By default the input pins are used to set the DROP bus mode. DMODE[1:0] = 01b: Telecom Mode DMODE[1:0] = 10b: DS3 Mode DMODE[1:0] = 11b: Dual Mode DMODE[1:0] = 00b: Reserved

10.11 Drop Bus Telecom Interface Signals

Pin Name	Pin Type	PIN No.	Function
DCK	Input	AH30	The DROP bus clock (DCK) provides timing for the DROP bus interface. DCK is nominally a 77.76 MHz, 50% duty cycle clock when the drop interface is configured as a single STS-12 (STM-4) interface. DCK is nominally a 19.44 MHz, 50% duty cycle clock when the drop interface is configured as a quad STS-3 (STM-1) interface. Frequency offsets between line side clock (or divided by 4 version of) and DCK are accommodated by pointer justification events on the DROP bus. DFP is sampled on the rising edge of DCK. Outputs DPL[4:1], DC1J1V1[4:1], DDP[4:1] and DD[31:0] are updated on the rising edge of DCK when used. An internal DLL insure proper timing for the 77.76 MHz configuration. The clock need to be stable after the reset, else it might need to be reseted by register A6H
DFP	Input	AG29	The active high DROP bus reference frame position signal (DFP) indicates when the first byte of the synchronous payload envelope (SPE byte #1) is available on the DD[7:0], DD[15:8], DD[23:16] and DD[31:24] busses. For the single bus STS-12(STM-4) interface the first SPE byte of STS-1 #1 is identified. For the quad bus STS-3 (STM-1) interface the first SPE byte of STS-1 #1 on the four output buses identified. Note that DFP has a fixed relationship to the SONET/SDH frame; the start of payload is determined by the STS (AU) pointer and may change relative to DFP. The SPECTRA-622 will flywheel in the absence of a DFP pulse. If the DFP aligment changes, all the slices are resynchronized and the DPGMs need to be manually regen if used. DFP is sampled on the rising edge of DCK.

Pin Name	Pin Type	PIN No.	Function
DD[0] DD[1] DD[2] DD[3] DD[4] DD[5] DD[6] DD[7]	Output	H29 H28 H27 J31 J30 J29 J28 J27	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[7:0]) contains the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) received SONET/SDH payload data. In quad DROP bus interface STS-3(STM-1) mode, the DROP bus data (DD[7:0]) contains the first STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data. When the DROP bus TSI functionality is disabled, the dropped payload multiplexing corresponds to that of the received SONET/SDH data. TSI may be used to reorder this multiplexing on the drop bus. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[7:0] is updated on the rising edge of DCK. These outputs are forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DD[8] DD[9] DD[10] DD[11] DD[12] DD[13] DD[14] DD[15]	Output	N29 N28 N27 P31 P30 P29 P28 P27	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[15:8]) is forced low. In quad DROP bus interface STS-3(STM-1) mode, the DROP bus data (DD[15:8]) contains the second STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data. When the DROP bus TSI functionality is disabled, the dropped payload corresponds to the STS-3(STM-1) #2 of the received SONET/SDH data. TSI may be used to reorder this multiplexing on the drop bus. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[15] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[8] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[15:8] is updated on the rising edge of DCK. These outputs are forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DD[16] DD[17] DD[18] DD[19] DD[20] DD[21] DD[22] DD[23]	Output	W27 Y31 Y30 Y29 Y28 Y27 AA30 AA29	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[23:16]) is forced low. In quad bus interface STS-3(STM-1) mode, the DROP bus data (DD[15:8]) contains the third TS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data. When the DROP bus TSI functionality is disabled, the dropped payload corresponds to the STS-3(STM-1) #3 of the received SONET/SDH data. TSI may be used to reorder this multiplexing on the drop bus. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[23] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[16] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[23:16] is updated on the rising edge of DCK. These outputs are forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DD[24] DD[25] DD[26] DD[27] DD[28] DD[29] DD[30] DD[31]	Output	AE31 AE30 AE29 AE28 AE27 AF30 AF29 AG31	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[31:24]) is forced low. In quad bus interface STS-3(STM-1) mode, the DROP bus data (DD[31:24]) contains the fourth STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data. When the DROP bus TSI functionality is disabled, the dropped payload corresponds to the STS-3(STM-1) #4 of the received SONET/SDH data. TSI may be used to reorder this multiplexing on the drop bus. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[31] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[24] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[31:24] is updated on the rising edge of DCK. These outputs are forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DPL[1]	Output	H31	The active high DROP bus payload active signal #1 (DPL[1]) indicates when the DD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[1] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[1] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DPL[2]	Output	N31	The active high DROP bus payload active signal #2 (DPL[2]) indicates when the DD[15:8] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[2] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[2] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DPL[3]	Output	W29	The active high DROP bus payload active signal #3 (DPL[3]) indicates when the DD[23:16] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[3] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[3] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DPL[4]	Output	AD28	The active high DROP bus payload active signal #4 (DPL[4]) indicates when the DD[31:24] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[4] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[4] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DC1J1V1[1]	Output	H30	The DROP bus composite timing signal #1 (DC1J1V1[1]) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus signals DD[7:0]. DC1J1V1[1] pulses high with the DROP bus payload active signal (DPL[1]) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[1] pulses high with DPL[1] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[1] signal pulses high on the V1 byte to indicate tributary multiframe boundaries using the ENDV1 bit in the SPECTRA-622 RPPS Path/DS-3 Configuration register. DC1J1V1[1] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DC1J1V1[2]	Output	N30	The DROP bus composite timing signal #2 (DC1J1V1[2]) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus signals DD[15:8]. DC1J1V1[2] pulses high with the DROP bus payload active signal (DPL[2]) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[2] pulses high with DPL[2] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[2] signal pulses high on the V1 byte to indicate tributary multiframe boundaries using the ENDV1 bit in the SPECTRA-622 RPPS Path/DS-3 Configuration register. DC1J1V1[2] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DC1J1V1[3]	Output	W28	The DROP bus composite timing signal #3 (DC1J1V1[3]) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus signals DD[23:16]. DC1J1V1[3] pulses high with the DROP bus payload active signal (DPL[3]) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[3] pulses high with DPL[3] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[3] signal pulses high on the V1 byte to indicate tributary multiframe boundaries using the ENDV1 bit in the SPECTRA-622 RPPS Path/DS-3 Configuration register. DC1J1V1[3] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DC1J1V1[4]	Output	AD27	The DROP bus composite timing signal #4 (DC1J1V1[4]) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus signals DD[31:24]. DC1J1V1[4] pulses high with the DROP bus payload active signal (DPL[4]) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[4] pulses high with DPL[4] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[4] signal pulses high on the V1 byte to indicate tributary multiframe boundaries using the ENDV1 bit in the SPECTRA-622 RPPS Path/DS-3 Configuration register. DC1J1V1[4] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DDP[1]	Output	K31	The DROP bus data parity signal #1 (DDP[1]) indicates the parity of the DROP bus signals. The DROP data bus signals (DD[7:0]) are always included in parity calculations. Register bits in the SPECTRA-622 DROP Bus Configuration register control the inclusion of the DPL[1] and DC1J1V1[1] signals in parity calculation and the sense (odd/even) of the parity. DDP[1] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DDP[2]	Output	R28	The DROP bus data parity signal #2 (DDP[2]) indicates the parity of the DROP bus signals. The DROP data bus signals (DD[15:8]) are always included in parity calculations. Register bits in the SPECTRA-622 DROP Bus Configuration register control the inclusion of the DPL[2] and DC1J1V1[2] signals in parity calculation and the sense (odd/even) of the parity. DDP[2] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

Pin Name	Pin Type	PIN No.	Function
DDP[3]	Output	AA28	The DROP bus data parity signal #3 (DDP[3]) indicates the parity of the DROP bus signals. The DROP data bus signals (DD[23:16]) are always included in parity calculations. Register bits in the SPECTRA-622 DROP Bus Configuration register control the inclusion of the DPL[3] and DC1J1V1[3] signals in parity calculation and the sense (odd/even) of the parity. DDP[3] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.
DDP[4]	Output	AF28	The DROP bus data parity signal #4 (DDP[4]) indicates the parity of the DROP bus signals. The DROP data bus signals (DD[31:24]) are always included in parity calculations. Register bits in the SPECTRA-622 DROP Bus Configuration register control the inclusion of the DPL[4] and DC1J1V1[4] signals in parity calculation and the sense (odd/even) of the parity. DDP[4] is updated on the rising edge of DCK. This output is forced low in DROP DS3 interface mode and STS-12/STM-4 parallel mode. The DROP interface mode is set via the DMODE[1:0] input pins or the DMODE[1:0] register bits in the SPECTRA-622 DROP Bus Configuration register.

10.12 Add Bus Telecom Interface Signals

Pin Name	Pin Type	PIN No.	Function
ACK	Input	E31	The ADD bus clock (ACK) provides timing for the ADD bus interface. ACK is nominally a 77.76 MHz, 50% duty cycle clock when the add interface is configured as a single STS-12 (STM-4) interface. ACK is nominally a 19.44 MHz, 50% duty cycle clock when the add interface is configured as a quad STS-3 (STM-1) interface. Inputs AD[31:0], APL[4:1], ADP[4:1], and AC1J1V1[4:1]/AFP[4:1] are sampled on the rising edge of ACK.
AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7]	Input	E28 F30 F29 F28 F27 G31 G30 G29	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[7:0]) contains the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) SONET/SDH payload data to transmit. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[7:0]) contains the 1st STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit. When ADD bus TSI functionality is enabled, the association of ADD bus payloads to the transmitted payloads is software configurable in the SPECTRA-622 ADD Bus STM-1 #1..4 AU3 #1..3 Select registers. The transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1[1]) or optionally by interpreting the H1 and H2 pointer bytes. AD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[7:0] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15]	Input	K28 K27 L30 L29 L28 M31 M30 M29	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[15:8]) is disabled. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[15:8]) contains the 2nd STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit. When ADD bus TSI functionality is enabled, the association of ADD bus payloads to the transmitted payloads is software configurable in the SPECTRA-622 ADD Bus STM-1 #1..4 AU3 #1..3 Select registers. The transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1[2]) or optionally by interpreting the H1 and H2 pointer bytes. AD[15] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[8] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[15:8] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23]	Input	U29 U28 U27 V31 V30 V29 V28 V27	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[23:16]) is disabled. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[23:16]) contains the 3rd STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit. When ADD bus TSI functionality is enabled, the association of ADD bus payloads to the transmitted payloads is software configurable in the SPECTRA-622 ADD Bus STM-1 #1..4 AU3 #1..3 Select registers. The transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1[3]) or optionally by interpreting the H1 and H2 pointer bytes. AD[23] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[16] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[23:16] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	Input	AB29 AB28 AB27 AC31 AC30 AC29 AC28 AD31	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[31:24]) is disabled. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[31:24]) contains the 4th STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit. When ADD bus TSI functionality is enabled, the association of ADD bus payloads to the transmitted payloads is software configurable in the SPECTRA-622 ADD Bus STM-1 #1..4 AU3 #1..3 Select registers. The transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1[4]) or optionally by interpreting the H1 and H2 pointer bytes. AD[31] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[24] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[31:24] is sampled on the rising edge of ACK.
APL[1]	Input	E30	The ADD bus payload active signal #1 (APL[1]) indicates when AD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[1] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[1] input must be strapped low when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. APL[1] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
APL[2]	Input	K30	The ADD bus payload active signal #2 (APL[2]) indicates when AD[15:8] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[2] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[2] input must be strapped low when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. APL[2] is sampled on the rising edge of ACK.
APL[3]	Input	U31	The ADD bus payload active signal #3 (APL[3]) indicates when AD[23:16] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[3] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[3] input must be strapped low when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. APL[3] is sampled on the rising edge of ACK.
APL[4]	Input	AB31	The ADD bus payload active signal #4 (APL[4]) indicates when AD[31:24] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[4] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[4] input must be strapped low when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. APL[4] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AC1J1V1[1] /	Input	E29	The ADD bus composite timing signal #1 (AC1J1V1[1]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set low. AC1J1V1[1] identifies the frame and optionally the payload and tributary multiframe boundaries on the ADD data bus signals AD[7:0]. AC1J1V1[1] pulses high with the ADD bus payload active signal #1 (APL[1]) set low to mark the first STS-1 (STM-0/AU3) Identification byte (C1). Optionally, the AC1J1V1[1] pulses high with APL[1] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[1] signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus signals (AD[7:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus signals (AD[7:0]) to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the C1 pulses of the associated AC1J1V1 signals. All C1 pulses must be aligned. If the AC1J1V1[1] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. The ATSI_ISOLATE bit can be used to disable the realignment of the 12 TPPS slice clocks by AC1J1V1/AFP[1] ADD BUS. This bit should only be used when all 12 TPPS slices are placed in Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) ADD BUS interface can not maintain a constant frame alignment. AC1J1V1[1] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AFP[1]			The active high ADD bus reference frame position signal #1 (AFP[1]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. AFP[1] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[7:0] bus. Note that AFP[1] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[1]. The DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register must be set high in this mode to enable pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[7:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the AFP pulses of the associated AC1J1V1/AFP signals. All AFP pulses must be aligned. If the AFP[1] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. The ATSI_ISOLATE bit can be used to disable the realignment of the 12 TPPS slice clocks by AC1J1V1/AFP[1] ADD BUS. This bit should only be used when all 12 TPPS slices are placed in Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) ADD BUS interface can not maintain a constant frame alignment. AFP[1] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AC1J1V1[2] /	Input	K29	The ADD bus composite timing signal #2 (AC1J1V1[2]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set low. AC1J1V1[2] identifies the frame and optionally the payload and tributary multiframe boundaries on the ADD data bus signals AD[15:8]. AC1J1V1[2] pulses high with the ADD bus payload active signal #2 (APL[2]) set low to mark the first STS-1 (STM-0/AU3) Identification byte (C1). Optionally, the AC1J1V1[2] pulses high with APL[2] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[2] signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus signals (AD[15:8]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus signals (AD[15:8]) to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the C1 pulses of the associated AC1J1V1. All C1 pulses must be aligned. If the AC1J1V1[2] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AC1J1V1[2] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AFP[2]			The active high ADD bus reference frame position signal #2 (AFP[2]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. AFP[2] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[15:8] bus. Note that AFP[2] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[2]. The DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register must be set high in this mode to enable pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[15:8]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the AFP pulses of the associated AC1J1V1/AFP signal. All AFP pulses must be aligned If the AFP[2] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AFP[2] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AC1J1V1[3] /	Input	U30	The ADD bus composite timing signal #3 (AC1J1V1[3]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set low. AC1J1V1[3] identifies the frame and optionally the payload and tributary multiframe boundaries on the ADD data bus signals AD[23:16]. AC1J1V1[3] pulses high with the ADD bus payload active signal #3 (APL[3]) set low to mark the first STS-1 (STM-0/AU3) Identification byte (C1). Optionally, the AC1J1V1[3] pulses high with APL[3] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[3] signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus signals (AD[23:16]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus signals (AD[23:16]) to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the C1 pulses of the associated AC1J1V1 signals. All C1 pulses must be aligned. If the AC1J1V1[3] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AC1J1V1[3] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AFP[3]			The active high ADD bus reference frame position signal #3 (AFP[3]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. AFP[3] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[31:24] bus. Note that AFP[3] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[3]. The DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register must be set high in this mode to enable pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[23:16]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned withthe AFP pulses of the associated AC1J1V1/AFP signals. All AFP pulses must be aligned. If the AFP[3] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AFP[3] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AC1J1V1[4] /	Input	AB30	The ADD bus composite timing signal #4 (AC1J1V1[4]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set low. AC1J1V1[4] identifies the frame and optionally the payload and tributary multiframe boundaries on the ADD data bus signals AD[31:24]. AC1J1V1[4] pulses high with the ADD bus payload active signal #4 (APL[1]) set low to mark the first STS-1 (STM-0/AU3) Identification byte (C1). Optionally, the AC1J1V1[4] pulses high with APL[4] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[4] signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus signals (AD[31:24]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus signals (AD[31:24]) to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the C1 pulses of the associated AC1J1V1 signals. All C1 pulses must be aligned. If the AC1J1V1[4] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AC1J1V1[4] is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AFP[4]			The active high ADD bus reference frame position signal #4 (AFP[4]) is defined when the AFPEN bit in SPECTRA-622 Add Bus Configuration is set high. AFP[4] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[31:24] bus. Note that AFP[4] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[4]. The DISJ1V1 bit in the SPECTRA-622 TPPS Path/DS3 Configuration register must be set high in this mode to enable pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[31:24]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] ADD buses must be frame aligned with the AFP pulses of the associated AC1J1V1/AFP signals. All AFP pulses must be aligned. If the AFP[4] aligment changes, all the slices are resynchronized and the APGMs need to be manually regen if used. AFP[4] is sampled on the rising edge of ACK.
ADP[1]	Input	G28	The ADD bus data parity signal #1 (ADP[1]) indicates the parity of the ADD bus #1 signals. The ADD data bus (AD[7:0]) is always included in parity calculations. Register bits in the SPECTRA-622 ADD Bus Configuration register control the inclusion of the APL[1] and AC1J1V1[1]/AFP[1] signals in parity calculations and the sense (odd/even) of the parity. ADP[1] is sampled on the rising edge of ACK. ADP[1] should not be tied high or low, this would prevent the detection of activity by the bit ACA1 (reg 1037H)

Pin Name	Pin Type	PIN No.	Function
ADP[2]	Input	M28	The ADD bus data parity signal #2 (ADP[2]) indicates the parity of the ADD bus #2 signals. The ADD data bus (AD[15:8]) is always included in parity calculations. Register bits in the SPECTRA-622 ADD Bus Configuration register control the inclusion of the APL[2] and AC1J1V1[2]/AFP[2] signals in parity calculations and the sense (odd/even) of the parity. ADP[2] is sampled on the rising edge of ACK. ADP[2] should not be tied high or low, this would prevent the detection of activity by the bit ACA2 (reg 1037H)
ADP[3]	Input	W31	The ADD bus data parity signal #3 (ADP[3]) indicates the parity of the ADD bus #3 signals. The ADD data bus (AD[23:16]) is always included in parity calculations. Register bits in the SPECTRA-622 ADD Bus Configuration register control the inclusion of the APL[3] and AC1J1V1[3]/AFP[3] signals in parity calculations and the sense (odd/even) of the parity. ADP[3] is sampled on the rising edge of ACK. ADP[3] should not be tied high or low, this would prevent the detection of activity by the bit ACA3 (reg 1037H)
ADP[4]	Input	AD30	The ADD bus data parity signal #4 (ADP[4]) indicates the parity of the ADD bus #4 signals. The ADD data bus (AD[31:24]) is always included in parity calculations. Register bits in the SPECTRA-622 ADD Bus Configuration register control the inclusion of the APL[4] and AC1J1V1[4]/AFP[4] signals in parity calculations and the sense (odd/even) of the parity. ADP[4] is sampled on the rising edge of ACK. ADP[4] should not be tied high or low, this would prevent the detection of activity by the bit ACA4 (reg 1037H)

10.13 DS3 System Side Interface

Pin Name	Type	Pin No.	Function
DS3RICLK	Input	AL27	The DS3 receive input clock (DS3RICLK) provides timing for the receive DS3 interface. It is a nominally 44.928 MHz, 50% duty cycle clock. DS3RICLK is gapped to generate the DS3 receive output clocks (DS3ROCLK[12:1]).
DS3ROCLK[1] DS3ROCLK[2] DS3ROCLK[3] DS3ROCLK[4] DS3ROCLK[5] DS3ROCLK[6] DS3ROCLK[7] DS3ROCLK[8] DS3ROCLK[9] DS3ROCLK[10] DS3ROCLK[11] DS3ROCLK[12]	Output	AK11 AJ11 AH11 AH12 AK17 AJ17 AH17 AG17 AL22 AK22 AJ22 AL23	The DS3 receive output clocks (DS3ROCLK[12:1]) provide timing to the DS3 received streams that have been de-mapped from the receive SONET/SDH stream. DS3ROCLK[n] is nominally 44.736 MHz. The de-mapped DS3 receive stream is clocked out on the DS3RDAT[n]. DS3ROCLK[n] is generated by gapping DS3RICLK when the DS3_SEL52 bit in the corresponding SPECTRA-622 RPPS Path and DS3 Configuration register is set low. DS3ROCLK[n] is generated by gapping an internal 51.84 MHz clock when the DS3_SEL52 bit is set high, in this mode, the REFCLK signal is required. DS3RDAT[n] is updated on the falling edge of DS3ROCLK[n].

Pin Name	Type	Pin No.	Function
DS3RDAT[1] DS3RDAT[2] DS3RDAT[3] DS3RDAT[4] DS3RDAT[5] DS3RDAT[6] DS3RDAT[7] DS3RDAT[8] DS3RDAT[9] DS3RDAT[10] DS3RDAT[11] DS3RDAT[12]	Output	AL12 AK12 AJ12 AG12 AG18 AH18 AJ18 AK18 AK23 AJ23 AH23 AG22	The DS3 receive data (DS3RDAT[12:1]) output signals contain NRZ encoded data of the DS3 streams that have been de-mapped from the receive SONET/SDH stream. The association of DS3 streams to the receive SONET/SDH payload streams are: DS3RDAT[1] STM-1 #1, AU3 #1 DS3RDAT[2] STM-1 #2, AU3 #1 DS3RDAT[3] STM-1 #3, AU3 #1 DS3RDAT[4] STM-1 #4, AU3 #1 DS3RDAT[5] STM-1 #1, AU3 #2 DS3RDAT[6] STM-1 #2, AU3 #2 DS3RDAT[7] STM-1 #3, AU3 #2 DS3RDAT[8] STM-1 #4, AU3 #2 DS3RDAT[9] STM-1 #1, AU3 #3 DS3RDAT[10] STM-1 #2, AU3 #3 DS3RDAT[11] STM-1 #3, AU3 #3 DS3RDAT[12] STM-1 #4, AU3 #3 DS3RDAT[n] is updated on the falling edge of DS3ROCLK[n].
DS3TICLK[1] DS3TICLK[2] DS3TICLK[3] DS3TICLK[4] DS3TICLK[5] DS3TICLK[6] DS3TICLK[7] DS3TICLK[8] DS3TICLK[9] DS3TICLK[10] DS3TICLK[11] DS3TICLK[12]	Input	AK13 AJ13 AG14 AJ14 AL19 AK19 AH19 AL20 AK24 AJ24 AL25 AK25	The DS3 transmit input clocks (DS3TICLK[12:1]) provide timing for the transmit DS3 data streams. DS3TICLK[n] is a nominally 44.736 MHz input clock. DS3TDAT[n] is sampled using the rising or falling edge of DS3TICLK[n] as selected using the DS3TICLKB bit in the SPECTRA-622 TPPS Path and DS3 Configuration register.

Pin Name	Type	Pin No.	Function
DS3TDAT[1] DS3TDAT[2] DS3TDAT[3] DS3TDAT[4] DS3TDAT[5] DS3TDAT[6] DS3TDAT[7] DS3TDAT[8] DS3TDAT[9] DS3TDAT[10] DS3TDAT[11] DS3TDAT[12]	Input	AL15 AK15 AH15 AG15 AH20 AK21 AJ21 AH21 AJ26 AH26 AK27 AJ27	The DS3 transmit data (DS3TDAT[12:1]) signals contain the DS3 or payload streams to be mapped into the SONET/SDH transmit streams when the corresponding DS3ADDSEL bit in the SPECTRA-622 TPPS Path and DS-3 Configuration register is set high. The association of DS3 streams to the transmit SONET/SDH payload streams are: DS3TDAT[1] STM-1 #1, AU3 #1 DS3TDAT[2] STM-1 #2, AU3 #1 DS3TDAT[3] STM-1 #3, AU3 #1 DS3TDAT[4] STM-1 #4, AU3 #1 DS3TDAT[5] STM-1 #1, AU3 #2 DS3TDAT[6] STM-1 #2, AU3 #2 DS3TDAT[7] STM-1 #3, AU3 #2 DS3TDAT[8] STM-1 #4, AU3 #2 DS3TDAT[9] STM-1 #1, AU3 #3 DS3TDAT[10] STM-1 #2, AU3 #3 DS3TDAT[11] STM-1 #3, AU3 #3 DS3TDAT[12] STM-1 #4, AU3 #3 DS3TDAT[n] is sampled using the rising or falling edge of DS3TICLK[n] as selected using the DS3TICLKB bit in the corresponding SPECTRA-622 TPPS Path and DS3 Configuration register.

10.14 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
MBEB	Input	E7	The active low Motorola bus enable (MBEB) signal configures the SPECTRA-622 for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the SPECTRA-622 is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
CSB	Input	C7	The active low chip select (CSB) signal is low during SPECTRA-622 register accesses. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB/ E	Input	B6	The active low read enable (RDB) signal is low during a SPECTRA-622 read access. The SPECTRA-622 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. The active high external access signal (E) is set high during SPECTRA-622 register access while in Motorola bus mode.
WRB/ RWB	Input	C6	The active low write strobe (WRB) signal is low during a SPECTRA-622 register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select signal (RWB) selects between SPECTRA-622 register read and write accesses while in Motorola bus mode. The SPECTRA-622 drives the data bus D[7:0] with the contents of the addressed register while CSB is low and RWB and E are high. The contents of D[7:0] are clocked into the addressed register on the falling E edge while CSB and RWB are low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	C12 D12 E12 B11 C11 D11 A10 B10	The bi-directional data bus, D[7:0], is used during SPECTRA-622 read and write accesses.

Pin Name	Type	Pin No.	Function
A[13]	Input	D10	The test register select signal (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS may be tied low.
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	E10 A9 B9 C9 D9 E9 A8 B8 C8 D8 E8 A7 B7	The address bus (A[12:0]) selects specific registers during SPECTRA-622 register accesses.
RSTB	Schmidt TTL Input	D6	The active low reset (RSTB) signal provides an asynchronous SPECTRA-622 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input	D7	The address latch enable (ALE) is an active-high signal and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the SPECTRA-622 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	C10	The active low interrupt (INTB) is set low when a SPECTRA-622 enabled interrupt source is active. The SPECTRA-622 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

10.15 Analog Miscellaneous Signals

Pin Name	Type	Pin No.	Function
TDREF0 TDREF1	Analog	N1 P5	The transmit data reference (TDREF0 and TDREF1) analog pins are provided to create calibrated currents for the PECL output transceivers TXD+/-. A 2 Kohm, 1% resistor is connected across TDREF0 and TDREF1 pins.
C0 C1	Analog	V2 V1	The analog C0 and C1 pins are provided to optimize the SPECTRA-622 for jitter transfer applications. To optimize the SPECTRA-622 for jitter transfer applications, a 47 nF non-polarized capacitor must be attached across C0 and C1 and the RTYPE bit in the CRSI Control register must be set to logic one. To optimize the SPECTRA-622 for jitter tolerance applications (if jitter transfer is not needed), the C0 and C1 pins must not be connected and the RTYPE bit in the CRSI Control register must be set to logic zero.
ATP[0] ATP[1]	Analog	L3 L2	Two analog test ports (ATP0, ATP1) are provided for production testing only. These pins must be tied to analog ground (AVS) during normal operation.
PREFEN	Input	G3	The differential PECL reference enable (PREFEN) allows the bias voltage of the PECL outputs to be controlled by the PECLREF input. When PREFEN is set high, the bias voltage of the PECL outputs is set by the PECLREF input. When PREFEN is set low, the PECLREF input is ignored and the bias voltage is set by the internal bandgap generator. This PIN should be tied to ground (VSS) during normal operation.
PECLREF	Analog	R2	The differential PECL reference (PECLREF) sets the bias voltage of the PECL output logic. When PREFEN is set high, the PECLREF voltage controls the bias voltage of the PECL outputs. When PREFEN is set low, the PECLREF input is ignored and the bias voltage is set by the internal bandgap generator. This PIN should be tied to analog ground (AVS) during normal operation.

10.16 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Input	B4	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	D5	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	B5	When the SPECTRA-622 is configured for JTAG operation, the test data input (TDI) signal carries test data into the SPECTRA-622 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	C5	The test data output (TDO) signal carries test data out of the SPECTRA-622 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input	A5	The active low test reset (TRSTB) signal provides an asynchronous SPECTRA-622 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

10.17 Power and Ground

Pin Name	Pin Type	PIN No.	Function
VBIAS[0] VBIAS[1]	Bias Voltage	AK28 E6	Digital input biases (VBIAS). When tied to +5V, the VBIAS inputs are used to bias the wells of the digital inputs so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When VBIAS are tied to +3.3V, the digital inputs will only tolerate 3.3V level voltages. Refer to the notes at the end of this section for a list of digital input pins which are not 5V tolerant.
PBIAS[0] PBIAS[1] PBIAS[2] PBIAS[3]	Bias Voltage	R4 Y4 M5 W4	PECL input biases (PBIAS). When tied to +5V, the PBIAS inputs are used to bias the wells in the PECL inputs and output so that the pads can tolerate 5V without forward biasing internal ESD protection devices. When the PBIAS inputs are tied to +3.3V, the pads will only tolerate 3.3V level voltages. Please see the Operation section for detailed information.
QAVD[0] QAVD[1]	Analog Power	L4 V3	The quiet power (QAVD) pins for the analog core. QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information.
QAVS[0] QAVS[1]	Analog Ground	K1 V4	The quiet ground (QAVS) pins for the analog core. QAVS should be connected to analog ground of the QAVD supply. Please see the Operation section for detailed information.
VDD	Digital Power	The digital power (VDD) pins should be connected to a well-decoupled +3.3 V digital power supply. Total of 48. A1, A31, B2, B30, C3, C4, C16, C28, C29, D3, D4, D16, D28, D29, E5, E11, E16, E21, E27, L5, L27, T3, T4, T5, T27, T28, T29, AA5, AA27, AG5, AG11, AG16, AG21, AG27, AH3, AH4, AH16, AH28, AH29, AJ3, AJ4, AJ16, AJ28, AJ29, AK2, AK30, AL1, AL31	

Pin Name	Pin Type	PIN No.	Function
VSS	Digital Ground	The digital ground (VSS) pins should be connected to the digital ground of the digital power supply. Total of 56. A2, A3, A4, A6, A11, A16, A21, A26, A28, A29, A30, B1, B3, B16, B29, B31, C1, C2, C30, C31, D1, D31, F1, F31, L1, L31, T1, T2, T30, T31, AA1, AA31, AF1, AF31, AH1, AH31, AJ1, AJ2, AJ30, AJ31, AK1, AK3, AK16, AK29, AK31, AL2, AL3, AL4, AL6, AL11, AL16, AL21, AL26, AL28, AL29, AL30		
AVD[0] AVD[1] AVD[2] AVD[3] AVD[4] AVD[5] AVD[6] AVD[7] AVD[8] AVD[9] AVD[10] AVD[11] AVD[12] AVD[13] AVD[14] AVD[15] AVD[16] AVD[17] AVD[18]	Analog Power	The analog power (AVD) pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information. AA2, AB1, AB4, AB5, U5, AC4, AC5, AD3, J2, J4, H2, K3, K5, M3, M4, W5, W3, N2, P3	

Pin Name	Pin Type	PIN No.	Function
AVS[0] AVS[1] AVS[2] AVS[3] AVS[4] AVS[5] AVS[6] AVS[7] AVS[8] AVS[9] AVS[10] AVS[11] AVS[12] AVS[13] AVS[14] AVS[15] AVS[16] AVS[17] AVS[18]	Analog Ground		The analog ground (AVS) pins for the analog core. The AVS pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information. AA3, AB2, AC1, AC2,U4, AC3, AD1, AD2, J3, H1, J5 , K4, J1, N5, N4, Y3, V5, P4, R5
SAVS[0] SAVS[1] SAVS[2] SAVS[3] SAVS[4] SAVS[5] SAVS[6] SAVS[7]	Analog Ground		The shielding analog ground (SAVS) pins for the analog I/O pins. The SAVS pins should be connected to the analog ground of the analog power supply. These pins are for shielding purposes only and do not sink any current. Please see the Operation section for detailed information. K2, N3, R3, R1, U1, Y5, AA4, AB3

Notes on Pin Description:

1. All SPECTRA-622 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except: the SD, REFCLK+/-, RXD+/-, and RRCLK+/- inputs which operate at pseudo-ECL (PECL) logic levels.

2. The SPECTRA-622 digital outputs and bidirectionals which have 2 mA drive capability are: D[7:0], B3E, INTB, LAIS/RRCPDAT, LOF, LOS/RRCPCLK, RAD, RALM, RLD, RLDCLK, RLOW, ROH, ROHCLK, ROWCLK, RPOH,

RPOHCLK, RPOHEN, RPOHFP, RSLD, RSLDCLK, RSOW, RSUC, RTOH, RTOHCLK, RTOHFP, SALM, SCPO[1:0], TDO.

The SPECTRA-622 digital outputs and bidirectionals which have 4 mA drive capability are: DS3RDAT[12:1], DS3ROCLK[12:1], TLDCLK, TOHCLK, TOWCLK, TPOHCLK, TPOHFP, TPOHRDY, TSLDCLK, TTOHCLK, TTOHFP, OOF, RFPO, TFP.

The SPECTRA-622 digital outputs and bidirectionals which have 6 mA drive capability are: DC1JV1[4:1], DD[31:0], DDP[4:1], DPL[4:1], PGMRCLK, PGMTCLK, RCLK, TC1J1V1/TFPO, TCLK, TD[7:0], TDP, TPL.

3. The SPECTRA-622 digital outputs which are not 5 volt tolerant are: DC1JV1[4:1], DD[31:0], DDP[4:1], DPL[4:1], PGMRCLK, PGMTCLK, RCLK, TC1J1V1/TFPO, TCLK, TD[7:0], TDP, TPL. All other outputs and inputs are 5 volt tolerant.

4. Inputs ALE, MBEB, RSTB, SCPI[3:0], TMS, TDI and TRSTB have internal pull-up resistors.

5. The differential pseudo-ECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operations section.

6. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.

7. It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.

8. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operations sections.

9. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

10. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

11. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

12. Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operations section.

11 FUNCTIONAL DESCRIPTION

11.1 Receive Line Interface

The Receive Line Interface block performs clock and data recovery on the incoming 622.08 Mbit/s data stream and performs serial to parallel conversion based on the recovered SONET/SDH A1/A2 framing pattern. It allows direct interface of the SPECTRA-622 to optical modules (ODLs) or other medium interfaces. The clock and data recovery unit can be bypassed using by setting the RBYP bit of the SPECTRA-622 Line Configuration #1 register (0002H) to allow interworking the SPECTRA-622 with an external CRU.

The Receive line interface can also be configured as a parallel interface. The 8 bit parallel interface supplies data and parallel 77.76 Mhz input clock. The SONET/SDH frame alignment can also be supplied via the frame pulse input. If the frame alignment is not known, the interface will frame to the incoming frame itself. The interface is also able to byte align the incoming data . The byte alignment uses the SONET/SDH framing bits to find the correct bit boundary for the byte alignment.

11.1.1 Clock Recovery Unit

The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET/SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a 77.76 MHz reference clock. The clock recovery unit provides status bits that indicates whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

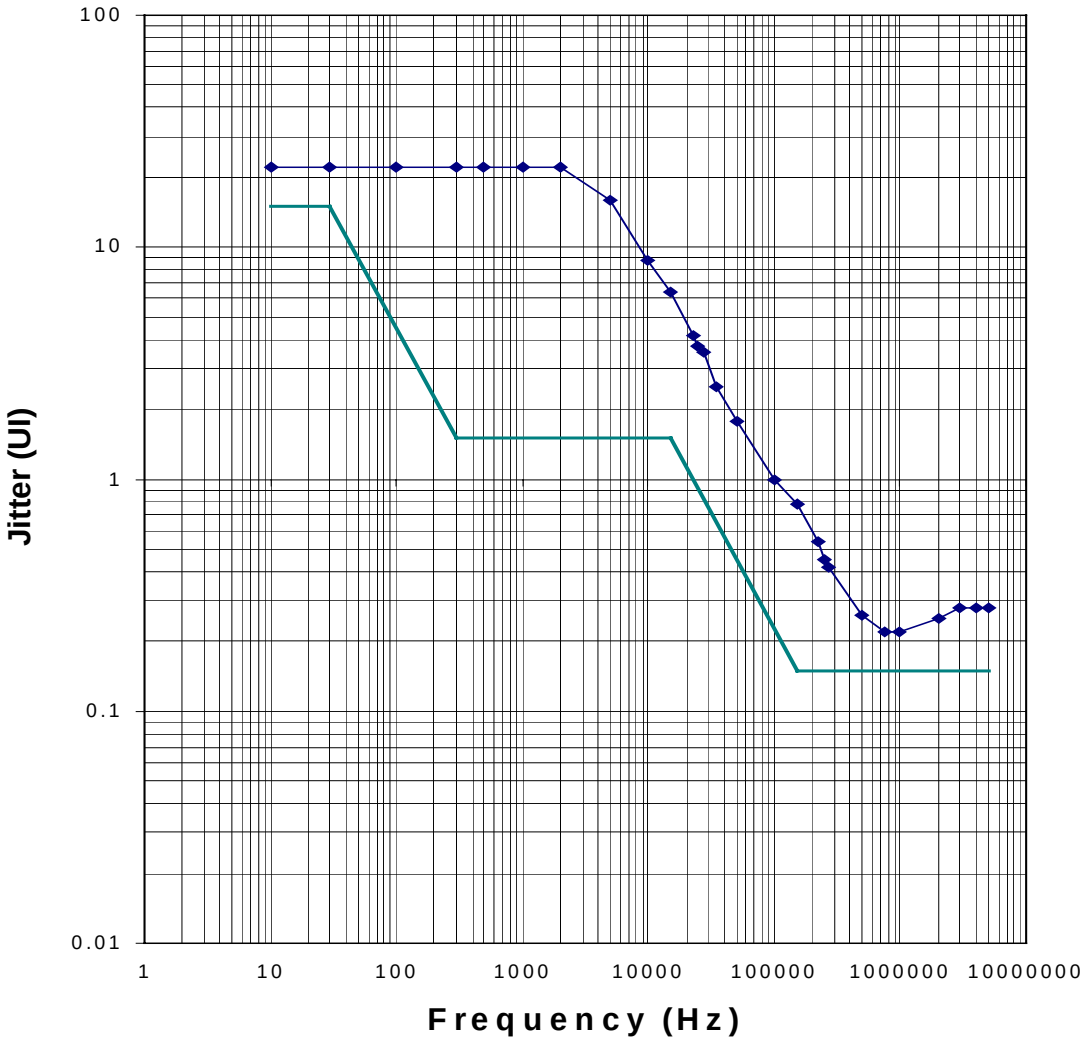
Initially, the PLL locks to the reference clock, REFCLK+/-. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK+/- reference accuracy under loss of signal conditions. In applications that are required to meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy

specification, the reference must be within +/-20 ppm. When not loop timed, the REFCLK+/- accuracy may be relaxed to +/-50 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE (issue 1995) as shown below.

Figure 11 - SPECTRA-622 Typical Jitter Tolerance at 622 Mbit/s



11.1.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial SONET/SDH stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

While out of frame, the CRSI-622 block monitors the receive bit-serial STS-12 (STM-4) data stream for an occurrence of the framing pattern (A1, A2). The CRSI-622 adjusts its byte alignment of the serial-to-parallel converter when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The CRSI-622 informs the RSOP Framer block when the framing pattern has been detected to reinitialize the RSOP to the new frame alignment. While in frame, the CRSI-622 maintains the byte alignment of the serial-to-parallel converter until RSOP declares out of frame.

11.2 Receive Section Overhead Processor (RSOP)

The Receive Section Overhead Processor (RSOP) block processes the section overhead (regenerator section) of the receive STS-12 (STM-4) stream.

The RSOP block optionally descrambles the received data and extracts the data communication channel, order wire channel and user channel from the section overhead, and provides them in gapped overhead mode as lower rate bit serial outputs (RSLD, RSOW, RSUC) together with associated clock signals (RSLDCLK, and ROWCLK). The complete descrambled SONET/SDH data stream is output by the RSOP in byte serial format. Line AIS is inserted in the receive data stream using input RLAIS or, optionally, automatically when loss-of-signal, loss-of-frame, section trace or loss-of-signal events occur. The automatic insertion of receive line AIS is controlled by the SPECTRA-622 Receive Line AIS Control Register.

Out-of-frame (OOF), loss-of-frame (LOF), and loss-of-signal (LOS) state outputs are provided and section level bit-interleaved parity errors are accumulated. A maskable interrupt is activated by state transitions on the SALM, LOF, or LOS outputs, or by a single B1 error event. Microprocessor readable registers are provided that allow accumulated B1 errors to be read out at intervals of up to one second duration.

The RSOP block frames to the data stream by operating with an upstream pattern detector (the Serial to Parallel Converter block) that searches for occurrences of the framing pattern (A1, A2) in the bit serial data stream. Once the serial to parallel converter has found byte alignment, the RSOP block monitors

for the next occurrence of the framing pattern 125µs later. The block declares frame alignment when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free. The first algorithm examines 24 bytes of A1 and A2 in the STS-12 (STM-4) stream. The second algorithm examines only the first occurrence of A1 and the first four bits of the last occurrence of A2 in the sequence. Once in frame, the RSOP block monitors the framing pattern sequence and declares OOF when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes are examined for bit errors in each frame, or only the A1 byte and the first four bits of the last A2 byte (i.e. 12 bits total) are examined for bit errors in each frame.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the serial to parallel converter which always examines all framing bits. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the SPECTRA-622 continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds in STS-12 (STM-4) SONET/SDH mode. The second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

When the parallel line interface PIN is used and upstream circuitry monitors the receive stream for an occurrence of the framing pattern while out-of-frame, the upstream circuitry is expected to pulse input FPIN when a framing pattern has been detected. RSOP monitors the receive data stream on PIN for the framing pattern as before. Once in frame, RSOP monitors the framing pattern sequence and sets the OOF pin when one or more bit errors in each framing pattern are detected for four consecutive frames.

The parallel line interface can also be used without the use of FPIN. The receive interface will frame to the parallel stream itself and function as in serial recovery mode.

The RSOP block provides descrambled data and frame alignment indication signals for use by the Receive Line Overhead Processor.

11.3 Receive Section Trace Buffer (SSTB)

In mode 1 operation, the receive portion of the SONET/SDH Section Trace Buffer (SSTB) captures the received section trace identifier message (J0 byte) into microprocessor readable registers. It contains three pages of trace message

memory. They are the capture page, the accepted page and the expected page. Section trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, line AIS may be inserted in the received stream when the receive message is in the mismatched or unstable state.

The length of the section trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the section trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the section trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the section trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

In addition, mode 2 section trace identifier operation is supported. For mode 2 support, a stable message is declared when forty eight of the same section trace identifier message (J0) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

If the section trace synchronization is disabled, the trace identifier mismatch and trace identifier unstable alarms are invalid, and may cause spurious interrupts.

11.4 Receive Line Overhead Processor (RLOP)

The Receive Line Overhead Processor block (RLOP) processes the line overhead (multiplexer section) of the receive STS-12 (STM-4) stream.

The SONET/SDH frame alignment is indicated by the Receive Section Overhead Processor. The RLOP extracts the line data communication channel, line order

wire channel and automatic protection switch channel from the line overhead, and provides them in gapped overhead mode as lower rate bit serial outputs (RLD, RLOW, ROH) together with associated clock signals (RLDCLK, ROWCLK, ROHCLK). Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The automatic protection switch bytes (K1, K2) are also extracted into the RASE Receive K1 Register and the RASE Receive K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE Receive K1/K2 Registers

The line level bit-interleaved parity (B2) is computed, and compared to the received B2 bytes. Line BIP-8 errors are accumulated in an internal counter. Registers are provided that allow accumulated line BIP-8 errors to be read out at intervals of up to one second duration.

Signal fail (SF) and signal degrade (SD) threshold crossing alarms are detected and indicated using internal register bits. The bit error rates associated with the SF and SD alarms are programmable over a range of 10^{-3} to 10^{-9} (See Section 14.5, Bit Error Rate Monitor, for details). The Receive APS, Synchronization Extractor and Bit Error (RASE) block extracts the Automatic Protection Switch (APS) bytes (K1 and K2), extracts the Synchronization Status byte (Z1/S1), and processes the Line BIP-8 (B2) events.

The received line BIP-8 error detection code (B2) byte is based on the line overhead and SPE of the receive stream. The line BIP code is a bit interleaved parity calculation using even parity, and the calculated BIP code is compared with the BIP code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 768000 (96 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-12 (STM-4) rate.

The line remote error indication (REI) byte (M1) is extracted and accumulated in an internal counter. Registers are provided that allow accumulated line REI events to be read out at intervals of up to one second duration. Bits 2 through 8 of the Z2/M1 byte are used for the line REI function. For STS-12 (STM-4)

streams, the line REI byte has 97 legal values (namely 00H - 60H) representing 0 to 96 line REI events. Illegal Z2/M1 values are interpreted as zero errors.

An interrupt output is provided that may be activated by declaration or removal of line AIS, line RDI, protection switching byte failure alarm, a change of APS code value, a single B2 error event, or a single line REI event. Each interrupt source is individually maskable.

11.5 Receive Transport Overhead Controller (RTOC)

The Receive Transport Overhead Controller block (RTOC) extracts the entire receive transport overhead on the RTOH, along with the nominal 20.736 MHz transport overhead clock, RTOHCLK, and the transport overhead frame position signal, RTOHFP, allowing identification of the bit positions in the transport overhead stream.

In addition, non-gapped (smooth) individual channels are generated on the outputs RSLD, ROH, RSUC, RLD and RLOW. These outputs are offered with two clocking modes, a smooth or gapped clock, the RTOC handles the smooth mode.. In the case of the smooth clock modes, output generated clocks are smooth and the RTOHFP can be used to identify the required byte alignment on the serial inputs. In gapped clock mode, the output generated clocks are gapped and gap detection circuitry is needed to identify the required data alignment on the serial outputs. The extracted TOH bytes on the above ports may also be forced to all ones on declaration of LOS/LOF/LAIS/TIM alarms.

11.6 Ring Control Port

The Transmit and Receive Ring Control Ports provide bit serial access to section and line layer alarm and maintenance signal status and control. These ports are useful in ring-based add drop multiplexer applications where alarm status and maintenance signal insertion control must be passed between separate SPECTRA-622s (possibly residing on separate cards). Each ring control port consists of three signals: clock, data and frame position. It is intended that the clock, data and frame position outputs of the receive ring control port are connected directly to the clock, data and frame position inputs of the transmit ring control port on the mate SPECTRA-622. The alarm status and maintenance signal control information that is passed on the ring control ports consists of

- Filtered APS (K1 and K2) byte values
- Change of filtered APS byte value status

- Protection switch byte failure alarm status
- Change of protection switch byte failure alarm status
- Insert the line RDI maintenance signal in the mate SPECTRA-622
- Insert the line AIS maintenance signal in the mate SPECTRA-622
- Insert line REI information in the mate SPECTRA-622.

The same APS byte values must be seen for three consecutive frames before being shifted out on the receive ring control port. The change of filtered APS byte value status is high for one frame when a new, filtered APS value is shifted out. The APS byte are not checked for valid value, only for identical values.

The protection switch byte failure alarm bit position is high when after twelve consecutive frames, starting with the last frame of the last three identical bytes sequence, no three consecutive frames contain identical K1 bytes have been received. The bit position is set low when three consecutive frames containing identical K1 bytes have been received. The change of protection switch byte failure alarm status bit position is set high for one frame when the alarm state changes.

The insert line RDI bit position is set high under register control, or when loss of signal, loss of frame, or line AIS alarms are declared. The insert line AIS bit position is set high under register control only.

The insert line REI bit positions are high for one bit position for each detected B2 bit error. Up to 96 line REIs may be indicated per frame for an STS-12 (STM-4) stream.

11.7 Receive Path Processing Slice (RPPS)

The Receive Path Processing Slice (RPPS) provides path processing, termination of one-twelfth of the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) stream received from the RLOP and provides DS3 de-mapping. Path processing includes pointer interpretation, path overhead and synchronous payload envelope (virtual container) extraction, and path level alarm and performance monitoring. Path trace identifier message (J1 bytes) is also extracted and processed. Plesiochronous frequency offsets between the receive data stream and the DROP bus are accommodated by pointer adjustments. The RPPS can also be configured to demap a DS3 signal from an STS-1 (STM-0/AU3) payload. PRBS payload generation and monitoring is also supported on a per STS (AU) basis.

Twelve RPPS's (RPPS#1 to RPPS#12) are required to process the STS-12 (STM-4) receive stream from RLOP. The RX_DEMUX block is in charge of de-multiplexing the STS-12 stream into 12 STS-1 streams. The mix of STS-3 (STM-1/AU3), STS-3c (STM-1/AU4), STS-Nc (STM-1/AU4-Xc) within the STS-12 (STM-4) stream is arbitrary. For an STS-12 (STM-4) consisting of twelve STS-1 (STM-0/AU3) streams, individual RPPS's will be independently processing an STS-1 (STM-0/AU3) stream each. For an STS-12 (STM-4) consisting of four STS-3/3c (STM-1/AU3/AU4) streams, the RPPS's must be configured into four groups with each group processing an STS-3/3c (STM-1/AU3/AU4) stream. An STS-3 (STM-1/AU3) stream is processed as three independent STS-1 (STM-0/AU3) streams by the individual RPPS's in the group.

In processing an STS-3c (STM-1/AU4), the first STS-1 (STM-0/AU3) equivalent stream will be processed by an RPPS (e.g. RPPS#1) configured as the master. The master RPPS controls two slave RPPS's (e.g. RPPS#5, RPPS#9) which process the second and third STS-1 (STM-0/AU3) equivalent streams respectively. Processing of a concatenated stream is co-ordinated by the control signals originating from the master RPPS and status information fed back from the slave RPPS's. Similarly, an STS-12c (STM-4-4c) is processed by the master RPPS (RPPS#1) controlling eleven slave RPPS's (RPPS#2 to RPPS#12).

Path Overhead bytes are extracted and serialized on output RPOH. RPOH is a multiplexed output signal carrying the path overhead bytes extracted by the RPPS's from all the receive STS-1 (STM-0/AU3) streams, STS-3c (STM-1/AU4) streams or the single STS-12c (STM-4-4c) stream. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) of the first STS-1 (STM-0/AU3) or the first STS-3c (STM-1/AU4) or the single STS-12c (STM-4-4c) on RPOH. Path overhead bytes are provided on RPOH at close to twice the rate in which they are received to facilitate the multiplexing of the extracted data from the various RPPS's on to a single serial output. Output RPOHEN is provided to mark the valid (fresh) path overhead bytes on RPOH. The path overhead clock, RPOHCLK is nominally a 12.96 MHz clock. RPOH, RPOHEN and RPOHFP are updated with timing aligned to RPOHCLK.

Received path BIP errors and receive path alarms for all the receive STS-1 (STM-0/AU3) streams, STS-3c (STM-1/AU4) streams or the single STS-12c (STM-4-4c) stream are communicated to the corresponding transmit path processing slices (TPPS's) in a mate SPECTRA-622 via the receive alarm port. The port carries the count of received path BIP errors. Detected receive alarms are reported in the alarm port and will trigger the corresponding remote TPOP to signal path RDI in the transmit stream.

The PRBS generator of an RPPS can be enabled to generate the DROP bus transport frame in addition to the payload. For an STS-3c (STM-1/AU4) stream,

the PRBS generator in each of the three RPPS's required to process the concatenated stream will generate one third (1 in 3) of the PRBS payload sequence. A complete PRBS payload sequence is produced when these three partial sequences are byte interleaved. The PRBS generator in the master RPPS co-ordinates the PRBS generation by itself and by its counterparts in the two slave RPPS's.

Similarly for an STS-12c (STM-4-4c) stream, the PRBS generator in the master RPPS will co-ordinate the distributed PRBS generation by the PRBS generators in the twelve RPPS's required to process this concatenated stream. Each PRBS generator will generate one twelfth (1 in 12) of the complete PRBS payload sequence.

When enabled, the PRBS monitor of an RPPS will synchronize to the receive payload sequence in an STS-1 (STM-0/AU3) or equivalent stream. If it is successful in finding the pseudo-random sequence then pattern errors detected will be accumulated in the corresponding error counter of each slice. For an STS-3c (STM-1/AU4) stream, the PRBS monitor in each of the three RPPS's required to process the concatenated stream will independently validate one third (1 in 3) of the PRBS payload sequence. For an STS-12c (STM-4-4c) stream, the PRBS monitor in each of the twelve RPPS's will validate one twelfth (1 in 12) of the PRBS payload sequence. The total number of errors for a STS-3c or STS-12c is representated by the sum of the master slice error count and of all its slave.

11.7.1 Receive Path Overhead Processor (RPOP)

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

11.7.1.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in an STS-1 (STM-0/AU3) or equivalent stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

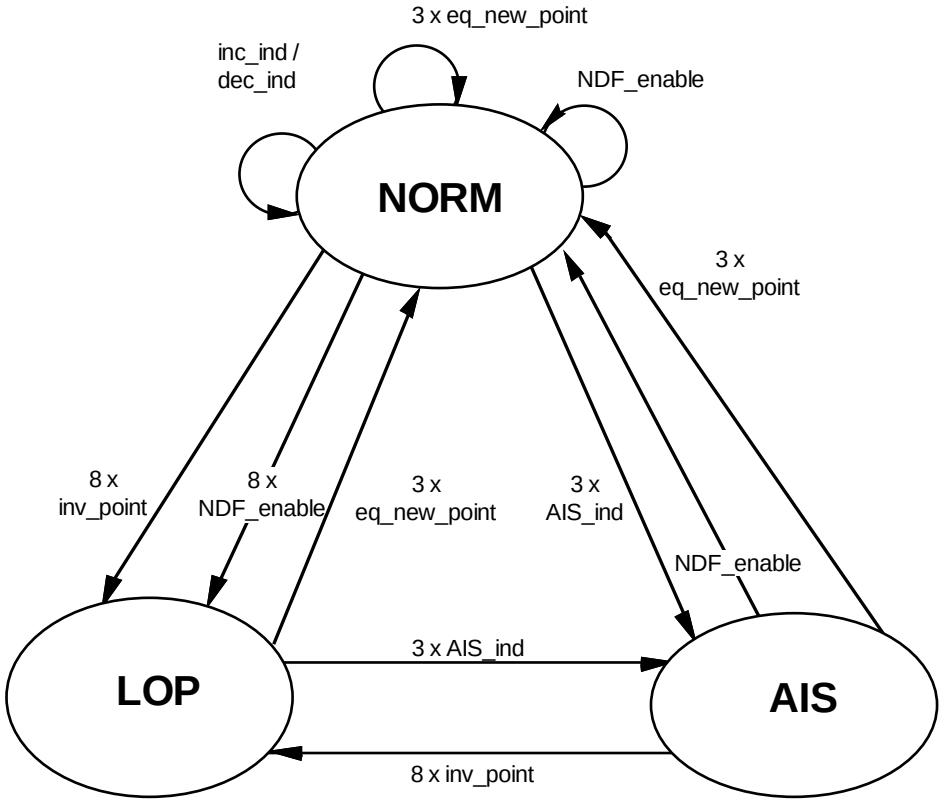
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 12 - Pointer Interpretation State Diagram



The following events (indications) are defined

norm_point : disabled NDF + ss + offset value equal to active offset

NDF_enable: enabled NDF + ss + offset value in range of 0 to 782

AIS_ind: H1 = 'hFF, H2 = 'hFF

inc_ind:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point:	not any of above (i.e., not norm_point, and not NDF_enable, not AIS_ind, and not inc_ind and not dec_ind)
new_point:	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted
dec_req:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted
Note 1	active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
Note 2	enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
Note 3	disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
Note 4	the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.
Note 5	ss bits are unspecified in SONET and has bit pattern 10 in SDH
Note 6	the use of ss bits in definition of indications may be optionally disabled.
Note 7	the requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
Note 8	new_point is also an inv_point.

Note 9	LOP is not declared if all the following conditions exist: the received pointer is out of range (>782), the received pointer is static, the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification. When the received pointer returns to an in-range value, the SPECTRA-622 will interpret it correctly.
Note 10	LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.
Note 11	For the purposes of 8xNDF_enable only, the requirement of the pointer to be within the range of 0 to 782 may be optionally disabled.

The transitions indicated in the state diagram are defined as follows:

inc_ind/dec_ind:	offset adjustment (increment or decrement indication)
3 x eq_new_point:	three consecutive equal new_point indications
NDF_enable:	single NDF_enable indication
3 x AIS_ind:	three consecutive AIS indications
8 x inv_point:	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications
Note 1	the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
Note 2	3 x new_point takes precedence over 8 x inv_point and resets the inv_point counter.

Note 3 all three offset values received in 3 x eq_new_point must be identical.

Note 4 "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in an STS-1 (STM-0/AU3) stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the DROP bus when LOP is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-622 to insert a path RDI indication. The Pointer Interpreter detects path AIS in an STS-1 (STM-0/AU3) stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-622 to insert a path RDI indication. The Pointer Interpreter detects loss of pointer – concatenated (LOPC) in an equivalent STS-1 (STM-0/AU3) stream. This alarm should be disabled for a RPOP operating in a master RPPS. LOPC is declared on entry to the LOPC_state as a result of eight consecutive pointers with values other than concatenation indications (‘b1001 xx 1111111111). Path AIS is optionally inserted in the DROP bus when LOPC is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-622 to insert a path RDI indication.

The Pointer Interpreter detects path AIS – concatenated (PAISC) in an equivalent STS-1 (STM-0/AU3) stream. This alarm should be disabled for a RPOP operating in a master RPPS. PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the DROP bus when AISC is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-622 to insert a path RDI indication.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset

is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

11.7.1.2 Multiframe Framer

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits. If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift. The primary process will enter out of multiframe state (OOM). A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected. Loss of multiframe (LOM) is declared after residing in the OOM state for eight frames without re-alignment. A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected.

11.7.1.3 Error Monitoring

Two 16-bit counters are provided to accumulate path BIP-8 errors (B3) and path remote error indications (REI). The contents of the counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame. BIP-8 errors are selectable to be counted as bit errors or as block errors via register bits. When processing a concatenated stream, the RPOP in a master RPPS will include the BIP-8 values computed by its slave RPPS's in the generation of the actual BIP-8 for the stream.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in

bits 5,6,7 of the path status byte indicates the same non error codepoint for five/ten consecutive frames.

11.7.1.4 Path Overhead Extract

Path overhead bytes are extracted from an STS-1 (STM-0/AU3) or equivalent stream which are being processed by the RPOP. When processing a concatenated stream, only the RPOP in a master RPPS will provide valid path overhead bytes. The extracted path overhead bytes will be serialized and multiplexed on to RPOH by higher level logic.

11.7.1.5 Receive Alarm Port

Path BIP errors and path remote defect indications (RDI) for an STS-1 (STM-0/AU3) or equivalent stream which are being processed by the RPOP are provided to the higher level logic for communicating via the Receive Alarm Port to the corresponding transmit path overhead processor (TPOP) in a mate SPECTRA-622. When processing a concatenated stream, only the RPOP in the master RPPS will provide the valid path BIP error count and path RDI code for the stream.

11.7.2 Receive Path Trace Buffer (SPTB)

In mode 1 operation, the receive portion of the SONET/SDH Path Trace Buffer (SPTB) captures the received path trace identifier message (J1 bytes) into microprocessor readable registers. It contains three pages of trace message memory. They are the capture page, the accepted page and the expected page. Path trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message the unstable counter is incremented by one. When the unstable count reaches eight, the received message is declared unstable. The received message is declared stable and the unstable counter reset, when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, path AIS may be inserted

in the DROP bus when the receive message is in the mismatched or unstable state.

The length of the path trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the SPTB synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the SPTB synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the path trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

In addition, mode 2 path trace identifier operation is supported. For mode 2 support, a stable message is declared when forty eight of the same section trace identifier message (J1) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

The path signal label (PSL) found in the path overhead byte (C2) is processed. Two detection algorithms are implemented for the declaration of path signal label mismatch. In mode 1, an incoming PSL is accepted when it is received unchanged for five consecutive frames. The accepted PSL is compared with the provisioned value. The PSL match/mismatch state is determined as follows:

Table 1 Path Signal Label match/mismatch state table.

Expected PSL	Accepted PSL	PSLM State
00	00	Match
00	01	Mismatch
00	X ≠ 00	Mismatch
01	00	Mismatch
01	01	Match
01	X ≠ 01	Match
X ≠ 00, 01	00	Mismatch
X ≠ 00, 01	01	Match
X ≠ 00, 01	X	Match
X ≠ 00, 01	Y	Mismatch

Each time an incoming PSL differs from the one in the previous frame, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once

on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable, when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive frames.

In mode2, the receive path signal mismatch alarm (PSLM) is declared based on the declaration of a match or mismatch between the received label and the expected label. The mismatch is set when 5 consecutive mismatches are declared. The mismatch is cleared when 5 consecutive matches are declared. Table 2 shows the Match/Mismatch and Unequipped declarations made to the different received and expected labels.

Table 2 PSL Mode 2 Match, Mismatch and Unequipped

Expect	Receive	Action	
00	00	Unequipped	Note:
00	01	Mismatch	
00	XX	Mismatch	XX = anything except 00H or 01H
01	00	Unequipped	YY = anything except 00H or 01H
01	01	Match	(XX not equal YY).
01	XX	Match	
XX	00	Unequipped	
XX	01	Match	
XX	XX	Match	
XX	YY	Mismatch	

The Unequipped (UNEQ) alarm is decallared based on the unequipped declaration. UNEQ is set high when 5 consecutive Unequipped are declared. UNEQ is set low when 5 consecutive Match or Mismatch are declared. The UNEQ and PSLM alarms are mutually exclusive.

In normal operation, only the status of the SPTB in a master RPPS should be monitored.

11.7.3 Receive Telecombus Aligner (RTAL)

The Receive Telecombus Aligner (RTAL) block takes the payload data from an STS-1 (STM-0/AU3) or equivalent stream from the Receive Path Overhead Processor. It aligns the frame of the received STS-1 (STM-0/AU3) or equivalent stream to the frame of the DROP bus. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the receive stream and that of the DROP bus. When processing a concatenated stream, only the RTAL in the master RPPS will be performing the pointer adjustment calculation. The RTAL's in the slave RPPS's will follow the new alignment of the RTAL in the master RPPS.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the receive data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. DROP bus pointer justification events are indicated and are accumulated in the Performance Monitor (PMON) block. Large differences between the number and type of received pointer justification events as indicated by the RPOP block, and pointer justification events generated by the RTAL block may indicate network synchronization failure.

When the RPOP block detects a loss of multiframe, the RTAL may optionally insert all ones in the tributary portion of the SPE. The path overhead column and the fixed stuff columns are unaffected.

The RTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a synchronous payload envelope (virtual container) may optionally be over-written all-zeros in the fixed stuff bytes.

During a PAIS condition, jump in J1 location can occur on the DROP bus.

11.7.3.1 Elastic Store

The Elastic Store perform rate adaptation between the receive data stream and the DROP bus. The entire received payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the receive byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Receive pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the DROP bus rate by the Pointer Generator. Analogously, pointer justifications on the DROP bus are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the DROP bus for three frames to alert downstream elements of data corruption. During PAIS, outgoing pointer justifications are not performed.

The elastic store may be bypassed through register control in Register 0n00H: Spectra-622 RPPS Configuration. DCK must be connected to PGMRCLK in this case. If the DROP interface is in the 77.76 MHz configuration, the DROP Bus DLL might need to be reseted, with register 00A6H, if the PGMRCLK is unstabled after the reset.

When in RTAL FIFO bypass mode, the V1 pulse on the DROP bus will always be outputted, it cannot be disabled. Also, the autonomous mode of the DPGM is not supported in bypass mode.

11.7.3.2 Pointer Generator

The Pointer Generator generates the DROP bus pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the DROP bus STS-1 (STM-0/AU3) stream. The algorithm can be modeled by a finite state machine. Within the pointer generator algorithm, five states are defined as shown below:

NORM_state (NORM)

AIS_state (AIS)

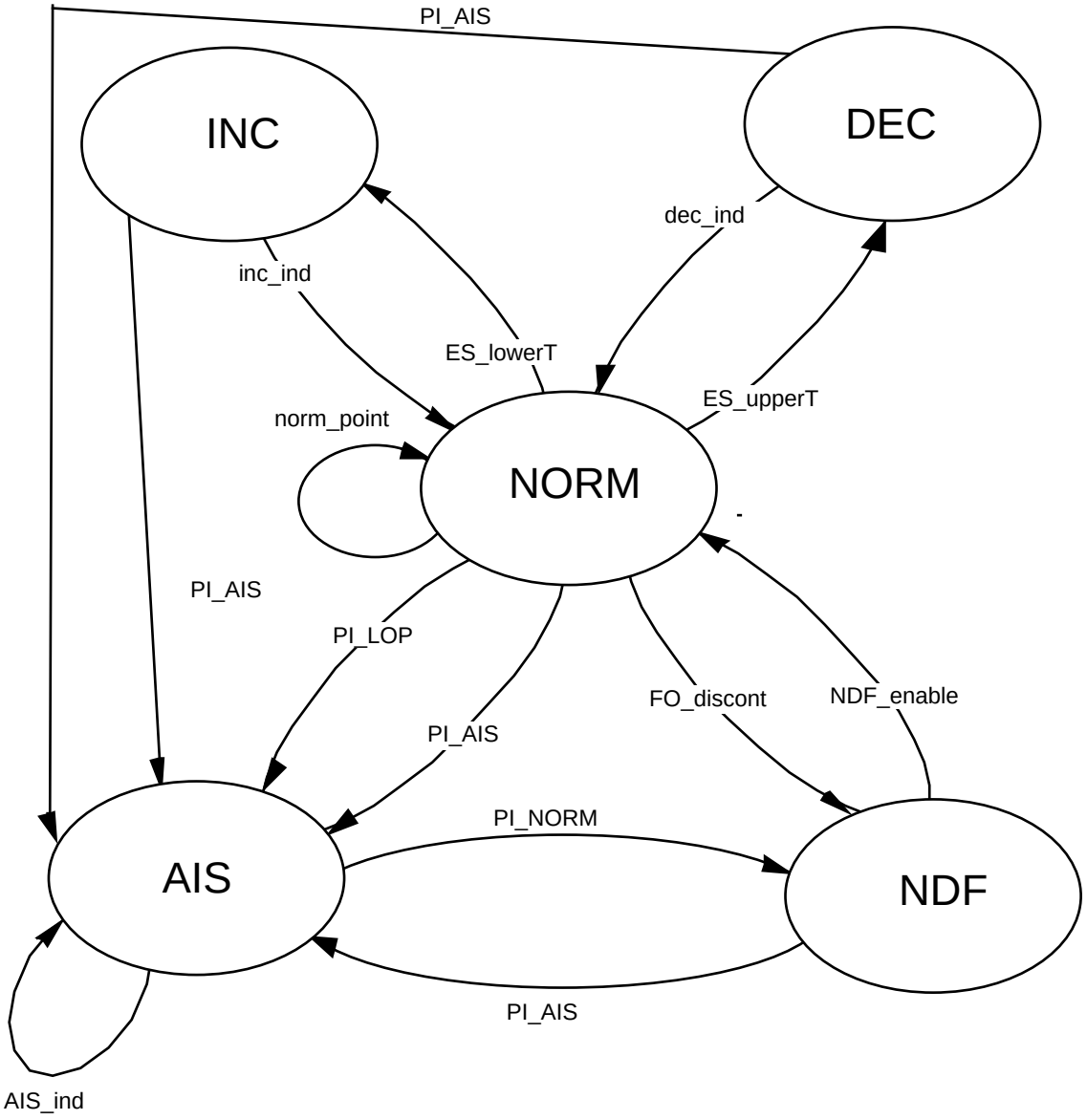
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive Path Overhead Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 13 - Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note 1 A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Note 1 active offset is defined as the phase of the SPE (VC).

Note 2 the ss bits are undefined in SONET, and has bit pattern 10 in SDH

Note 3 enabled NDF is defined as the bit pattern 1001.

Note 4 disabled NDF is defined as the bit pattern 0110.

When operating in a slave RPPS, the concatenation indications (‘b1001 xx 1111111111) will be generated in the pointer bytes (H1 and H2) when enabled in the RPOP block.

11.7.3.3 Bypass

The RPPS can be put in bypass mode by setting the RESBYP of the DROP Bus Configuration register (bit 4, register 0D30H). In this mode, all twelve slices are

put in bypass mode. Once in bypass, all the features related to the RTAL can no longer be use. This includes the generation of pointers and of TUAIS alarms. The drop clock, DCK, must be connected to the PGMRCLK since FIFOs are no longer present. The pointer outputted on the drop bus will be the same as the one received. Since pointer generation related to AIS transitions is not supported, no NDF will be generated.

When in bypass mode, the V1 pulse on the DROP bus will always be outputted, it cannot be disabled. Also, the autonomous mode of the DPGM is not supported in bypass mode.

11.7.4 DS3 Mapper DROP Side (D3MD)

The DS3 Mapper DROP Side (D3MD) block demaps a DS3 signal from an STS-1 (STM-0/AU3) receive stream. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. The asynchronous DS3 mapping is shown below:

Table 3 - Asynchronous DS3 mapping to STS-1 (STM-0/AU3).

J1	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
STS	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
POH	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I

R: Fixed Stuff bit - set to logic ‘0’ or ‘1’

C: Stuff Control bit - set to logic ‘1’ for stuff indication

S: Stuff Opportunity bit - when stuff control bit is ‘0’, stuff opportunity is I bit

O: Overhead communication channel

I: DS3 payload information

11.7.4.1 DS3 Demapper

The D3MD performs majority vote on the received C-bits. If 3 out of 5 C-bits are ‘1’s, the associated S bit is interpreted as a stuff bit. If 3 out of 5 C-bits are ‘0’s, the associated S bit is interpreted as an Information bit. The information bits are written to an elastic store and the Fixed Stuff bits (R) are ignored.

Given a LOS, LOF, LAIS, LOP, PAIS, path signal label mismatch (PSLM) or path signal label unstable (PSLU), path trace identifier mismatch (TIM) or path trace identifier unstable (mode 1 or 2 TIU) condition, the D3MD optionally ignores the STS-1 (STM-0/AU3) SPE and writes a DS3 AIS pattern to the elastic store. In addition, the desynchronization algorithm assumes a nominal ratio of data to stuff bits carried in the S bits (1 out of 3 S bits is assumed to be an information (data) bit). DS3 AIS is defined below:

Table 4 - DS3 AIS format.

X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**

- valid M-frame alignment bits (M-bits), M-subframe alignment bits (F-bits), and parity bit of the preceding M-frame (P-bits). The two P-bits are identical, either both are zeros or ones.
- all the C-bits in the M-frame are set to zeros
- the X-bits are set to ones
- the information bit (84 Data bits with repeating sequence of 1010..)

11.7.4.2 Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS-3 stream extracted from the STS-1 (STM-0/AU3) SPE and the incoming DS3RICLK. The DS3 Demapper extracts I bits from the STS-1

(STM-0/AU3) SPE and writes the bits into a 128 bit (16 byte) elastic store. Eight bytes are provided for SONET/SDH overhead (3 bytes for TOH, 1 byte for a positive stuff, 1 byte for POH) and DS3 reserve stuffing bits (2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte). The remaining 8 bytes are provided for path pointer adjustments.

Data is read out of the Elastic Store using a divide by 8 version of the input DS3RICLK clock. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

11.7.4.3 DS3 Desynchronizer

The Desynchronizer monitors the Elastic Store level to control the de-stuffing algorithm to avoid overflow and underflow conditions. The Desynchronizer assumes either a 51.84 MHz clock (provided internally from REFCLK) or a 44.928 MHz clock (provided via input DS3RICLK).

When using a 44.928 MHz DS3RICLK clock, the DS3 clock is generated using a fixed 8 KHz interval. The 8KHz interval is subdivided into 9 rows. Each row contains either 621 or 622 clock periods. The DS3RICLK contains 624 pulses at 72KHz (9*8KHZ). To generate 621 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 207 clocks + 1 clock gap is used. To generate 622 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 208 clocks is used.

When using the internal 51.84 MHz clock, the DS3 clock, DS3ROCLK is generated using similar gapping patterns. To generate 621 pulses per row, a gapping pattern of 63 * (7 clocks + 1 clock gap) + 36 * (5 clocks + 1 clock gap) is used. To generate 622 pulses per row, a gapping pattern of 63 * (7 clocks + 1 clock gap) + 35 * (5 clocks + 1 clock gap) + 6 clocks) is used.

The following table illustrates the gap patterns used to generate the desynchronized clock, DS3ROCLK under the normal, DS3 AIS, faster and slower status. The faster pattern is used to drain the elastic store to avoid overflows. The slower pattern is used to allow the elastic store to fill to avoid underflows.

Table 5 - DS3 desynchronizer clock gapping algorithm.

Row Number	Normal or DS3 AIS	Run Faster	Run Slower
1	621	621	621
2	621	621	621
3	622	622	622
4	621	621	621
5	621	622	621
6	622	622	621
7	621	621	621
8	621	622	621
9	622	622	621

11.7.5 DROP Bus PRBS Generator and Monitor (DPGM)

The DROP bus Pseudo-random bit sequence Generator and Monitor (DPGM) block generates and monitors an unframed 2^{23}-1 payload test sequence in an STS-1 (STM-0/AU3) or equivalent stream on the DROP bus.

The PRBS generator of the DPGM can be configured to overwrite the payload bytes on the DROP bus as well as autonomously generating both the payload bytes and the framing on the DROP bus. The path overhead column and, optionally, the fixed stuff columns in an STS-1 (STM-0/AU3) stream are not overwritten with PRBS payload bytes. When processing a concatenated stream, the DPGM in a master RPPS co-ordinates the distributed PRBS generation by itself and its counterparts in the slave RPPS's. Each DPGM will generate one twelfth (1 in 12) of the complete PRBS sequence for an STS-12c (STM-4-4c) stream. The master DPGM will be generating the partial sequence for the 1st (after the transport overhead columns) and subsequent SPE bytes occurring at a 12-byte interval. The next partial sequence for the 2nd and every twelfth bytes thereafter will be generated by the first (in the order of payload generation) slave DPGM and so on. This corresponds to each DPGM processing an equivalent STS-1 (STM-0/AU3) stream in the concatenated stream. Similarly, for an STS-3c (STM-4/AU4) stream, one third (1 in 3) of the sequence is generated per DPGM.

To ensure that the DPGM blocks in the slave RPPS's are synchronized with the DPGM in the master RPPS, a signature derived from its current state is continuously broadcasted by the master DPGM to allow the slave DPGM blocks to check their relative states. A DPGM operating in a slave RPPS continuously

generates a matching signature based on its own state. A signature mis-match is flagged as an out-of-synch state by the slave DPGM. A re-synchronization of the PRBS generation is initiated by the master DPGM (under software control) when one or more slave DPGM's report an out-of-synch state in relation to that of the master DPGM. This involves a re-starting of PRBS generation in each DPGM from a pre-determined state according to the order of generation (transmission or reception) assigned to a particular DPGM.

When a path overhead byte position is encountered by the master DPGM in an STS-3c (STM-1/AU4) stream, the master DPGM will not generate the next PRBS data byte, this task is left to the (first) slave DPGM which is next in line to generate a PRBS data byte. The second slave DPGM (in the order of generation) will now generate the PRBS data byte which is supposed to be generated by the first slave DPGM and so on. This means that the current states of the slave DPGM blocks will be re-aligned relative to the new state of the master DPGM to collectively skip over the path overhead byte position encountered by the master DPGM. For an STS-12c (STM-4-4c) stream, the states of all twelve DPGM blocks required to process the stream have to be re-aligned to collectively skip over the path overhead byte and the three consecutive fixed stuff bytes immediately following it.

The PRBS monitor of the DPGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors detected based on this pseudo-random pattern. The DPGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the DPGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the DPGM will fall out of synchronization and it will continuously attempt to re-synchronize to the input sequence until it is successful.

When processing a concatenated stream, individual DPGM blocks, including the master DPGM, independently monitor their corresponding one twelfth (1 in 12) or one third (1 in 3) of the complete PRBS payload sequence according to the SONET/SDH concatenated mode of the stream. The master DPGM will be monitoring the partial sequence contained in the 1st (after the transport overhead columns) and subsequent SPE bytes occurring at a 12-byte interval. The next partial sequence contained in the 2nd and every twelfth bytes thereafter will be validated by the first (in the order of payload reception) slave DPGM and so on. Individual DPGM synchronization status and error count accumulation are provided. Optionally, an interrupt can be generated by the DPGM whenever a loss of synchronization or re-synchronization occurs.

Path overhead bytes and fixed stuff columns in the receive concatenated stream will be collectively skipped over as described for the PRBS generator of the

DPGM. To ensure that all payload bytes (all STS-1 (STM-0/AU3) or equivalent streams) in a concatenated stream together contain a single PRBS sequence, the signature generation by the master DPGM and signature matching by the slave DPGM monitors will be performed as described for the PRBS generation. Individual DPGM can only declared that has synchronized to the receive PRBS sequence when it has synchronized to its corresponding partial sequence and its has detected no signature mis-match.

If the DFP aligment is changed, all the slices will be resynchronized to the new frame pulse and the aligment of the PRBS sequence for concatenated payload might be loss. The PRBS sequence thus need to be regenerated by setting the GEN_REGEN bit of all the master slices. The signature analyzer interrupt (GEN_SIGE) can be used to detect this condition.

To use the autonomous mode of the DPGM, the RPPS must not be put in bypass mode, bit RESBYP of register 0D30H must not be set.

11.8 Transmit Path Processing Slice (TPPS)

The Transmit Path Processing Slice (TPPS) generates transport frame alignment, inserts path overhead and synchronous payload envelope as well as path level alarm signals and path BIP-8 (B3) for an STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus. Path trace identifier message (J1 bytes) can also be inserted. Plesiochronous frequency offsets and phase differences (due to normal network operation) between the ADD bus and the line are accommodated by pointer adjustments in the transmit stream. The TPPS can optionally interpret the pointer (H1, H2) and detects alarm conditions (e.g. PAIS) in the STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus. The TPPS can also be configured to map a DS3 signal into the transmit STS-1 (STM-0/AU3) stream. PRBS payload generation and monitoring is also supported on a per STS (AU) basis.

Twelve TPPS’s (TPPS#1 to TPPS#12) are required to process the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) stream from the ADD bus. For an STS-12 consisting of twelve STS-1 (STM-0/AU3) streams, individual TPPS’s will be independently processing an STS-1 (STM-0/AU3) stream each. For an STS-12 consisting of four STS-3/3c (STM-1/AU3/AU4) streams, the TPPS’s must be configured into four groups with each group processing an STS-3/3c (STM-1/AU3/AU4) stream. An STS-3 (STM-1/AU3) stream is processed as three independent STS-1 (STM-0/AU3) streams by the individual TPPS’s in the group.

In processing an STS-3c (STM-1/AU4), the first STS-1 (STM-0/AU3) equivalent stream will be processed by a TPPS (e.g. TPPS#1) configured as the master. The master TPPS controls two slave TPPS’s (e.g. TPPS#5, TPPS#9) which

process the second and third STS-1 (STM-0/AU3) equivalent streams respectively. Processing of a concatenated stream is co-ordinated by the control signals originating from the master TPPS and status information feedback from the slave TPPS's. Similarly, an STS-12c (STM-4-4c) is processed by the master TPPS (TPPS#1) controlling eleven slave TPPS's (TPPS#2 to TPPS#12).

TPOH is a multiplexed input signal carrying the path overhead bytes for the transmit STS-1 (STM-0/AU3), the STS-3c (STM-1/AU4) streams or the single STS-12c (STM-4-4c) stream being processed by the TPPS's. Output TPOHFP is provided to identify the most significant bit of the path trace byte (J1) of the first STS-1 (STM-0/AU3) or the first STS-3c (STM-1/AU4) or the single STS-12c (STM-4-4c) on TPOH. Time-slots for path overhead bytes insertion via TPOH are provided at close to twice the rate in which the path overhead bytes are transmitted. This is to facilitate the multiplexing of input path overhead bytes destined for the various TPPS's. Input TPOHEN is used to mark the most significant bit of a path overhead byte that needs to be transmitted in the corresponding transmit stream. Output TPOHRDY is provided to indicate that a particular path overhead byte on TPOH is accepted for transmission. Re-insertion of a path overhead byte in its next available time-slot on TPOH is required if it is not accepted for transmission during the current time-slot. The transmit path overhead clock, TPOHCLK is nominally a 12.96 MHz clock. TPOH, TPOHEN, TPOHRDY and TPOHFP are sampled or updated by TPOHCLK.

Received path BIP errors (REI) and path remote defect indications (RDI) for all the receive STS-1 (STM-0/AU3) streams, STS-3c (STM-1/AU4) streams or the single STS-12c (STM-4-4c) stream from the RPPS's in a remote SPECTRA-622 are communicated to the corresponding TPPS's in the local SPECTRA-622 via the transmit alarm port. The transmit alarm port can also contain the transmit APS bytes (K1, K2) of the (remote) working SPECTRA-622. In the protection (local) SPECTRA-622, the APS bytes in the transmit stream may be optionally sourced from the transmit alarm port.

The PRBS generator of an TPPS can be enabled to overwrite the transmit stream framing in addition to the payload. For an STS-3c (STM-1/AU4) stream, the PRBS generator in each of the three TPPS's required to process the concatenated stream will generate one third (1 in 3) of the PRBS payload sequence. A complete PRBS payload sequence is produced when these three partial sequences are byte interleaved downstream. The PRBS generator in the master TPPS co-ordinates the PRBS generation by itself and its counterparts in the two slave TPPS's.

Similarly for an STS-12c (STM-4-4c) stream, the PRBS generator in the master TPPS will co-ordinate the distributed PRBS generation by the PRBS generators in the twelve TPPS's required to process this concatenated stream. Each PRBS

generator will generate one twelfth (1 in 12) of the complete PRBS payload sequence.

When enabled, the PRBS monitor of a TPPS will attempt to synchronize to the payload sequence in the STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus. If it is successful in finding the supported pseudo-random sequence then pattern errors detected will be accumulated in the corresponding error counter. For an STS-3c (STM-1/AU4) stream, the PRBS monitor in each of the three TPPS's required to process the concatenated stream will independently validate one third (1 in 3) of the PRBS payload sequence. For an STS-12c (STM-4-4c) stream, the PRBS monitor in each of the twelve TPPS's will validate one twelfth (1 in 12) of the PRBS payload sequence. The total number of errors for a STS-3c or STS-12c is representated by the sum of the master slice error count and of all its slave.

11.8.1 ADD Bus PRBS Generator and Monitor (APGM)

The ADD bus Pseudo-random bit sequence Generator and Monitor (APGM) block generates and monitors an unframed 2^{23}-1 payload test sequence in an STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus.

The PRBS generator of the APGM can be configured to overwrite the payload bytes of the ADD bus STS-1 (STM-0/AU3) SPE (VC3) data stream with an unframed 2^{23}-1 sequence as well as autonomously generating both the payload bytes and the SPE (VC3) frames. The PRBS monitor of the APGM block monitors the payload data from the ADD bus for the presence of an unframed 2^{23}-1 sequence and accumulates pattern errors detected based on this pseudo-random pattern.

The operation of the APGM block is identical to that of the DPGM block described in the Receive Path Processing Slice section.

If the AFP/AC1J1V1 aligment is changed, all the slices will be resynchronized to the new frame pulse and the aligment of the PRBS sequence for concatenated payload might be loss. The PRBS sequence thus need to be regenerated by setting the GEN_REGEN bit of all the master slices. The signature analyzer interrupt (GEN_SIGE) can be used to detect this condition.

11.8.2 DS3 Mapper ADD Side (D3MA)

The DS3 Mapper ADD Side (D3MA) block maps a DS3 signal into an STS-1 (STM-0/AU3) transmit stream and compensate for any frequency differences between the incoming DS3 serial bit rate (DS3TICLK) and the available STS-1

(STM-0/AU3) SPE mapped payload capacity. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. Please refer to the D3MD block for a description of the DS3 mapping.

11.8.2.1 DS3 Serializer and Elastic Store

Incoming high speed serial data is sampled on the DS3TDAT input, deserialized and written into the Elastic Store by the DS3 Serializer block.

The elastic store block is provided to compensate for frequency differences between the DS-3 stream (DS3TDAT) and the STS-1 (STM-0/AU3) SPE capacity. The DS3 Serializer writes data into the elastic store at one eighth of the DS3TICLK rate while data is read out at the stuffed STS-1 (STM-0/AU3) byte rate. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

The Elastic store is 128 bits (16 bytes) to allow for a fixed read/write pointer lag of 7 bytes (3 bytes for TOH, 1 byte for POH, 2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte). Four bytes are also added on either side for positive and negative threshold detection.

11.8.2.2 DS3 Synchronizer

The DS3 Synchronizer performs the mapping of the DS3 into the STS-1 (STM-0/AU3) SPE. The DS3 Synchronizer monitors the Elastic Store level to control the stuffing algorithm to avoid overflow (i.e. run faster) and underflow (i.e. run slower) conditions. The fill level of the elastic store is monitored and stuff opportunities in the DS3 mapping are used to center the Elastic Store. To consume a stuff opportunity, the five C-bits on a row are set to ones and the S bit is used to carry an DS3 information bit. When the S bit is not used to carry information, the C-bits on the row are set to zeros.

The DS3 synchronizer uses a fixed bit leaking algorithm which leaks 8 bits of phase buildup in 500 µs. The 8kHz STS-1 (STM-0/AU3) frame interval is subdivided into 9 rows. Each row contains one stuff opportunity. The following table illustrates the stuffing implementation where S means stuff bit and I means an information bit (DS3 data).

Table 6 - DS3 synchronizer bit stuffing algorithm.

Row Number	Normal or DS3 AIS	Run Faster	Run Slower
1	S	S	S
2	S	S	S
3	I	I	I
4	S	S	S
5	S	I	S
6	I	I	S
7	S	S	S
8	S	I	S
9	I	I	S

Under microprocessor control, the incoming DS3 stream can be overwritten with the framed DS3 AIS. When asserting DS3 AIS, a nominal stuff pattern is used as illustrated above. Please refer to the D3MD functional description section for a description of the DS3 AIS frame.

The D3MA outputs the STS-1 (STM-0/AU3) with the mapped DS3 onto an internal ADD bus for further processing by the downstream block.

11.8.3 Transmit Pointer Interpreter Processor (TPIP)

The Transmit Pointer Interpreter Processor (TPIP) block takes STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus, interprets the pointer (H1, H2), indicates the J1 byte location and detects alarm conditions (e.g. PAIS).

The TPIP block allows the SPECTRA-622 to operate with Telecombus like back plane systems which do not indicate the J1 byte position. The TPIP block can be enabled using the DISJ1V1 bit in the SPECTRA-622 Path/DS3 Configuration register. When enabled, the TPIP takes a STS-1 (STM-0/AU3) SONET/SDH stream from the System Side Interface block, processes the stream, identifies the J1 byte location and provides the stream to the corresponding Transmit Telecombus Aligner block.

The TPIP is held in reset in DS3 mode, DS3ADDSEL = ‘1’ and when SLLBEN = '0' (reg 1n00). When held in reset, TPIP registers cannot be accessed.

11.8.4 Transmit Telecombus Aligner (TTAL)

The Transmit Telecombus Aligner (TTAL) block takes the STS-1 (STM-0/AU3) SPE (VC3) or equivalent data stream from the ADD bus and aligns it to the frame of the transmit stream. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the ADD bus and the transmit stream. In processing a concatenated stream, the TTAL in the master TPPS will perform the pointer offset recalculation and the TTAL's in the slave TPPS's will follow the new pointer offset.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the ADD bus and the transmit stream are accommodated by pointer adjustments in the transmit stream. For a concatenated stream, the master TTAL will compute and perform the appropriate pointer adjustment to which the slave TTAL's will follow.

The TTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a synchronous payload envelope (virtual container) may optionally be over-written with all-zeros in the fixed stuff bytes.

11.8.4.1 Elastic Store

The Elastic Store block performs rate adaptation between the ADD bus and the transmit stream. The entire ADD bus payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the ADD bus byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. ADD bus pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the transmit stream rate by the Pointer Generator block. Analogously, pointer justifications on the transmit stream are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests are made to the Pointer Generator block based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator block schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO

underflow and overflow events are detected and path AIS is inserted in the transmit stream for three frames to alert downstream elements of data corruption.

11.8.4.2 Pointer Generator

The Pointer Generator Block generates the transmit stream pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the transmit STS-1 (STM-0/AU3) or equivalent stream. The algorithm is identical to that described in the Receive Telecombus Aligner (RTAL) block.

When operating in a slave TPPS, the concatenation indications (‘b1001 xx 1111111111) will be generated in the pointer bytes (H1 and H2) when enabled in the TPOP block.

11.8.4.3 Bypass

The TPPS can be put in bypass mode by setting the TESBYP of the ADD Bus Configuration register (bit 5, register 1030H). In this mode, all twelve slices are put in bypass mode. Once in bypass, all the features related to the TTAL can no longer be used. This includes the generation of pointers and of TUAIS alarms. The ADD clock, ACK, must be connected to the PGMTCLK since FIFOs are no longer present. The pointer outputted on the tx side will be the same as the one received from the add bus. Since pointer generation related to AIS transitions is not supported, no NDF will be generated. In this mode, a mix of DISJ1V1 bit setting is not supported (register 1102H). In addition, a mix of Telecombus and DS3 is also not supported.

11.8.5 Transmit Path Trace Buffer (SPTB)

The transmit portion of the SONET/SDH Path Trace Buffer (SPTB) sources the path trace identifier message (J1) for the Transmit Path Overhead Processor (TPOP) block. The length of the trace message is selectable between 16 bytes and 64 bytes. The SPTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transmit Path Overhead Processor block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, SPTB may be programmed to transmit null characters to prevent transmission of partial messages.

11.8.6 Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion.

11.8.6.1 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE (VC) of the outgoing STS-1 (STM-0/AU3) or equivalent stream. The fixed stuff columns in the VC3 format may be optionally excluded from BIP calculations. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

In processing a concatenated stream, the BIP-8 Calculate Block of the TPOP in the master TPPS will include calculated BIP-8 values from the slave TPPS's in the final computation of the path BIP-8 (B3) value of the stream.

11.8.6.2 Path REI Calculate

The Path REI Calculate Block accumulates path remote error indications on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the path REI bit positions of the path status (G1) byte. The path REI information is derived from path BIP-8 errors detected by the corresponding Receive Path Overhead Processor, RPOP. The asynchronous nature of these signals implies that more than eight path REI events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining path REIs are transmitted at the next opportunity. Alternatively, path REI can be accumulated from path REI counts reported on the transmit alarm port when the local SPECTRA-622 is paired with a receive section of a remote SPECTRA-622. Far end block errors may be inserted under register control for diagnostic purposes. Optionally, path REI insertion may be disabled and the incoming G1 byte passes through unchanged to support applications where the received path processing does not reside in the local SPECTRA-622.

11.8.6.3 Transmit Alarm Port

Received path BIP errors (REI) and remote defect indications (RDI) from Receive Path Overhead Processors (RPOP) in a remote SPECTRA-622 are

communicated to the corresponding TPOP's in the local SPECTRA-622 via the transmit alarm port. When the port is enabled, the path BIP error count and the remote defect indication for each TPOP are sampled from the transmit alarm port and inserted in the path REI and path RDI positions of the path status byte (G1) in the transmit stream.

The TAD port can retrieve up to a maximum of 15 BIP errors for each slice per frame (125 us). Given the timing of the RAD port, a mate SPECTRA-622 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames, and the timing makes them appear within one frame period, one count could be lost.

11.8.6.4 Path Overhead Insert

The Path Overhead Control Block provides a bit serial path overhead interface to the TPOP. Any, or all of the path overhead bytes may be sourced from, or modified by the bit serial path overhead stream sampled from TPOH by higher-level logic. The individual bits of each path overhead byte are shifted in from the overhead controller using the path overhead clock generated by TPOP. The default path overhead byte values from internal register source are inserted in the STS-1 (STM-0/AU3) or equivalent stream if external modification via TPOH is not required. For example, the path trace byte (J1) is optionally sourced from the Transmit Path Trace Buffer block if J1 byte insertion via TPOH is not active.

11.8.6.5 SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the transmit stream. When in-band error reporting is enabled, the path REI and path RDI bits of the path status (G1) byte has already been formed by the corresponding Receive Path Overhead Processor and is transmitted unchanged.

11.9 Transmit Transport Overhead Controller (TTOC)

The Transmit Transport Overhead Controller block (TTOC) allows the manual insertion of the transmit transport overhead bytes, the insertion of section or line BIP errors or insertion of payload pointer byte errors.

The complete transport overhead to be inserted at once using the TTOH, along with the nominal 20.736 MHz transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from TTOH.

In addition, individual channels can be sourced from inputs TSLD, TOH, TSUC, TLD and TLOW. These inputs offer two clocking modes, a smooth or gapped clock. The non-gapped mode is processed by the TTOC. In the case of the smooth clock modes, output generated clocks for these inputs are smooth and the TTOHFP can be used to identify the required byte alignment on the serial inputs. In gapped clock mode, the output generated clocks are gapped and gap detection circuitry is needed to identify the required data alignment on the serial inputs.

The TTOC block also allows setting of the Unused and National Use bytes in the SONET/SDH TOH. Specific registers exist to program fixed values in the Z0 bytes and the S1 byte of the TOH. The Remote Error Indication (REI) in the M1 byte may also be manually set via the TTOH input or the error count can be supplied via the TTOHREI input whose pulses are counted to generate an REI error code.

Upon inserting or modification of a transport overhead byte by the TTOC block, the TTOC disables downstream blocks from modifying the same TOH byte again.

		1	2	3	4-12	1	2	3	4-12	1	2	3	4-12
Section	1	A1	A1	A1	A1	A2	A2	A2	A2	J0	Z0	Z0	Z0
	2	B1				E1				F1			
	3	D1				D2				D3			
Line	4	H1	H1	H1	H1	H2	H2	H2	H2	H3	H3	H3	H3
	5	B2	B2	B2	B2	K1				K2			
	6	D4				D5				D6			
	7	D7				D8				D9			
	8	D10				D11				D12			
	9	S1	Z1	Z1	Z1	Z2	Z2	M1	Z2	E2			

National Bytes
Unused Bytes

The National overhead bytes are defined as the following;

- Z0 byte positions of STS-1 #N for 5≤N≤12
- F1 byte positions of STS-1 #N for 2≤N≤12
- E2 byte positions of STS-1 #N for 2≤N≤12

The Unused overhead bytes are defined as the following;

- B1 byte positions of STS-1 #N for 2≤N≤12.
- E1 byte positions of STS-1 #N for 2≤N≤12.
- D1 to D3 byte positions of STS-1 #N for 2≤N≤12.
- K1 and K2 byte positions of STS-1 #N for 2≤N≤12.
- D4 to D12 byte positions of STS-1 #N for 2≤N≤12.
- Z1 bytes of STS-1 #N for 2≤N≤12.
- Z2 bytes of STS-1 #N for N=1, 2 and 4≤N≤12.

11.10 Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor block (TLOP) processes the line overhead of a transmit STS-12 (STM-4) stream.

The TLOP optionally inserts the line data communication channel, the line order wire channel, and the automatic protection switch channel into the line overhead of the transmit stream. In gapped mode these line overhead channels are separately fed to the TLOP as bit serial inputs (TLD, TLOW, and TOH). The TLOP provides the gapped mode bit serial clock for each line overhead channel (TLDCLK, TOWCLK, TOHCLK).

Line RDI may be inserted in the transmit stream under the control of an external input (TLRDI), or a writeable register. The bits in the SPECTRA-622 Line RDI Control Register controls the immediate insertion of Line RDI upon detection of various errors in the received SONET/SDH stream.

Line REI may be inserted automatically in the SONET/SDH stream under the control of the AUTOLREI bit in the SPECTRA-622 Ring Control Register. Receive B2 errors are accumulated and optionally inserted automatically in bits 2 to 8 of the third Z2/M1 byte of the transmit STS-12 (STM-4) stream. Up to 96 errors may be inserted per frame.

The line BIP (B2) error detection code for the transmit stream is calculated by the TLOP and is inserted into the line overhead. Errors may be inserted in the B2 code for diagnostic purposes. A byte serial stream, along with a frame position indicator is passed to the Transmit Section Overhead Processor.

11.11 Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) block processes the section overhead of the transmit STS-12 (STM-4) stream.

The TSOP accepts an unscrambled stream in byte serial format from the Transmit Line Overhead Processor. It optionally inserts the section data communication channel, the order wire channel, and the user channel into the section overhead (regenerator section) of the stream. These section overhead channels are input to the SPECTRA-622 in gapped mode as bit serial signals (TOH, TSLD, TSOW, and TSUC). The TSOP provides the bit serial clock for each section overhead channel (TOHCLK, TSLDCLK, and TOWCLK). The line alarm indication signal may optionally be inserted into the data stream under the control of an external input (TLAIS), or a microprocessor writeable register.

The section BIP-8 error detection code (B1) is calculated by the TSOP block and is inserted into the section overhead of the transmit stream. Errors may be inserted in the B1 code for diagnostic purposes. Framing (A1, A2) and identity bytes (J0) are also inserted. Finally, the complete transmit stream is scrambled and output by the TSOP in byte serial format to the Transmit Line Interface.

The TSOP block is intended to operate with a downstream serializer (the Parallel to Serial Converter block) that accepts the transmit stream in byte serial format and serializes it at the appropriate line rate.

11.12 Transmit Section Trace Buffer (SSTB)

The transmit portion of the SONET/SDH Section Trace Buffer (SSTB) sources the section trace identifier message (J0) for the Transmit Transport Overhead Access block. The length of the trace message is selectable between 16 bytes and 64 bytes. The section trace buffer contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transport

Overhead Access block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, the buffer may be programmed to transmit null characters to prevent transmission of partial messages.

11.13 Transmit Line Interface

The Transmit Line Interface allows to directly interface the SPECTRA-622 with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion on the outgoing 622.08 Mbit/s data stream.

The Transmit Line Interface block performs clock synthesis and performs parallel to serial conversion.The transmit interface also offers a telecom bus parallel output. The parallel interface can be used to output the fully terminated SONET/SDH stream in byte parallel format.

In APS applications the parallel interface may be enabled along with the serial stream output. In this mode the serial stream outputs the fully termainated (section/line) stream while the parallel interface outputs the path terminated stream. The path terminated stream may them be fed into the ADD bus of a second mate SPECTRA622 which can be used to generate the section and line.

11.13.1 Clock Synthesis

The transmit clock may be synthesized from a 77.76 MHz reference. The phase lock loop filter transfer function is optimized to enable the PLL to track the reference, yet attenuate high frequency jitter on the reference signal. This transfer function yields a typical low pass corner of **1** MHz, above which reference jitter is attenuated at **20** dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference, the intrinsic jitter is less than **0.07** UI RMS when measured using a band pass filter with a low cutoff frequency of 12 KHz and a high cutoff frequency of 5 MHz.

The REFCLK reference should be within ±20 ppm to meet the SONET/SDH free-run accuracy requirements specified in GR-253-CORE. The CSU may require a software reset when the supply voltage drops below the minimum operating level. See the CSPI-622 register description for more information.

11.13.2 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD+/- PECL

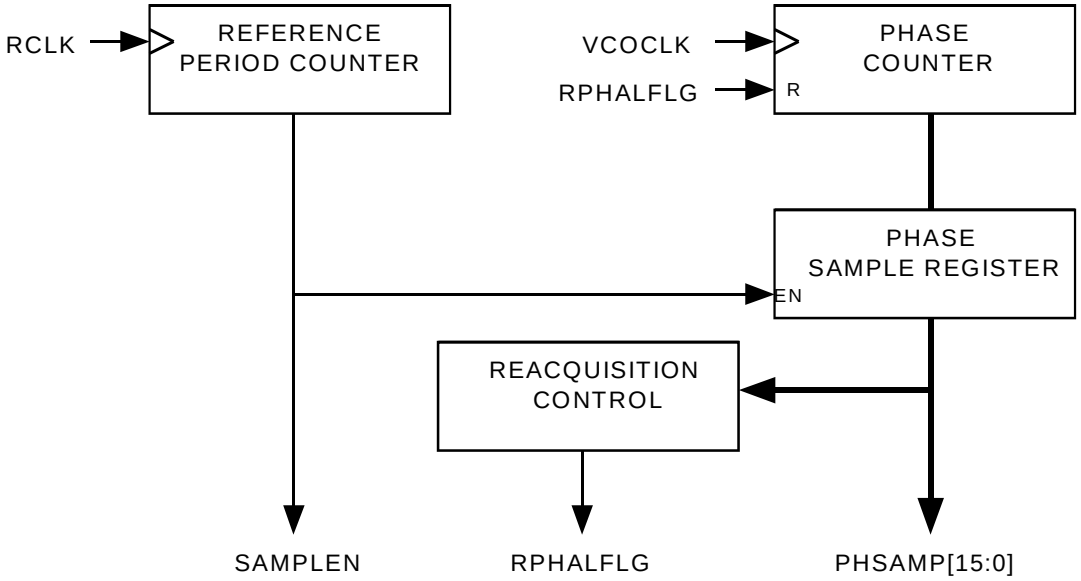
output. When the parallel transmit interface mode is used, the PISO block is not used.

11.14 WAN Synchronization Controller (WANS)

The WANS provides hardware support to implement a local clock reference compliant to SONET Stratum 3 clock specifications (GR-253-CORE & GR-1244-CORE) in wander transfer, long term and holdover stability. The WANS is intended to be used in conjunction with an external processor, DAC, analog circuitry and VCXO. The software running on the external processor is responsible for performing: digital loop filtering, temperature compensation, VCXO linearity compensation; determining the validity of the timing reference; and performing reference switchover if need be. A typical high level representation of a complete PLL is shown below.

The WANS block contains circuitry to implement a digital phase comparison between the reference clock (RCLK) and the variable clock (VCOCLK). It also performs an averaging process of the value obtained.

Figure 14 -Phase Comparator Block Diagram



Phase Comparison

The phase comparison between the reference clock (RCLK) and the variable clock (or VCXO clock, VCOCLK) is implemented by sampling, at a fixed interval, the Reference Period the output of the Phase Counter.

Successive reading of the value obtained, referred as phase sample (PHSAMP), can be used to calculate the phase relation between both clocks. Both the Reference Counter and the Phase Counter are programmable counters and are set to have equal cycle period. Therefore, if VCOCLK were locked to RCLK, successive readings of the phase sample would be equal. The phase sample value will increase or decrease depending if VOCLK is faster or slower than RCLK.

The Reference Period is obtained by dividing RCLK. At each reference period, a signal enabling the sampling (SAMPLEN) of the Phase Counter is produced. This signal is resynchronized to VCOCLK to avoid any potential metastability problem that could result due to the asynchronous nature of both clocks.

Phase Reacquisition Control

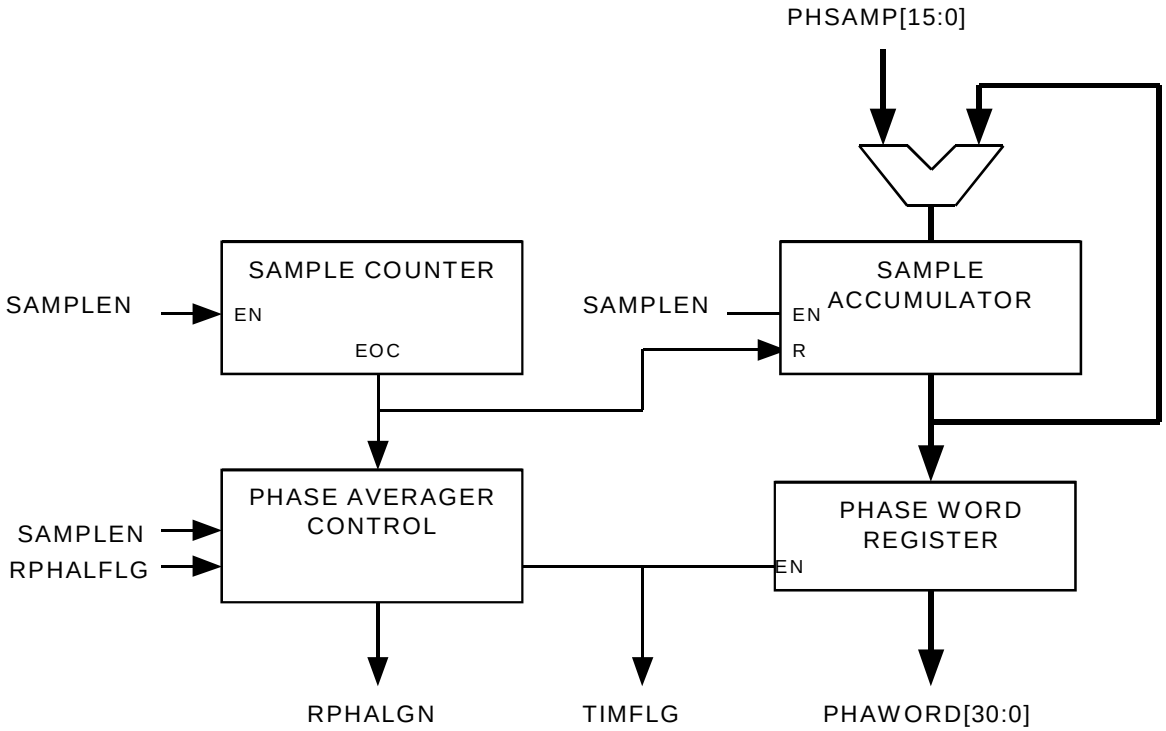
The Phase Reacquisition Control circuit prevents using the phase sample from both sides of the counter wrap-around point when performing the Phase Sample averaging. The Phase Count is first divided in four quadrants, each equal to approximately a quarter of the Phase Count. Comparators are used to determine in which quadrant each phase sample is located. When two successive samples (one in the first quadrant and the other in the last quadrant) are seen, the Reference Phase Alignment Flag (RPHALFLG) is generated.

Upon reception of this signal, the Phase Counter is reset to align the phase count sampling point towards its middle count. This signal is also sent to the Phase Averager circuit. The generation of this signal may be squelched by setting the AUTOREAC bit of the WANS configuration register.

Phase Averager

To provide some noise immunity and improve the resolution of the phase detector algorithm of the WANS, the phase samples are averaged over a programmable number of samples.

Figure 15 -Phase Averager Block Diagram



Although referred to as an averaging process, it is truly an accumulation process. It retains full resolution, i.e. no division is performed on the accumulated value. The Phase Word includes an integer and a fractional part. The number of averaging samples sets the size of the fractional part.

A programmable counter, the Sample Counter, in incremented at each SAMPLEN signal. This Sample Counter defines the Phase Averaging Period, equal to the Reference Period times the programmed number of phase samples. At the end of this period, the accumulated phase sample value is transferred to the Phase Word register. The Phase Word (PHAWORD) is then accessible by an external processor. An internal timer flag is raised at the end of each averaging period. The flag may be used to generate an interrupt request (TIMI) to an external processor.

Because it indicates that the averaging process includes invalid sample values, the RPHALFLG signal also prevents the Phase Word register from being updated at the end of the current Phase Averaging period. The RPHAFLG signal indicates this event by sending the Reference Phase Alignment condition signal (RPHALGN) to the WANS Interrupt and Status register (0081H). The RPHALGN signal is reset at the end of the following valid Phase Averaging period.

11.15 ADD/DROP Bus Time-Slot Interchange (TSI)

The Time-Slot Interchange (TSI) logic at the Telecom ADD and DROP buses supports the grooming of the corresponding receive and transmit SONET/SDH streams by performing column (time-slot) switching in those streams. The ADD or DROP bus TSI logic treats an STS-12 (STM-4) SONET/SDH stream as consecutive blocks consisting of twelve independent time-division multiplexed columns (time-slots) of data. The twelve columns correspond to the twelve constituent STS-1 (STM-0/AU3) or equivalent payload streams. The relationship between the columns and the payload streams is summarized in the “Column#” and “STS-1 (STM-0/AU3) Streams” headings of the association table below. The columns are numbered in the order of transmission (reception) and the corresponding payload streams are labeled according to their STS-3 (STM-1) group and STS-1 (STM-0/AU3) sub-group.

Table 7 -Columns and STS-1 (STM-0/AU3) streams association.

Column # (Tx/Rx Order)	STS-1 (STM-0/AU3) Streams
1	**STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1**
2	STS-3 (STM-1) #2 STS-1 (STM-0/AU3) #1
3	STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #1
4	STS-3 (STM-1) #4 STS-1 (STM-0/AU3) #1
5	**STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #2**
6	STS-3 (STM-1) #2 STS-1 (STM-0/AU3) #2
7	STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #2
8	STS-3 (STM-1) #4 STS-1 (STM-0/AU3) #2
9	**STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #3**
10	STS-3 (STM-1) #2 STS-1 (STM-0/AU3) #3
11	STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #3
12	STS-3 (STM-1) #4 STS-1 (STM-0/AU3) #3

Switching of columns (time-slots) is arbitrary, thus any column can be switched to any of the time-slots. Concatenated streams such as STS-3c (STM-1/AU4) should be switched as a group to keep the constituent STS-1 (STM-0/AU3) streams in the correct transmit or receive order within the group.

On the DROP side, the DROP bus TSI logic grooms the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) receive stream provided by the twelve Receive Path Processing Slices (RPPS) into the corresponding STS-12/12c (STM-4/AU3/AU4/AU4-Xc) or 4xSTS-3/3c (STM-1) DROP bus stream.

Similarly, on the ADD side, the ADD bus TSI logic grooms the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) or 4xSTS-3/3c (STM-1) ADD bus stream provided by the Telecombus Interface into the corresponding STS-12/12c (STM-4/AU3/AU4/AU4-Xc) transmit stream to be processed by the twelve Transmit Path Processing Slices (TPPS).

The software configuration of the ADD or DROP bus TSI logic to perform grooming at the respective ADD or DROP buses is described in the Operations section.

11.16 System Side Interfaces

11.16.1 Telecombus Interface

The Telecombus Interface supports a single (STM-4) 77.76 MHz byte Telecom bus or four (STM-1) 19.44 MHz byte Telecom bus modes. It performs multiplexing and demultiplexing to support STS-12/12c (STM-4/AU3/AU4/AU4-Xc) operations.

For an STS-12/12c (STM-4/AU3/AU4/AU4-Xc) receive stream, the Telecombus interface multiplexes the DROP side data streams from the DROP bus TSI logic at the STS-1 (STM-0/AU3) rate and provides the combined data stream (the groomed receive stream) to the DROP bus configured as a single (STM-4) 77.76 MHz byte Telecom bus or four (STM-1) 19.44 MHz byte Telecom buses. For the STM-4 Telecom bus mode, all four constituent STM-1's (STM-1 #1 - #4) are presented at the single 77.76 MHz DROP bus (DD[7:0]). For the STM-1 byte Telecom bus mode, the DROP bus STM-1 #1, STM-1 #2, STM-1 #3 and STM-1 #4 streams are presented at the DD[7:0], DD[15:8], DD[23:16] and DD[31:24] buses, respectively.

For an STS-12/12c (STM-4/AU3/AU4/AU4-Xc) transmit stream, the Telecombus interface accepts a byte stream from the single (STM-4) 77.76 MHz Telecom ADD bus or four byte streams from the four (STM-1) 19.44 MHz byte Telecom ADD buses. The byte streams are de-multiplexed into twelve STS-1 (STM-0/AU3) equivalent streams and presented to the ADD bus TSI logic for grooming. The groomed ADD bus STS-12 (STM-4) stream is then processed and transmitted. For the STM-4 Telecom bus mode, all four constituent STM-1's (STM-1 #1 - #4) are sourced from the single 77.76 MHz ADD bus (AD[7:0]). For the STM-1 byte Telecom bus modes, the ADD bus STM-1 #1, STM-1 #2, STM-1 #3 and STM-1 #4 streams are sourced from the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] buses, respectively.

In the STM-1 Telecom bus mode, one or more adjacent STM-1 ADD or DROP buses can be grouped together to support concatenated payload streams larger then an STS-3c (STM-1/AU4). On the DROP side, the payload data de-mux'ed onto the STM-1 DROP buses in the group will experience identical delays and thus preserving byte sequencing integrity of the concatenated receive payload stream. The transport frames of the STM-1 DROP buses in the group can be aligned by the DFP frame pulse. On the ADD side, the transport frames of the STM-1 ADD buses in the group must be aligned (coincident C1/AFP pulses on the associated AC1J1V1/AFP signals). The payload data provided on the STM-1 ADD buses in the group will experience identical delays and the byte sequencing integrity of the concatenated transmit payload stream is thus preserved.

The Telecombus is very flexible and can support a wide range of system backplane architectures. Table 8 shows the system side ADD bus options:

Table 8 - System Side ADD Bus Configuration Options

AFPEN Bit	DISJ1V1 Bit	APL[4:1] Input Pin	AC1J1V1[4:1]/ AFP[4:1] Input Pin	Comments
0	0	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block is bypassed.
0	1	Tied to ground	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1
0	1	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block interprets pointers for J1/V1. Ignores J1/V1 indications on AC1J1V1
0	1	APL marks payload bytes	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1

AFPEN Bit	DISJ1V1 Bit	APL[4:1] Input Pin	AC1J1V1[4:1]/ AFP[4:1] Input Pin	Comments
1	X	X	AFP marks first SPE byte position only	TPIP block interprets pointers for J1/V1. Ignores APL input.

Table 9 shows the system side DROP bus options:

Table 9 - System Side DROP Bus Configuration Options

ENDV1	DPL[4:1]	DC1J1V1[4:1]
1	DPL marks payload bytes	DC1J1V1 marks C1, J1 and V1 positions
0	DPL marks payload bytes	DC1J1V1 marks C1 and J1 positions only

11.16.2 Serial DS3 Interface

The Serial DS3 Interface conditions the input and output signals for the D3MA and D3MD blocks. Note, STS-3c (STM-1/AU4) streams in an STS-12 (STM-4/AU3/AU4) and STS-12c (STM-4-4c) streams are not supported by this interface.

For an STS-12 (STM-4/AU3) receive operation using external DS3 framers, twelve independent DS3 interfaces are provided to the twelve D3MD blocks for demapping of DS3 streams from the SONET/SDH receive stream.

For STS-12 (STM-4/AU3) transmit operation using external DS3 framers, twelve independent DS3 interfaces are provided to the twelve D3MA blocks for optional mapping of DS3 streams into the SONET/SDH transmit stream.

For applications which drive a T3 line interface, the de-synchronized DS-3 streams must be de-jittered externally before it can be connected to the line interface.

11.17 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST

instructions are supported. The SPECTRA-622 identification code is 053130CD hexadecimal.

11.18 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the SPECTRA-622. The normal mode registers are used during normal operation to configure and monitor the SPECTRA-622. The test mode registers are used to enhance the testability of the SPECTRA-622. The register set is accessed as shown in Table 10. In the following section every register is documented and identified using the register numbers in Table 10. The corresponding memory map address is identified by the address column of the table. Within each Transmit Path Processing Slices (TPPS) the address mappings are identical. The same is true for the Receive Path Processing Slices (RPPS). The address space of the twelve RPPS registers span the addresses where A[13:12]=0h and A[11:8]=**n**h where 1≤**n**≤12. The address space of the twelve TPPS registers span the addresses where A[13:12]=1h and A[11:8]=**n**h where 1≤**n**≤12. The variable **n** represents the slice number or index. Addresses that are not shown are not used and must be treated as Reserved.

Table 10 -Register Memory Map

REG #	Address A[13:0]	Register Description
0000H	0000H	SPECTRA-622 Reset, Identity and Accumulation Trigger.
0001H	0001H	SPECTRA-622 Line Activity Monitor
0002H	0002H	SPECTRA-622 Line Configuration #1
0003H	0003H	SPECTRA-622 Line Configuration #2
0004H	0004H	SPECTRA-622 Clock Control
0005H	0005H	SPECTRA-622 Receive Line AIS Control
0006H	0006H	SPECTRA-622 Ring Control
0007H	0007H	SPECTRA-622 Line RDI Control
0008H	0008H	SPECTRA-622 Section Alarm Output Control #1
0009H	0009H	SPECTRA-622 Section Alarm Output Control #2
000AH	000AH	Reserved
000BH	000BH	SPECTRA-622 Section/Line Block Interrupt Status
000CH	000CH	SPECTRA-622 Auxiliary Section/Line Interrupt Enable
000DH	000DH	SPECTRA-622 Auxiliary Section/Line Interrupt Status
000EH	000EH	SPECTRA-622 Auxiliary Signal Interrupt Enable

REG #	Address A[13:0]	Register Description
000FH	000FH	SPECTRA-622 Auxiliary Signal Status/Interrupt Status
0010H	0010H	SPECTRA-622 Path Processing Slice Interrupt Status #1
0011H	0011H	SPECTRA-622 Path Processing Slice Interrupt Status #2
0012H	0012H	SPECTRA-622 Path Processing Slice Interrupt Status #3
0013H	0013H	SPECTRA-622 Transmit Telecom Bus Configuration
0014H	0014H	SPECTRA-622 Serial Control Port Status and Control
0015H	0015H	SPECTRA-622 Serial Control Port Interrupt Enable
0016H	0016H	SPECTRA-622 Serial Control Port Interrupt Status
0017-002FH	0017-002FH	Reserved
0030H	0030H	CRSI Configuration and Interrupt
0031H	0031H	CRSI Status
0032H	0032H	CRSI Clock Recovery Control
0033H	0033H	CRSI Clock Training Configuration
0034H	0034H	RSOP Control and Interrupt Enable
0035H	0035H	RSOP Status and Interrupt
0036H	0036H	RSOP Section BIP (B1) Error Count #1
0037H	0037H	RSOP Section BIP (B1) Error Count #2
0038-003Fh	0038-003Fh	Reserved
0040H	0040H	RLOP Control and Status
0041H	0041H	RLOP Interrupt Enable and Status
0042H	0042H	RLOP Line BIP (B2) Error Count #1
0043H	0043H	RLOP Line BIP (B2) Error Count #2
0044H	0044H	RLOP Line BIP (B2) Error Count #3
0045H	0045H	RLOP Line REI Error Count #1
0046H	0046H	RLOP Line REI Error Count #2
0047H	0047H	RLOP Line REI Error Count #3
0048-004Fh	0048-004Fh	Reserved
0050H	0050H	SSTB Section Trace Control
0051H	0051H	SSTB Section Trace Status
0052H	0052H	SSTB Section Trace Indirect Address
0053H	0053H	SSTB Section Trace Indirect Data
0054H	0054H	SSTB Reserved

REG #	Address A[13:0]	Register Description
0055H	0055H	SSTB Reserved
0056H	0056H	SSTB Section Trace Operation
0057H	0057H	SSTB Reserved
0058-005FH	0058-005FH	Reserved
0060H	0060H	RASE Interrupt Enable
0061H	0061H	RASE Interrupt Status
0062H	0062H	RASE Configuration/Control
0063H	0063H	RASE SF Accumulation Period
0064H	0064H	RASE SF Accumulation Period
0065H	0065H	RASE SF Accumulation Period
0066H	0066H	RASE SF Saturation Threshold
0067H	0067H	RASE SF Saturation Threshold
0068H	0068H	RASE SF Declaring Threshold
0069H	0069H	RASE SF Declaring Threshold
006AH	006AH	RASE SF Clearing Threshold
006BH	006BH	RASE SF Clearing Threshold
006CH	006CH	RASE SD Accumulation Period
006DH	006DH	RASE SD Accumulation Period
006EH	006EH	RASE SD Accumulation Period
006FH	006FH	RASE SD Saturation Threshold
0070H	0070H	RASE SD Saturation Threshold
0071H	0071H	RASE SD Declaring Threshold
0072H	0072H	RASE SD Declaring Threshold
0073H	0073H	RASE SD Clearing Threshold
0074H	0074H	RASE SD Clearing Threshold
0075H	0075H	RASE Receive K1
0076H	0076H	RASE Receive K2
0077H	0077H	RASE Receive Z1/S1
0078-007FH	0078-007FH	Reserved
0080H	0080H	WANS Configuration
0081H	0081H	WANS Interrupt and Status
0082H	0082H	WANS Phase Word LSB
0083H	0083H	WANS Phase Word

REG #	Address A[13:0]	Register Description
0084H	0084H	WANS Phase Word
0085H	0085H	WANS Phase Word MSB
0086H	0086H	WANS Reserved
0087H	0087H	WANS Reserved
0088H	0088H	WANS Reserved
0089H	0089H	WANS Reference Period LSB
008AH	008AH	WANS Reference Period MSB
008BH	008BH	WANS Phase Counter Period LSB
008CH	008CH	WANS Phase Counter Period MSB
008DH	008DH	WANS Phase Average Period
008EH	008EH	WANS Reserved
008FH	008FH	WANS Reserved
0090H	0090H	RTOC Overhead Control
0091H	0091H	RTOC AIS Control
0092-0097H	0092-0097H	RTOC Reserved
0098-009FH	0098-009FH	Reserved
00A0H	00A0H	Reserved
00A1H	00A1H	Reserved
00A2H	00A2H	Reserved
00A3H	00A3H	Reserved
00A4H	00A4H	DROP Bus DLL Configuration
00A5H	00A5H	Reserved
00A6H	00A6H	DROP Bus DLL Reset Register
00A7H	00A7H	DROP Bus DLL Control Status
00A8H	00ABH	Reserved
00ACH	00ACH	Reserved
00ADH	00ADH	Reserved
00B0H	00B0H	CSPI Configuration
00B1H	00B1H	CSPI Status
00B2H	00B2H	Reserved
00B3H	00B3H	Reserved
00B4H	00B4H	TSOP Control
00B5H	00B5H	TSOP Diagnostic

REG #	Address A[13:0]	Register Description
00B6-00B7H	00B6-00B7H	TSOP Reserved
00B8H	00B8H	TLOP Control
00B9H	00B9H	TLOP Diagnostic
00BAH	00BAH	TLOP Transmit K1
00BBH	00BBH	TLOP Transmit K2
00B6-00BFH	00B6-00BFH	Reserved
00C0H	00C0H	TTOC Transmit Overhead Output Control
00C1H	00C1H	TTOC Transmit Overhead Byte Control
00C2H	00C2H	TTOC Transmit Z0
00C3H	00C3H	TTOC Transmit S1
00C4-00C7H	00C4-00C7H	TTOC Reserved
0100H	0**n**00H	SPECTRA-622 RPPS Configuration
0102H	0**n**02H	SPECTRA-622 RPPS Path and DS3 Configuration
0110H	0**n**10H	SPECTRA-622 RPPS Path/DS3 AIS Control #1
0111H	0**n**11H	SPECTRA-622 RPPS Path/DS3 AIS Control #2
0114H	0**n**14H	SPECTRA-622 RPPS Path REI/RDI Control #1
0115H	0**n**15H	SPECTRA-622 RPPS Path REI/RDI Control #2
0118H	0**n**18H	SPECTRA-622 RPPS Path Enhanced RDI Control #1
0119H	0**n**19H	SPECTRA-622 RPPS Path Enhanced RDI Control #2
011CH	0**n**1CH	SPECTRA-622 RPPS RALM Output Control #1
011DH	0**n**1DH	SPECTRA-622 RPPS RALM Output Control #2
0128H	0**n**28H	SPECTRA-622 RPPS Path/DS3 Interrupt Status
012CH	0**n**2CH	SPECTRA-622 RPPS Auxiliary Path Interrupt Enable #1
012DH	0**n**2DH	SPECTRA-622 RPPS Auxiliary Path Interrupt Enable #2
0130H	0**n**30H	SPECTRA-622 RPPS Auxiliary Path Interrupt Status #1
0131H	0**n**31H	SPECTRA-622 RPPS Auxiliary Path Interrupt Status #2
0134H	0**n**34H	SPECTRA-622 RPPS Auxiliary Path Status
0150H	0**n**50H	RPOP Status and Control (EXTD=0)
		RPOP Status and Control (EXTD=1)
0151H	0**n**51H	RPOP Alarm Interrupt Status (EXTD=0)
		RPOP Alarm Interrupt Status (EXTD=1)
0152H	0**n**52H	RPOP Pointer Interrupt Status

REG #	Address A[13:0]	Register Description
0153H	0**n**53H	RPOP Alarm Interrupt Enable (EXTD=0)
		RPOP Alarm Interrupt Enable (EXTD=0)
0154H	0**n**54H	RPOP Pointer Interrupt Enable
0155H	0**n**55H	RPOP Pointer LSB
0156H	0**n**56H	RPOP Pointer MSB
0157H	0**n**57H	RPOP Path Signal Label
0158H	0**n**58H	RPOP Path BIP-8 Count LSB
0159H	0**n**59H	RPOP Path BIP-8 Count MSB
015AH	0**n**5AH	RPOP Path REI Count LSB
015BH	0**n**5BH	RPOP Path REI Count MSB
015CH	0**n**5CH	RPOP Tributary Multiframe Status and Control
015DH	0**n**5DH	RPOP Ring Control
015EH	0**n**5EH	RPOP Reserved
015FH	0**n**5FH	RPOP Reserved
0160-016FH	0**n**60-0**n**6FH	RPPS Reserved
0170H	0**n**70H	PMON Reserved
0171H	0**n**71H	PMON Reserved
0172H	0**n**72H	PMON Reserved
0173H	0**n**73H	PMON Reserved
0174H	0**n**74H	PMON Receive Positive Pointer Justification Count
0175H	0**n**75H	PMON Receive Negative Pointer Justification Count
0176H	0**n**76H	PMON Transmit Positive Pointer Justification Count
0177H	0**n**77H	PMON Transmit Negative Pointer Justification Count
0178-017FH	0**n**78-0**n**7FH	RPPS Reserved
0180H	0**n**80H	RTAL Control
0181H	0**n**81H	RTAL Interrupt Status and Control
0182H	0**n**82H	RTAL Alarm and Diagnostic Control
0183H	0**n**83H	RTAL Reserved
0184-018FH	0**n**84-0**n**8FH	RPPS Reserved
0190H	0**n**90H	SPTB Control
0191H	0**n**91H	SPTB Path Trace Identifier Status
0192H	0**n**92H	SPTB Indirect Address

REG #	Address A[13:0]	Register Description
0193H	0**n**93H	SPTB Indirect Data
0194H	0**n**94H	SPTB Expected Path Signal Label
0195H	0**n**95H	SPTB Path Signal Label Status
0196H	0**n**96H	SPTB Path Trace Operation
0197H	0**n**97H	SPTB Reserved
0198-01AFH	0**n**98-0**n**AFH	RPPS Reserved
01B0H	0**n**B0H	D3MD Control
01B1H	0**n**B1H	D3MD Interrupt Status
01B2H	0**n**B2H	D3MD Interrupt Enable
01B3H	0**n**B3H	D3MD Reserved
01B4-01CFH	0**n**B4-0**n**CFH	RPPS Reserved
01D0H	0**n**D0H	DPGM Generator Control #1
01D1H	0**n**D1H	DPGM Generator Control #2
01D2H	0**n**D2H	DPGM Generator Concatenate Control
01D3H	0**n**D3H	DPGM Generator Status
01D4-01D7H	0**n**D4-0**n**D7H	DPGM Reserved
01D8H	0**n**D8H	DPGM Monitor Control #1
01D9H	0**n**D9H	DPGM Monitor Control #2
01DAH	0**n**DAH	DPGM Monitor Concatenate Control
01DBH	0**n**DBH	DPGM Monitor Monitor Status
01DCH	0**n**DCH	DPGM Monitor Error Count #1
01DDH	0**n**DDH	DPGM Monitor Error Count #2
01DE-01DFH	0**n**DE-0**n**DFH	DPGM Reserved
01E0-01FF	0**n**E0-0**n**FFH	RPPS Reserved
0D01H	0D01H	DROP Bus STM-1 #1 AU3 #1 Select
0D02H	0D02H	DROP Bus STM-1 #2 AU3 #1 Select
0D03H	0D03H	DROP Bus STM-1 #3 AU3 #1 Select
0D04H	0D04H	DROP Bus STM-1 #4 AU3 #1 Select
0D05H	0D05H	DROP Bus STM-1 #1 AU3 #2 Select
0D06H	0D06H	DROP Bus STM-1 #2 AU3 #2 Select

REG #	Address A[13:0]	Register Description
0D07H	0D07H	DROP Bus STM-1 #3 AU3 #2 Select
0D08H	0D08H	DROP Bus STM-1 #4 AU3 #2 Select
0D09H	0D09H	DROP Bus STM-1 #1 AU3 #3 Select
0D0AH	0D0AH	DROP Bus STM-1 #2 AU3 #3 Select
0D0BH	0D0BH	DROP Bus STM-1 #3 AU3 #3 Select
0D0CH	0D0CH	DROP Bus STM-1 #4 AU3 #3 Select
0D0D-0D1FH	0D0D-0D1FH	DROP Bus Reserved
0D20-0D2FH	0D20-0D2FH	Reserved
0D30H	0D30H	SPECTRA-622 DROP Bus Configuration
0D31-102FH	0D31-102FH	Reserved
1030H	1030H	SPECTRA-622 ADD Bus Configuration
1031H	1031H	Reserved
1032H	1032H	SPECTRA-622 ADD Bus Parity Interrupt Enable
1033H	1033H	Reserved
1034H	1034H	SPECTRA-622 ADD Bus Parity Status/Interrupt
1035H	1035H	Reserved
1036H	1036H	SPECTRA-622 System Side Clock Activity Monitor
1037H	1037H	SPECTRA-622 ADD Bus Signal Activity Monitor
1038-1060H	1038-1060H	Reserved
1061H	1061H	ADD Bus STM-1 #1 AU3 #1 Select
1062H	1062H	ADD Bus STM-1 #2 AU3 #1 Select
1063H	1063H	ADD Bus STM-1 #3 AU3 #1 Select
1064H	1064H	ADD Bus STM-1 #4 AU3 #1 Select
1065H	1065H	ADD Bus STM-1 #1 AU3 #2 Select
1066H	1066H	ADD Bus STM-1 #2 AU3 #2 Select
1067H	1067H	ADD Bus STM-1 #3 AU3 #2 Select
1068H	1068H	ADD Bus STM-1 #4 AU3 #2 Select
1069H	1069H	ADD Bus STM-1 #1 AU3 #3 Select
106AH	106AH	ADD Bus STM-1 #2 AU3 #3 Select
106BH	106BH	ADD Bus STM-1 #3 AU3 #3 Select
106CH	106CH	ADD Bus STM-1 #4 AU3 #3 Select

REG #	Address A[13:0]	Register Description
106D-10FFH	106D-10FFH	Reserved
1100H	1**n**00H	SPECTRA-622 TPPS Configuration
1101H	1**n**01H	TPPS Reserved
1102H	1**n**02H	SPECTRA-622 TPPS Path and DS3 Configuration
1103-1105H	1**n**03-1**n**05H	TPPS Reserved
1106H	1**n**06H	SPECTRA-622 TPPS Path Transmit Control
1107H	1**n**07H	TPPS Reserved
1108H	1**n**08H	SPECTRA-622 TPPS DS3 Activity Monitor
1109H	1**n**09H	Reserved
1110H	1**n**10H	SPECTRA-622 TPPS Path AIS Control
1109-1127H	1**n**09-1**n**27H	TPPS Reserved
1128H	1**n**28H	SPECTRA-622 TPPS Path/DS3 Interrupt Status
1129-112BH	1**n**29-1**n**2BH	TPPS Reserved
112CH	1**n**2CH	SPECTRA-622 TPPS Auxiliary Path Interrupt Enable
112D-112FH	1**n**2D-1**n**2FH	TPPS Reserved
1130H	1**n**30H	SPECTRA-622 TPPS Auxiliary Path Interrupt Status
1131-114FH	1**n**31-1**n**4FH	TPPS Reserved
1150H	1**n**50H	TPOP Control
1151H	1**n**51H	TPOP Pointer Control
1152H	1**n**52H	TPOP Reserved
1153H	1**n**53H	TPOP Current Pointer LSB
1154H	1**n**54H	TPOP Current Pointer MSB
1155H	1**n**55H	TPOP Payload Pointer LSB
1156H	1**n**56H	TPOP Payload Pointer MSB
1157H	1**n**57H	TPOP Path Trace
1158H	1**n**58H	TPOP Path Signal Label
1159H	1**n**59H	TPOP Path Status
115AH	1**n**5AH	TPOP Path User Channel
115BH	1**n**5BH	TPOP Path Growth #1

REG #	Address A[13:0]	Register Description
115CH	1**n**5CH	TPOP Path Growth #2
115DH	1**n**5DH	TPOP Reserved
115EH	1**n**5EH	TPOP Reserved
115FH	1**n**5FH	TPOP Reserved
1180H	1**n**80H	TTAL Control
1181H	1**n**81H	TTAL Interrupt Status and Control
1182H	1**n**82H	TTAL Alarm and Diagnostic Control
1183H	1**n**83H	TTAL Reserved
1184-118FH	1**n**84-1**n**8FH	TPPS Reserved
1190H	1**n**90H	TPIP Status and Control (EXTD=0)
		TPIP Status and Control (EXTD=1)
1191H	1**n**91H	TPIP Alarm Interrupt Status
1192H	1**n**92H	TPIP Pointer Interrupt Status
1193H	1**n**93H	TPIP Alarm Interrupt Enable (EXTD=0)
		TPIP Alarm Interrupt Enable (EXTD=1)
1194H	1**n**94H	TPIP Pointer Interrupt Enable
1195H	1**n**95H	TPIP Pointer LSB
1196H	1**n**96H	TPIP Pointer MSB
1197H	1**n**97H	TPIP Reserved
1198H	1**n**98H	TPIP Path BIP-8 Count LSB
1199H	1**n**99H	TPIP Path BIP-8 Count MSB
119AH	1**n**9AH	TPIP Reserved
119BH	1**n**9BH	TPIP Reserved
119CH	1**n**9CH	TPIP Tributary Multiframe Status and Control
119DH	1**n**9DH	TPIP BIP Control
119EH	1**n**9EH	TPIP Reserved
119FH	1**n**9FH	TPIP Reserved
11A0-11AFH	1**n**A0-1**n**AF H	TPPS Reserved
11B0H	1**n**B0H	D3MA Control
11B1H	1**n**B1H	D3MA Interrupt Status
11B2H	1**n**B2H	D3MA Interrupt Enable
11B3H	1**n**B3H	D3MA Reserved

REG #	Address A[13:0]	Register Description
11B4-11CFH	1**n**B4-1**n**CFH	TPPS Reserved
11D0H	1**n**D0H	APGM Generator Control #1
11D1H	1**n**D1H	APGM Generator Control #2
11D2H	1**n**D2H	APGM Generator Concatenate Control
11D3H	1**n**D3H	APGM Generator Status
11D4-11D7H	1**n**D4-1**n**D7H	APGM Reserved
11D8H	1**n**D8H	APGM Monitor Control #1
11D9H	1**n**D9H	APGM Monitor Control #2
11DAH	1**n**DAH	APGM Monitor Concatenate Control
11DBH	1**n**DBH	APGM Monitor Monitor Status
11DCH	1**n**DCH	APGM Monitor Error Count #1
11DDH	1**n**DDH	APGM Monitor Error Count #2
11DE-11DFH	1**n**DE-1**n**DFH	APGM Reserved
11EO-1FFFh	11E0-1FFFh	Reserved
	2000H	Master Test
	2001H	Master Test Slice Select
	2002H-3FFFH	Reserved for Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.

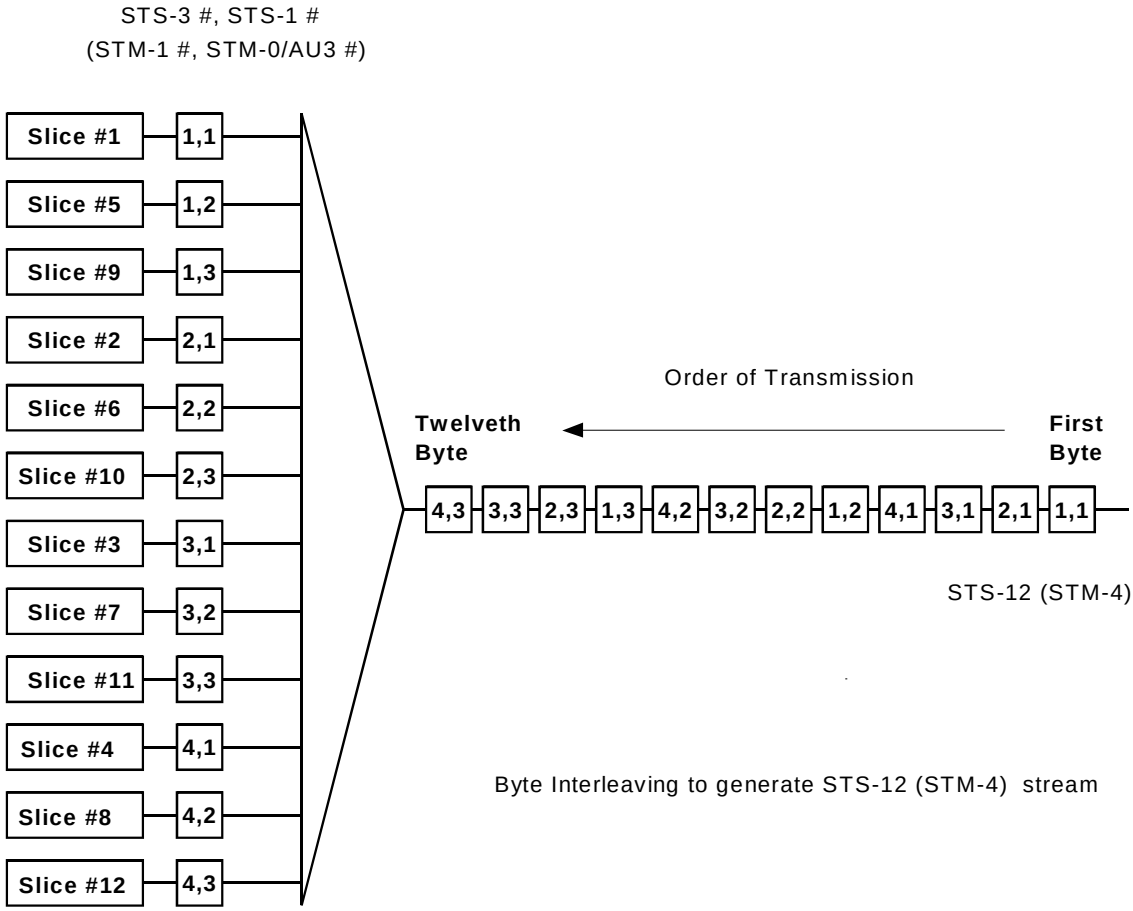
2. Addresses that are not shown must be treated as Reserved.

3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

The Path Processing Slices and Order of Transmission diagram below shows the relationship between the (Transmit/Receive) Path Processing Slices and the corresponding STS-12 (STM-4) SPE (VC) columns or bytes which they process. The SPE (VC) columns or bytes are labeled using an STS-3 (STM-1) group and STS-1 (STM-0/AU3) sub-group numbering scheme. For example, to control the path processing of transmit STS-1 (STM-0/AU3) #1 of the STS-3 (STM-1) #3

stream, the register set of the Transmit Path Processing Slice (TPPS) #7 in the address range of 1700H-17FFH must be used. Similarly, to access the path processing status of the same STS-1 (STM-0/AU3) stream on the receive side, the register set of the Receive Path Processing Slice (RPPS) #7 in the address range of 0700H-07FFH must be accessed.

Figure 16 -Path Processing Slices and Order of Transmission



12 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the SPECTRA-622. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing to unused bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SPECTRA-622 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect SPECTRA-622 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the SPECTRA-622 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0000H: SPECTRA-622 Reset, Identity and Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R/W	RESET_PATH	0
Bit 5	R/W	TIP	X
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision number of the SPECTRA-622 to be read by software permitting graceful migration to newer, feature-enhanced versions of the SPECTRA-622.

In addition, writing to this register initiates a transfer of all performance monitor counter values in the RSOP, RLOP, PMON's, RPOP's, DPGM's and APGM's blocks into holding registers.

ID[4:0]:

The version identification bits ID[4:0], are set to the value 01H, representing the version number of the SPECTRA-622.

TIP:

The Transfer in Progress bit is set to a logic one when the performance meter registers are being loaded. Writing to this register will initiate an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, PMON's, RPOP's, DPGM's and APGM's blocks.
TIP remains high while the transfer is in progress, and is set to logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

RESET_PATH:

The RESET_PATH bit allows the path processing blocks of the SPECTRA-622 to be asynchronously reset under software control. If the RESET_PATH bit is set to logic one, all Transmit Path Processing Slices (TPPS #1 to #12) and all Receive Path Processing Slices (RPPS #1 to #12) are held in reset. This is independent of all other processing blocks. This bit is not self clearing. Therefore, a logic zero must be written to bring the slices out

of reset. A hardware reset clears the RESET_PATH bit, thus negating the software reset. In addition, the following top level registers are also reset: 0100H-0D00H, 1060H and 106DH-1CDDH. When performing a path reset, a TIP will also be generated at the section and line level since it is generated by every write to this register.

RESET:

The RESET bit allows the SPECTRA-622 to be asynchronously reset under software control. If the reset bit is a logic one, the entire SPECTRA-622 is held in reset. This bit is not self clearing. Therefore, a logic zero must be written to bring the SPECTRA-622 out of reset. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset. On every reset, the following operation need to be performed. In order to activate the TX line interface, the TCLK must be enabled for a few clock cycles or the TX bypass mode must be enabled by setting the BYPASS bit in register 1030H. Either of those writes will activate the TX line interface, once done, those bits can be reprogrammed at any value.

Register 0001H: SPECTRA-622 Line Activity Monitor

Bit	Type	Function	Default
Bit 7	R	REFCLKA	X
Bit 6	R	PICLKA	X
Bit 5	R	TDCKA	X
Bit 4	R	PINA	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides activity monitoring on SPECTRA-622 parallel line inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

PINA:

The PIN[7:0] bus data active (PINA) bit monitors for low to high transitions on the PIN[7:0] bus when configured for parallel line mode. PINA is set high when rising edges have been observed on all the signals in the PIN[7:0] bus, and is set low when this register is read.

TDCKA:

The TDCK active (TDCKA) bit monitors activity on the TDCK input to aid in the detection of a loss of clock state. When TDCK makes a low to high transition, the TDCKA bit is set high. The bit will remain high until this register is read at which point the TDCKA bit is cleared. Therefore, a lack of transitions on TDCK is indicated when TDCKA is low. This register should be read at periodic intervals to detect clock failures.

PICLKA:

The PICLK active (PICLKA) bit monitors activity on input PICLK to aid in the detection of a loss of clock state. When PICLK makes a low to high transition, the PICLKA bit is set high. The bit will remain high until this register is read at which point the PICLKA bit is cleared. Therefore, a lack of transitions on PICLK is indicated when PICLKA is low. This register should be read at periodic intervals to detect clock failures.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

Register 0002H: SPECTRA-622 Line Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	SLLE	0
Bit 6	R/W	SDLE	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	PDLE	0
Bit 3	R/W	RBYP	0
Bit 2	R/W	TX_LIFSEL[1]	0
Bit 1	R/W	TX_LIFSEL[0]	0
Bit 0	R/W	RX_LIFSEL	0

This register is used to configure the receive and transmit line side interfaces. Some of the following bits must not be programmed simultaneously.

RX_LIFSEL:

The receive line interface select (RX_LIFSEL) bit selects between serial and parallel receive line interface modes of operation. When RX_LIFSEL is set low, serial mode is selected, enabling clock and data recovery and the SIPO functions. The clock and data recovery may also be bypassed in serial mode via the RBYP register bit. When RX_LIFSEL is set high, the parallel mode is selected, by-passing the clock and data recovery, and the SIPO functions.

TX_LIFSEL[1:0]:

The transmit line interface select (TX_LIFSEL[1:0]) bit selects between serial and parallel transmit line interface modes of operation. For the parallel mode, it also selects the SONET/SDH termination of the transmit stream.

TX_LIFSEL[1:0]	Mode	Termination
00	Serial Transmit Line Interface.	Section,Line and Path
01	Parallel Transmit Line Interface	Section, Line and Path
10	APS MODE: Serial Transmit Line Interface and Parallel Transmit Line Interface	Serial – Section, Line and Path Parallel – Path only
11	Undefined	

In serial transmit mode, clock synthesis and the PISO functions are enabled. The transmit stream is completely terminated with a valid section and line overhead (regenerator and multiplex section overheads). The same is true in APS mode except that the parallel transmit interface is also enabled and supplying path terminated data from after the TX_REMUX. The TSOP, TLOP and TTOC blocks are bypassed for the parallel data.
In parallel mode, the clock synthesis and PISO functions are bypassed and the parallel input clock is used to time the transmit line side. The transmit stream is completely terminated with a valid section and line overhead (regenerator and multiplex section overheads)

RBYP:

The receive bypass (RBYP) bit selects whether to bypass the CRU. When RBYP is set high, the internal CRU is bypassed and RRCLK+/- inputs should contain the line receive clock used to sample RXD+/-. When RBYP is set low, the internal CRU is used and REFCLK+/- should contain the reference clock. The SDLE bit can not be set at the same time as the RBYP bit.

PDLE:

The PDLE bit enables the parallel diagnostic loopback. When PDLE is a logic one, the transmit parallel stream on the TD[7:0] outputs is internally connected to the PIN[7:0] inputs on the receive line side. The PDLE and the SLLE bits should not be set high simultaneously.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK (Clock Synthesis Unit). When LOOPT is a logic one, the transmitter timing is derived from the recovered clock (Clock Recovery Unit). The LOOPT and SLLE bits should not be set high simultaneously,

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream on the TXD+/- differential outputs is internally connected to the received serial RXD+/- differential inputs. The SDLE and the SLLE bit or RBYP bit should not be set high simultaneously.

SLLE:

The SLLE bit enables the SPECTRA-622 line loopback mode when the device is configured for 622.08 Mbit/s serial line interface mode of operation. When SLLE is a logic one, the recovered data from the receive serial RXD+/-

differential inputs is mapped to the TXD+/- differential outputs. The LOOPT and the SLLE bits should not be set high simultaneously. In addition, the SDLE and the SLLE bits should not be set high simultaneously.

Register 0003H: SPECTRA-622 Line Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	FPPOS	0
Bit 3	R/W	TFPWSEL	0
Bit 2	R/W	RFPWSEL	0
Bit 1	R/W	TXDINV	0
Bit 0	R/W	RXDINV	0

This register is used to configure the receive and transmit line side interfaces. The Reserved bits must be set low for proper operation of the SPECTRA-622.

RXDINV:

The receive inversion RXDINV controls the polarity of the receive data. When RXDINV is set high, the polarity of the RXD+/- and PIN[7:0] inputs is inverted. When RXDINV is set low, the RXD+/- and PIN[7:0] inputs operate normally.

TXDINV:

The transmit inversion TXDINV controls the polarity of the transmit data. When TXDINV is set high, the polarity of the TXD+/- is inverted. When TXDINV is set low, the TXD+/- outputs operate normally.

RFPWSEL

The Receive Frame Pulse Width Select is used to set the pulse width of the device RFP output frame pulse pin. Setting this bit to logic zero generates a frame pulse of one RCLK cycle wide. Setting this bit to logic one generates a frame pulse of four RCLK cycles wide.

TFPWSEL

The Transmit Frame Pulse Width Select is used to set the pulse width of the device TFP output frame pulse pin. Setting this bit to logic zero generates a frame pulse of one TCLK cycle wide. Setting this bit to logic one generates a frame pulse of four TCLK cycles wide.

FPPOS

The Frame Pulse Position register bit is used to identify the positioning of the input frame pulse (FPIN) on the receive parallel interface. Setting this bit to

logic zero defines the input frame pulse as identifying the 3rd A2 byte of the received stream on PIN(7:0). Setting this bit to logic one defines the input frame pulse as identify the 1st SPE byte of the received stream on PIN(7:0). NOTE: This bit must be set to logic zero when the CRSI parallel framing is enabled. Framing is enabled setting the PFPEN bit in the CRSI Configuration and Interrupt to the default value of logic zero.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

Register 0004H: SPECTRA-622 Clock Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RCLKEN	0
Bit 4	R/W	TCLKEN	0
Bit 3	R/W	PGMRCLKEN	0
Bit 2	R/W	PGMRCLKSEL	0
Bit 1	R/W	PGMTCLKEN	0
Bit 0	R/W	PGMTCLKSEL	0

This register controls the various line side output clocks generated for the SPECTRA-622.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PGMTCLKSEL:

The PGMTCLKSEL bit selects the clock frequency of the PGMTCLK output. When PGMTCLKSEL is set low, PGMTCLK is a nominally 77.76 MHz clock. When PGMTCLKSEL is set high, PGMTCLK is a nominally 19.44 MHz clock.

PGMTCLKEN:

The PGMTCLK enable (PGMTCLKEN) bit controls gating of the PGMTCLK output. When PGMTCLKEN is set low, the PGMTCLK output is held low. When PGMTCLKEN is set high, the PGMTCLK output is allowed to operate normally.

PGMRCLKSEL:

The PGMRCLKSEL bit selects the clock frequency of the PGMRCLK output. When PGMRCLKSEL is set low, PGMRCLK is a nominally 77.76 MHz clock. When PGMRCLKSEL is set high, PGMRCLK is a nominally 19.44 MHz clock.

PGMRCLKEN:

The PGMRCLK enable (PGMRCLKEN) bit controls gating of the PGMRCLK output. When PGMRCLKEN is set low, the PGMRCLK output is held low. When PGMRCLKEN is set high, the PGMRCLK output is allowed to operate normally.

TCLKEN:

The TCLK enable (TCLKEN) bit controls gating of the TCLK output. When TCLKEN is set low, the TCLK output is held low. When TCLKEN is set high, the TCLK output is allowed to operate normally. TCLK must be enabled in serial mode applications where TFPI will be used. The TFPI input must be set low prior to disabling the TCLK output. After a reset this bit or the TESBYP bit of register 1030H needs to be set for a few clock cycle to activate the TX line interface.

RCLKEN:

The RCLK enable (RCLKEN) bit controls gating of the RCLK output. When RCLKEN is set low, the RCLK output is held low. When RCLKEN is set high, the RCLK output is allowed to operate normally.

Register 0005H: SPECTRA-622 Receive Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDAIS	0
Bit 6	R/W	SFAIS	0
Bit 5	R/W	LOFAIS	1
Bit 4	R/W	LOSAIS	1
Bit 3	R/W	RTIMAIS	0
Bit 2	R/W	RTIUAIS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register enables various section and line alarms to control the insertion of path AIS on the SPECTRA-622 DROP bus.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

RTIUAIS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIUAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of section trace identifier (mode 1 or 2) unstable. If RTIUAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when the SSTB declares a RTIU.. Path AIS is terminated when the RTIU is removed

RTIMAIS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIMAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of section trace identifier (mode 1) mismatch. If RTIMAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when the accepted identifier message differs from the expected message. Path AIS is terminated when the accepted message matches the expected message.

LOSAIS:

The LOSAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of loss of signal (LOS). If LOSAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when LOS is declared. Path AIS is terminated when LOS is removed.

LOFAIS:

The LOFAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of loss of frame (LOF). If LOFAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when LOF is declared. Path AIS is terminated when LOF is removed.

SFAIS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SFAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of signal fail (SF). If SFAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when SF is declared. Path AIS is terminated when SF is removed.

SDAIS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SDAIS bit enables the insertion of path AIS in the DROP direction upon the declaration of signal degrade (SD). If SDAIS is a logic 1, path AIS is inserted into the SONET/SDH frame when SD is declared. Path AIS is terminated when SD is removed.

Register 0006H: SPECTRA-622 Ring Control

Bit	Type	Function	Default
Bit 7	R	INSLRDI	X
Bit 6	R	INSLAIS	X
Bit 5	R/W	RINGEN	0
Bit 4	R/W	AUTOLREI	0
Bit 3	R/W	RCPEN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SLRDI	0
Bit 0	R/W	SLAIS	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

SLAIS:

The SLAIS bit controls the value of the SENDLAIS bit position in the receive ring control port stream. The SLAIS bit is used to cause a mate SPECTRA-622 to send the line AIS maintenance signal under software control.

SLRDI:

The SLRDI bit controls the value of the SENDLRDI bit position in the receive ring control port stream. The SENDLRDI bit value is determined by the logical OR of this register bit along with the line RDI insertion events programmed in the SPECTRA-622 line RDI Control register. The SLRDI bit is used to cause a mate SPECTRA-622 to send the line RDI maintenance signal under software control.

RCPEN:

The RCPEN bit controls the enabling of the receive and transmit ring control ports. When RCPEN is a logic zero, the ring control ports are disabled, and the LOS, LAIS and LRDI outputs and the RLAIS, TLAIS, and TLRDI inputs are used to monitor alarm status and control maintenance signal insertion. When RCPEN is a logic one, the ring control ports are enabled, and alarm status and maintenance signal insertion control is provided by the RRCPCLK, RRCPFP, and RRCPDAT outputs and the TRCPCLK, TRCPFP, and TRCPDAT inputs.

AUTOLREI:

The AUTOLREI bit enables the automatic insertion/indication of line REI events to the mate transmitter (local or remote). When AUTOLREI is a logic one and the local ring control port is disabled, receive B2 errors detected by the SPECTRA-622 are automatically inserted in the Z2/M1 byte of the transmit stream. When AUTOLREI is a logic one and the remote ring control port is enabled, received B2 errors are output on the ring control port for insertion in the Z2/M1 byte of the remote transmit stream.

When AUTOLREI is a logic zero, line REI events are not automatically inserted in the transmit stream nor indicated on the ring control port. A Z2/M1 byte inserted from the transmit transport overhead port (using the TTOHEN input) takes precedence over the automatic insertion of line REI events.

RINGEN:

The RINGEN bit controls the operation of the transmit ring control port when the ring control ports are enabled by the RCPEN bit. When RINGEN is a logic one, the automatic insertion of line RDI, line AIS, and line REI is controlled by bit positions in the transmit ring control port input stream.

When RINGEN is a logic zero, the insertion of line RDI is done automatically based on alarms detected by the receive portion of the SPECTRA-622. Also, line REI is inserted based on B2 errors detected by the receive portion of the SPECTRA-622.

INSLAIS:

The INSLAIS bit reports the value of the SENDLAIS bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA-622 is inserting the line AIS maintenance signal.

INSLRDI:

The INSLRDI bit reports the value of the SENDLRDI bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA-622 is inserting the line RDI maintenance signal.

Register 0007H: SPECTRA-622 Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDLRDI	0
Bit 6	R/W	SFLRDI	0
Bit 5	R/W	LOFLRDI	1
Bit 4	R/W	LOSLRDI	1
Bit 3	R/W	RTIMLRDI	0
Bit 2	R/W	RTIULRDI	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAISLRDI	1

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.LAISLRDI:

The LAISLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of line AIS. When LAISLRDI is a logic 1, the detection of line AIS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIULRDI:

The RTIULRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace identifier (mode 1 or 2) unstable. When RTIULRDI is a logic 1, the detection of section trace identifier (mode 1) unstable results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIMLRDI:

The RTIMLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace identifier (mode 1) mismatch. When RTIMLRDI is a logic 1, the detection of section trace identifier (mode 1) mismatch results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOSLRDI:

The LOSLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of signal. When LOSLRDI is a logic 1, the detection of LOS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOFLRDI:

The LOFLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of frame. When LOFLRDI is a logic 1, the detection of LOF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

SFLRDI:

The SFLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal failure. When SFLRDI is a logic 1, the detection of SF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

SDLRDI:

The SDLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal degrade. When SDLRDI is a logic 1, the detection of SD results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

Register 0008H: SPECTRA-622 Section Alarm Output Control #1

Bit	Type	Function	Default
Bit 7	R/W	SDSALM	0
Bit 6	R/W	SFSALM	0
Bit 5	R/W	LOFSALM	0
Bit 4	R/W	LOSSALM	0
Bit 3	R/W	RTIMSALM	0
Bit 2	R/W	RTIUSALM	0
Bit 1		Reserved	0
Bit 0	R/W	LAISSALM	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.LAISSALM:

The LAISSALM bit allows the line alarm indication signal (LAIS) to be ORed into the SALM output. When the LAISSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the LAISSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

RTIUSALM:

The RTIUSALM bit allows the section trace identifier (mode 1 or 2) unstable (RTIU) alarm indication to be ORed into the SALM output. When the RTIUSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the RTIUSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

RTIMSALM:

The RTIMSALM bit allows the section trace identifier (mode 1) mismatch (RTIM) alarm indication to be ORed into the SALM output. When the RTIMSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the RTIMSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

LOSSALM:

The LOSSALM bit allows the loss of signal (LOS) alarm indication to be ORed into the SALM output. When the LOSSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM.

When the LOSSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

LOFSALM:

The LOFSALM bit allows the loss of frame (LOF) alarm indication to be ORed into the SALM output. When the LOFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the LOFSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

SFSALM:

The SFSALM bit allows the signal fail (SF) alarm indication to be ORed into the SALM output. When the SFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the SFSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

SDSALM:

The SDSALM bit allows the signal degrade (SD) alarm indication to be ORed into the SALM output. When the SDSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the SDSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

Register 0009H: SPECTRA-622 Section Alarm Output Control #2

Bit	Type	Function	Default
Bit 7	R/W	LRDISALM	0
Bit 6	R/W	OOFSALM	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

Reserved:

The Reserved bits must be set to their default values for proper operation of the SPECTRA-622.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.OOFSALM:

The OOFSALM bit allows the out of frame (OOF) alarm indication to be ORed into the SALM output. When the OOFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the OOFSALM bit is set low, the corresponding alarm indication does not affect the SALM output.

LRDISALM:

The LRDISALM bit allows the line remote defect indication (LRDI) to be ORed into the SALM output. When the LRDISALM bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the LRDISALM bit is set low, the corresponding alarm indication does not affect the SALM output.

Register 000BH: SPECTRA-622 Section/Line Block Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SCPII	X
Bit 6	R	WANSI	X
Bit 5	R	CSPII	X
Bit 4	R	RASEI	X
Bit 3	R	CRSII	X
Bit 2	R	RSOPI	X
Bit 1	R	SSTBI	X
Bit 0	R	RLOPI	X

This register allows the source of an active interrupt from a section or line processing block to be identified. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

RLOPI:

The RLOPI bit is set high when one or more of the maskable interrupt sources in the receive line overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RLOP Interrupt Enable and Status Register.

SSTBI:

The SSTBI bit is set high when one or more of the maskable interrupt sources in the section trace buffer has been activated. This register bit remains high until the interrupt is acknowledged by reading the SSTB Section Trace Status Register.

RSOPI:

The RSOPI bit is set high when one or more of the maskable interrupt sources in the receive section overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RSOP Interrupt Status Register.

CRSII:

The CRSII bit is set high when one or more of the maskable interrupt sources in the Clock Recovery Unit or the Serial to Parallel Converter block has been activated. This register bit remains high until the interrupt is acknowledged by reading the CRSI Clock Recovery Control/Status/Interrupt register.

RASEI:

The RASEI bit is set high when one or more of the maskable interrupt sources in the receive APS and synchronization extractor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RASE Interrupt Status Register.

CSPII:

The CSPII bit is set high when one or more of the maskable interrupt sources in the Clock Synthesis or the Parallel to Serial Converter block has been activated. This register bit remains high until the interrupt is acknowledged by reading the CSPI Clock Synthesis Control, Status and Interrupt register.

WANSI:

The WANSI bit is a logic one when an interrupt request is active from the WANS block. The WANS interrupt sources are enabled in the WANS Interrupt Enable/Status Register. This register bit remains high until the interrupt is acknowledged by reading the WANS Interrupt Status register.

SCPII:

The SCPII bit is a logic one when an interrupt request is active from the SCPI input pins. The SCPI interrupt sources are enabled in Serial Control Port Interrupt Enable Register. This register bit remains high until the interrupt(s) is(are) acknowledged by clearing the enabled interrupt bit in the Serial Control Port Interrupt Status register.

Register 000CH: SPECTRA-622 Auxiliary Section/Line Interrupt Enable

Bit	Type	Function	Default
Bit 5	R/W	Reserved	0
Bit 6	R/W	TROOLE	0
Bit 5	R/W	RDOOLE	0
Bit 4	R/W	OOFE	0
Bit 3	R/W	LRDIE	0
Bit 2	R/W	LAISE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	LOSE	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.LOSE:

The loss of signal (LOS) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

LOFE:

The loss of frame (LOF) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

LAISE:

The line alarm indication signal (LAIS) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

LRDIE:

The line remote defect indication (LRDI) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

OOFE:

The out of frame (OOF) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

RDOOLE:

The receive data out of lock (RDOOL) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

TROOLE:

The transmit reference out of lock (TROOL) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

Note, these interrupt enable bits do not affect the actual interrupt bits found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status register.

Register 000DH: SPECTRA-622 Auxiliary Section/Line Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	X
Bit 6	R/W	TROOLI	X
Bit 5	R/W	RDOOLI	X
Bit 4	R/W	OOFI	X
Bit 3	R/W	LRDII	X
Bit 2	R/W	LAISI	X
Bit 1	R/W	LOFI	X
Bit 0	R/W	LOSI	X

The SPECTRA-622 Auxiliary Section/Line Interrupt Status register replicates section and line interrupts that can be found in the CRU, CSU, RSOP and RLOP registers. However, unlike the above interrupt register bits that clear on reads, the SPECTRA-622 Auxiliary Section/Line Interrupt Status register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.LOSI:

The LOSI bit is set high when loss of signal is declared or removed.

LOFI:

The LOFI bit is set high when loss of frame is declared or removed.

LAISI:

The LAISI bit is set high when line LAIS is declared or removed.

LRDII:

The LRDII bit is set high when line RDI is declared or removed.

OOFI:

The OOFI bit is set high when out of frame is declared or removed.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the DOOLV bit of the SPECTRA-622 CRSI Clock Recovery

Control, Status and Interrupt register changes state. DOOLV is a logic one if the divided down recovered clock frequency is not within 488 ppm of the REFCLK frequency or if no transitions have occurred on the RXD+/- inputs for more than 96 bit periods.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the ROOLV bit of the SPECTRA-622 CSPI Clock Synthesis Control, Status and Interrupt register changes state. ROOLV indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK and is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK frequency. The CSU tracks slow rate changes in REFCLK.

Register 000EH: SPECTRA-622 Auxiliary Signal Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SDE	0
Bit 0	R/W	SFE	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.SFE:

The signal fail (SF) interrupt enable bit controls interrupt generation on output INTB by the corresponding SFI in the SPECTRA-622 Auxiliary Signal Status/Interrupt register.

SDE:

The signal degrade (SD) interrupt enable bit controls interrupt generation on output INTB by the corresponding SDI bit in the SPECTRA-622 Auxiliary Signal Status/Interrupt register.

Note, these enable bits do not affect the actual interrupt bits.

Register 000FH: SPECTRA-622 Auxiliary Signal Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	X
Bit 6	R/W	Reserved	X
Bit5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	SDI	X
Bit 0	R/W	SFI	X

This register replicates the receive signal status and interrupts that can be found in the registers of the RASE block. However, unlike the RASE interrupt register bits that clear on reads, the interrupt bits in this register do not clear when read. To clear these register bits, a logic one must be written to the register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.SFI:

The signal fail interrupt (SFI) status bit indicate when the signal fail threshold has been crossed as controlled using RASE registers. This register bit is the same as the SFBERI bit found in the RASE Interrupt Status register with the exception that it does not clear when read. To clear the register bit, a logic one must be written to it.

SDI:

The signal degrade interrupt (SDI) status bit indicate when the signal degrade threshold has been crossed as controlled using RASE registers. This register bit is the same as the SDBERI bit found in the RASE Interrupt Status register with the exception that it does not clear when read. To clear the register bit, a logic one must be written to it.

Register 0010H: SPECTRA-622 Path Processing Slice Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	RPPSI[8] (4,2)	X
Bit 6	R	RPPSI[7] (3,2)	X
Bit5	R	RPPSI[6] (2,2)	X
Bit 4	R	RPPSI[5] (1,2)	X
Bit 3	R	RPPSI[4] (4,1)	X
Bit 2	R	RPPSI[3] (3,1)	X
Bit 1	R	RPPSI[2] (2,1)	X
Bit 0	R	RPPSI[1] (1,1)	X

Register 0011H: SPECTRA-622 Path Processing Slice Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	RPPSI[12] (4,3)	X
Bit 6	R	RPPSI[11] (3,3)	X
Bit5	R	RPPSI[10] (2,3)	X
Bit 4	R	RPPSI[9] (1,3)	X
Bit 3	R	TPPSI[12] (4,3)	X
Bit 2	R	TPPSI[11] (3,3)	X
Bit 1	R	TPPSI[10] (2,3)	X
Bit 0	R	TPPSI[9] (1,3)	X

Register 0012H: SPECTRA-622 Path Processing Slice Interrupt Status #3

Bit	Type	Function	Default
Bit 7	R	TPPSI[8] (4,2)	X
Bit 6	R	TPPSI[7] (3,2)	X
Bit5	R	TPPSI[6] (2,2)	X
Bit 4	R	TPPSI[5] (1,2)	X
Bit 3	R	TPPSI[4] (4,1)	X
Bit 2	R	TPPSI[3] (3,1)	X
Bit 1	R	TPPSI[2] (2,1)	X
Bit 0	R	TPPSI[1] (1,1)	X

The SPECTRA-622 Path Processing Slice Interrupt Status registers (#1, 2 and 3) are used to indicate the interrupt status of the twelve receive and twelve transmit path processing slices. A subsequent read of the SPECTRA-622 RPPS Path and

DS3 Interrupt Status or SPECTRA-622 TPPS Path and DS3 Interrupt Status of the slice in interrupt reveals the source of the interrupt. The index numbers refer to the follow receive and transmit STS-1 (STM-0/AU-3)

Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)
1	(1,1)	5	(1,2)	9	(1,3)
2	(2,1)	6	(2,2)	10	(2,3)
3	(3,1)	7	(3,2)	11	(3,3)
4	(4,1)	8	(4,2)	12	(4,3)

RPPSI[12:1]:

The Receive Path Processing Slice Interrupts (RPPSI[12:1]) are high when an interrupt request is active from the index number receive slice.

TPPSI[12:1]:

The Transmit Path Processing Slice Interrupts (TPPSI[12:1]) are high when an interrupt request is active from the indexed number transmit slice.

Register 0013H: SPECTRA-622 Transmit Telecom Bus Configuration

Bit	Type	Function	Default
Bit 7	R/W	TC1J1V1EN	0
Bit 6	R/W	DISTV1	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ODDPT	0
Bit 1	R/W	INCTPL	0
Bit 0	R/W	INCTC1J1V1	0

This register allows the parity insertion in the Transmit Telecom Bus of the SPECTRA-622 to be configured.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.INCTC1J1V1:

The INTDC1J1V1 bit controls whether the composite timing signal, TC1J1V1, on the Transmit bus is used to calculate the corresponding parity signal, TDP. When INCTC1J1V1 is set high, the parity signal set includes the TC1J1V1 signal. When INCTC1J1V1 is set low, parity is calculated without regard to the state of the corresponding TC1J1V1 signal on the Transmit bus.

INCTPL:

The INCTPL bit controls whether the payload active signal, TPL, on the Transmit bus is used to calculate the corresponding parity signal, TDP. When INCTPL is set high, the parity signal set includes the TPL signal. When INCTPL is set low, parity is calculated without regard to the state of the corresponding TPL signal on the Transmit bus.

ODDPT:

The ODDPT bit controls the parity placed on the Transmit bus parity signal, TDP. When set high, the ODDPT bit configures the bus parity to be odd. When set low, the ODDPT bit configures the bus parity to be even.

DISTV1:

When set high, the DISTV1 bit configures the TC1J1V1 output to mark only the frame and synchronous payload envelope (virtual container) alignments (C1 and J1 bytes). TC1J1V1 will not indicate the tributary multiframe

alignment. When DISTV1 is set low, TC1J1V1 marks all three of the frame, payload envelope and tributary multiframe alignments.

TC1J1V1EN:

The TC1J1V1EN bit enables the transmit Telecom Bus Interface. When TC1J1V1EN is set high, the C1, J1 and optionally the V1 byte positions on the TD[7:0] output are marked by the TC1J1V1/TFPO and the TPL output signals. The corresponding Telecom Bus parity will be provided on the TDP output. When TC1J1V1EN is set low, only the first synchronous payload envelope byte after the J0/Z0 bytes on TD[7:0] will be marked by the TC1J1V1/TFPO output

Register 0014H: SPECTRA-622 Serial Control Port Status and Control

Bit	Type	Function	Default
Bit 7	R/W	SCPO_TS	1
Bit 6	R/W	Reserved	0
Bit 5	R	SCPIV[3]	X
Bit 4	R	SCPIV[2]	X
Bit 3	R	SCPIV[1]	X
Bit 2	R	SCPIV[0]	X
Bit 1	R/W	SCPO[1]	0
Bit 0	R/W	SCPO[0]	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.SCPO[1:0]:

The values written to the SCPO[1:0] bits directly correspond to the states set on the SCPO[1:0] output pins. This provides a generic port useful for controlling up to 2 signals.

SCPO_TS:

The serial control port output tristate bit controls tristating of the SCPO[1:0] outputs. When SCPO_TS is set high, the outputs SCPO[1:0] are tristate. SCPO_TS defaults to logic one so that SCPO[1:0] are tristate after reset.

SCPIV[3:0]:

The serial control port input status (SCPIV[3:0]) bits give the status of the associated SCPI[3:0] input pins. An interrupt may be generated on the rising or falling edge of the input. See the SPECTRA-622 Serial Control Port Interrupt Enable Register.

Register 0015H: SPECTRA-622 Serial Control Port Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	SCPIRE[3]	0
Bit 6	R/W	SCPIRE[2]	0
Bit 5	R/W	SCPIRE[1]	0
Bit 4	R/W	SCPIRE[0]	0
Bit 3	R/W	SCPIFE[3]	0
Bit 2	R/W	SCPIFE[2]	0
Bit 1	R/W	SCPIFE[1]	0
Bit 0	R/W	SCPIFE[0]	0

SCPIFE[3:0]

The SCPIFE[3:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of a falling edge event on the corresponding SCPI[3:0] input activates the interrupt (INTB). When a logic zero is written to these locations, the occurrence of a falling edge event on the corresponding SCPI[1:0] input is inhibited from activating the interrupt.

SCPIRE[3:0]

The SCPIFE[3:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of a rising edge event on the corresponding SCPI[3:0] input activates the interrupt (INTB). When a logic zero is written to these locations, the occurrence of a rising edge event on the corresponding SCPI[1:0] input is inhibited from activating the interrupt.

Register 0016H: SPECTRA-622 Serial Control Port Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	SCPIRI[3]	X
Bit 6	R/W	SCPIRI[2]	X
Bit 5	R/W	SCPIRI[1]	X
Bit 4	R/W	SCPIRI[0]	X
Bit 3	R/W	SCPIFI[3]	X
Bit 2	R/W	SCPIFI[2]	X
Bit 1	R/W	SCPIFI[1]	X
Bit 0	R/W	SCPIFI[0]	X

SCPIFI[3:0]

The SCPIFI[3:0] bits are set high on the the occurrence of a falling edge event on the corresponding SCPI[3:0] input. The interrupt is cleared by writing a logic one to the register bit position. The interrupts may be enabled via the Serial Control Port Interrupt Enable register to generate a device interrupt.

SCPIRI[3:0]

The SCPIRI[3:0] bits are set high on the the occurrence of a rising edge event on the corresponding SCPI[3:0] input. The interrupt is cleared by writing a logic one to the register bit position. The interrupts may be enabled via the Serial Control Port Interrupt Enable register to generate a device interrupt.

Register 0030H: CRSI Configuration and Interrupt

Bit	Type	Function	Default
Bit 7	R/W	SDINV	0
Bit 6	R/W	PFPEN	0
Bit 5	R/W	SENB	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	LOTI	X
Bit 1	R	ROOLI	X
Bit 0	R	DOOLI	X

The CRSI Configuration and Interrupt register is provided to configure the CRU-622 clock recovery PLL and SONET Framer.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

DOOLI:

The DOOLI bit is the data out of lock interrupt status bit. DOOLI is set high when the DOOLV bit changes state, indicating the CRU has either locked to the incoming data stream or has gone out of lock. DOOLI is cleared when this register is read. If the DOOLE interrupt enable is set, the INTB output is also asserted.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV register changes state, indicating the CRU PLL has either locked to the reference clock REFCLK or has gone out of lock. ROOLI is cleared when this register is read. If the ROOLE interrupt enable is logic one, the INTB output is also asserted with ROOLI asserted.

LOTI:

The LOTI bit is the loss of transition interrupt status bit. LOTI is set high when a loss of transition event occurs. A loss of transition is defined as either the SD input set low or more than 96 consecutive ones or zeros received. The consecutive ones or zeros condition may be disabled via the SENB register bit and RSOP used to declare this failure. LOTI is cleared when this register is read. If the LOTE interrupt enable is logic one, the INTB output is also asserted with LOTI asserted.

SENB:

The loss of signal transition detector enable (SENB) bit enables the declaration of loss of transition (LOT) when more than 95 consecutive ones or zeros occurs in the receive data. When SENB is a logic zero, a loss of transition is declared when more than 95 consecutive ones or zeros occurs in the receive data or when the SD input is low. When SENB is a logic one, a loss of transition is declared only when the SD input is low.

PFPEN:

The parallel frame pulse enable (PFPEN) enables the parallel frame pulse operation when the parallel data interface is enabled (LIFSEL set high or PDLE set high). When PFPEN is a logic zero, the input frame pulse is ignored and the SONET framing is performed on the PIN[7:0] data. When PFPEN is a logic one, the SONET framer is ignored and the PIN[7:0] bus is assumed to be byte aligned marked with the input frame pulse (FPIN). PFPEN is ignored when the parallel data interface is disabled.

SDINV:

The signal detect input invert (SDINV) controls the polarity of the SD input. The value of the SD input is logically XOR'ed with the value of the SDINV register. Therefore, when SDINV is a logic zero, valid signal power is indicated by the SD input high. When SDINV is a logic one, valid signal power is indicated by the SD input low.

Register 0031H: CRSI Status

Bit	Type	Function	Default
Bit 7	R	LOCK	X
Bit 6	R	LOTV	X
Bit 5	R	ROOLV	X
Bit 4	R	DOOLV	X
Bit 3		Unused	X
Bit 2	R/W	LOTE	0
Bit 1	R/W	ROOLE	0
Bit 0	R/W	DOOLE	0

The Clock Recovery Status register provides information on the status of the CRU-622 clock recovery.

DOOLE:

The DOOLE bit is an interrupt enable for the recovered data out of lock status. When DOOLE is set to logic one, an interrupt is generated upon assertion and negation events of the DOOLV register. When DOOLE is set low, changes in the DOOL status does not generate an interrupt.

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOLV register. When ROOLE is set low, changes in the ROOL status does not generate an interrupt.

LOTE:

The LOTE bit enables the loss of transition indication interrupt. When LOTE is set high, an interrupt is generated upon assertion events of the LOTV register. When LOTE is set low, changes in the LOTV status does not generate an interrupt.

DOOLV:

The recovered data out of lock status indicates the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is a logic one if the divided down recovered clock frequency is not within 488ppm of the REFCLK frequency or if no transitions have occurred on the RXD input for more than 96 bits.

ROOLV:

The recovered reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the divided down synthesized clock frequency is not within 488ppm of the REFCLK frequency. At startup, ROOLV may remain at logic 1 for several hundred millisecond while the PLL obtains lock. The CRU tracks slow rate changes in REFCLK.

LOTV:

The loss of transition status indicates the receive power is lost or more than 96 consecutive ones or zeros have been received. LOTV is a logic zero if the SD input is high or 96 or less consecutive ones or zeros have been received. LOTV is a logic one if the SD input is low or more than 96 consecutive ones or zeros have been received. The condition of consecutive zeros or ones may be disabled via the SENB register bit of the CRSI and RSOP used to detect this condition.

LOCK:

The CRU reference locking status indicates if the CRU is locking to the reference clock or locking to the receive data. LOCK is a logic zero if the CRU is locking or locked to the reference clock. LOCK is a logic one if the CRU is locking or locked to the receive data. LOCK is invalid if the CRU is not used.

Register 0032H: CRSI Clock Recovery Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RTYPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Clock Recovery Control register provides direct access to the CRU-622 clock recovery circuitry.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

RTYPE:

To optimize the SPECTRA-622 for jitter transfer applications, the RTYPE bit in the CRSI Control register must be set to logic one. To optimize the SPECTRA-622 for jitter tolerance applications, the RTYPE bit in the CRSI Control register must be set to logic zero.

Register 0033H: CRSI Clock Training

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	OUTDATA	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved:

The Reserved bits must be set to their default values for proper operation of the SPECTRA-622.

OUTDATA

This bit must be set to one for proper operation of the CRSI. This has to be done only once right after every software or hardware reset.

Register 0034H: RSOP Control and Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is a logic one, a section interrupt is generated when the out-of-frame alarm is declared or removed.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is a logic one, a section interrupt is generated when the loss of frame alarm is declared or removed.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is a logic one, a section interrupt is generated when the loss of signal alarm is declared or removed.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 (B1) errors. When BIPEE is a logic one, a section interrupt is generated when a section BIP-8 error is detected.

ALGO2:

The ALGO2 bit selects the framing algorithm used to confirm and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing

algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:

The FOOF bit is used to force the RSOP out-of-frame. When a logic one is written to the FOOF bit location, the SPECTRA-622 is forced out-of-frame at the next frame boundary, for only one frame. The out-of-frame event results in the assertion of the OOFV register bit. The FOOF bit is defined as write only and the reading of this bit is undefined.

DDS:

The DDS bit is used to disable the descrambling of the received stream. When a logic one is written to the DDS bit position, the descrambler is disabled. When a logic zero is written to the DDS bit position, the descrambler is enabled.

BLKBIP:

The BLKBIP bit enables the accumulating of section block BIP errors. When set to logic one, one or more errors in the section BIP-8 byte (B1) results in a single error accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register 0035H: RSOP Status and Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is set high when out of frame is declared. OOFV is set high and out-of frame declared while the SPECTRA-622 is unable to find a valid framing pattern (A1, A2) in the incoming stream. OOF is removed when a valid framing pattern is detected. This alarm indication is also available on SPECTRA-622 OOF and SALM outputs.

LOFV:

The LOFV bit is set high when loss of frame is declared. LOFV is set high and loss of frame declared when an out-of-frame state persists for 3 ms. LOF is removed when an in frame state persists for 3 ms. This alarm indication is also available on the SPECTRA-622 LOF and SALM outputs.

LOSV:

The LOSV bit is set high when loss of signal is declared. LOSV is set high and loss of signal declared when 20 ± 2.5 µs of consecutive all zeros patterns is detected in the incoming stream. LOS is removed when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. This alarm indication is also available on the SPECTRA-622 LOS/RRCPFP and SALM outputs.

OOFI:

The OOFI bit is set high when out of frame is declared or removed. This bit is cleared when this register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

LOFI:

The LOFI bit is set high when loss of frame is declared or removed. This bit is cleared when this register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

LOSI:

The LOSI bit is set high when loss of signal is declared or removed. This bit is cleared when this register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

BIPEI:

The BIPEI bit is set high when a section BIP error is detected. This bit is cleared when the RSOP Interrupt Status Register is read.

Register 0036H: RSOP Section BIP (B1) Error Count #1

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0037H: RSOP Section BIP (B1) Error Count #2

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15] through SBE[0] represent the number of section BIP-8 parity (B1) errors (individual or block) that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-622 Reset, Identity and Accumulation Trigger Register. Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RSOP B1 Error Count Registers may be read.

Register 0040H: RLOP Control and Status

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	LAISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	BLKREI	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is set high when line Remote Defect Indication (RDI) is detected. Line RDI is detected when a 110 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LRDIDET bit in this register). Line RDI is removed when any pattern other than 110 is detected for three or five consecutive frames. This alarm indication is also available on the SPECTRA-622 LRDI/RRCPCLK and SALM outputs.

LAISV:

The LAISV bit is set high when line Alarm Indication Signal (AIS) is detected. Line AIS is detected when a 111 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LAISDET bit in this register). Line AIS is removed when any pattern other than 111 is detected for three or five consecutive frames. This alarm indication is also available on the SPECTRA-622 LAIS/RRCPDAT and SALM outputs.

BLKREI:

The BLKREI (Block REI) bit controls the accumulation of REI's. When BLKREI is logic 1, and the REI has a value between 1 and 4, the REI event counter is incremented for each set REI bit. If the REI has value greater than 4, and is valid, the REI counter is only incremented by 4. When BLKREI is logic 0, the REI event counter is incremented for each and every REI bit that occurs during that frame. The counter may be incremented up to 96 times.. The REI counter is not incremented for invalid REI codewords.

BLKBIPO:

The BLKBIPO (Block BIP Out) bit controls the indication of line BIP (B2) errors reported to the TLOP and RRCP blocks for insertion as REI. When BLKBIPO is logic one, one BIP error is indicated per frame whenever one or more B2 bit errors occur during that frame. When BLKBIPO is logic zero, a BIP error is indicated for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BLKBIP register bit.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6,7 and, 8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

LAISDET:

The LAISDET bit determines the line AIS alarm detection algorithm. When LAISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6,7 and,8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LAISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically overwriting the SONET/SDH frame with all-ones whenever line AIS is detected. When ALLONES is set to logic one, the SONET/SDH frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the SONET/SDH frame is immediately returned to carrying the receive stream. When ALLONES is set to logic zero, the outputs carry the receive stream regardless of the state of the line AIS alarm.

BLKBIP:

The BLKBIP (Block Bip) bit controls the accumulation of B2 errors. When BLKBIP is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When

BLKBIP is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 96 times per frame).

Register 0041H: RLOP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 7	R/W	LREIE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	LREII	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the remote defect indication interrupt status bit. LRDII is set high when line RDI is declared or removed. This bit is cleared when this register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

LAISI:

The LAISI bit is the alarm indication signal interrupt status bit. LAISI is set high when line LAIS is declared or removed. This bit is cleared when this register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

BIPEI:

The BIPEI bit is the line BIP-96 interrupt status bit. BIPEI is set high when a line BIP error is detected. This bit is cleared when this register is read.

LREII:

The LREII bit is the remote error indication status bit. LREII is set high when a line REI error is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the remote defect indication alarm. When LRDIE is a logic one, a line interrupt is generated when line RDI is declared or removed.

LAISE:

The LAIS bit is an interrupt enable for the line alarm indication signal.. When LAISE is a logic one, a line interrupt is generated when line AIS is declared or removed.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-96 errors. When BIPEE is a logic one, a line interrupt is generated when a line BIP-96 error (B2) is detected.

LREIE:

The LREIE is an interrupt enable for the line remote error indications. When LREIE is a logic one, a line interrupt is generated when a line REI indication is detected.

Register 0042H: RLOP Line BIP (B2) Error Count #1

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0043H: RLOP Line BIP (B2) Error Count #2

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0044H: RLOP Line BIP (B2) Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]:

Bits LBE[19:0] represent the number of line bit-interleaved parity errors (individual or block) that have been detected since the last accumulation

interval. The error counters are polled by writing to any of the RLOP B2 Error Count or the RLOP REI Error Count registers along with writing to the SPECTRA-622 Reset, Identify and Accumulation Trigger Register. Such writes transfer the internally accumulated error count to these registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RLOP B2 Error Count Registers may be read.

Register 0045H: RLOP REI Error Count #1

Bit	Type	Function	Default
Bit 7	R	LREI[7]	X
Bit 6	R	LREI[6]	X
Bit 5	R	LREI[5]	X
Bit 4	R	LREI[4]	X
Bit 3	R	LREI[3]	X
Bit 2	R	LREI[2]	X
Bit 1	R	LREI[1]	X
Bit 0	R	LREI[0]	X

Register 0046H: RLOP REI Error Count #2

Bit	Type	Function	Default
Bit 7	R	LREI[15]	X
Bit 6	R	LREI[14]	X
Bit 5	R	LREI[13]	X
Bit 4	R	LREI[12]	X
Bit 3	R	LREI[11]	X
Bit 2	R	LREI[10]	X
Bit 1	R	LREI[9]	X
Bit 0	R	LREI[8]	X

Register 0047H: RLOP REI Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LREI[19]	X
Bit 2	R	LREI[18]	X
Bit 1	R	LREI[17]	X
Bit 0	R	LREI[16]	X

LREI[19:0]:

Bits LREI[19:0] represent the number of line remote error indications (individual or block) that have been detected since the last accumulation

interval. The error counters are polled by writing to any of the RLOP B2 Error Count or the RLOP REI Error Count registers along with writing to the SPECTRA-622 Reset, Identify and Accumulation Trigger Register. Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RLOP REI Error Count Registers may be read.

Register 0050H: SSTB Section Trace Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUE	0
Bit 4	R/W	RTIME	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes. When LEN16 is set high, the section trace message length is 16 bytes. When LEN16 is set low, the section trace message length is 64 bytes.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, the RTIM and RTIV alarms are invalid and may cause spurious interrupts.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer are ignored and all-zeros bytes are optionally inserted into the J0 byte. When TNULL is set low the contents of the transmit section trace buffer is optionally inserted into the J0 byte. . TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIME:

The receive section trace identifier (mode 1) mismatch interrupt enable bit (RTIME) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIME is set high, changes in match state activates the interrupt (INTB) output. When RTIME is set low, section trace identifier (mode 1) state changes will not affect INTB. This bit is should be disabled in Trace identifier Mode 2 since the RTIM is generate using the Mode 1 algorithm.

RTIUE:

The receive section trace identifier (mode 1) unstable interrupt enable bit (RTIUE) controls the activation of the interrupt output when the receive identifier message state (RTIUV) changes from stable to unstable and vice versa. State changes dependent on the Trace Identifier Mode When RTIUE is set high, changes in the receive section trace identifier unstable (RTIUV) state will activate the interrupt (INTB) output. When RTIUE is set low, section trace identifier unstable state changes will not affect INTB.

TIMODE**:**

The Trace Identifier Mode is used to set the mode for the received section trace identifier. Setting this bit to low sets the Trace Identifier Mode to Mode 1. In this mode the section trace identifier is defined as a regular 16 or 64 byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message. Setting this bit to high sets the Trace Identifier Mode to Mode2. In this mode the section trace identifier is defined as a 16 byte message with a single repeating byte that is monitored for persistency and errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more byte errors are detected in three consecutive 16 byte windows. RTIM is not defined in this mode.

ZEROEN:

The zero enable bit (ZEROEN) is defined for Trace Identifier Mode 1 only and enables trace identifier mismatch (RTIM) assertion and removal based on an

all ZEROs section trace message string. When ZEROEN is set high, all ZEROs section trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs section trace message strings are ignored. Trace identifier unstable (RTIU) assertion and removal is not affected by setting this register bit.

Register 0051H: SSTB Section Trace Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace identifier status.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

RTIMV:

The receive section trace identifier mismatch status bit (RTIMV) is set high in Trace Identifier Mode 1 when the accepted message differs from the expected message. The accepted message is the last message to have been received 5 times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted section trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN register bit in the Control register is set. This bit is usually ignored in Trace Identifier Mode 2.

RTIMI:

The receive trace identifier mismatch indication status bit (RTIMI) is set high in Trace Identifier Mode 1 when the match/mismatch status (RTIMV) of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read. This bit is usually ignored in Trace Identifier Mode 2.

RTIUV:

The receive section trace identifier unstable status bit (RTIUV) is dependent on the Trace Identifier Mode. In Mode 1, the bit is set high when 8 trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected. The unstable

counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (3 or 5 consecutive matching messages). RTIUV is set high when the unstable counter reaches 8. RTIUV is set low and the unstable counter cleared once a persistent message has been received.
In Mode 2, RTIUV is set low during the stable state which is declared after having received the same 16 byte trace message 3 consecutive times (stable trace byte for forty-eight consecutive frames). The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected in three consecutive 16 byte windows. The 16 byte windows do not overlap and start immediately upon the first detected error.

RTIUI:

The receive section trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state. The setting of this bit is dependent on the unstable status (RTIUV) which is dependent on the Trace Identifier Mode. This bit and the interrupt are cleared when this register is read.

Register 0052H: SSTB Section Trace Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. If RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the address specified.

A[7:0]:

The indirect read address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J0 byte of the transmit stream. Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 191 reference the receive capture page while addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

A[7:0]	RAM Contents
0-3Fh	Transmit Trace Message
40h-7Fh	Receive Accepted Trace Message
80h-BFh	Receive Captured Trace Message
C0-FFh	Receive Expected Trace Message

Register 0053H: SSTB Section Trace Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 0056H: SSTB Section Trace Operation

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. The access will be performed when the SSTB Indirect Address register is written to.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to the path trace RAM has been completed. BUSY is set high upon writing to the SSTB Path Trace Indirect Address register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the SSTB Indirect Data register. The maximum latency for the BUSY to return low is 10 us.

Register 0060H: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1/S1E:

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 0061H: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read. A clear on write version of this register bit may be found in the SPECTRA-622 Auxiliary Section/Line Interrupt Status Registers.

Z1/S1I:

The Z1/S1I bit is set high when a new synchronization status message has been extracted into the RASE Receive Z1/S1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the RASE Receive K1 and RASE Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 0062H: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Unused	X

SDCMODE:

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic 0 the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic 1 the RASE clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic 0 the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic 1 the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.
All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic 0 the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic 1 the RASE clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic 0 the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic 1 the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.
All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP:

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for eight consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Register 0063H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 0064H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 0065H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the

SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 0066H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 0067H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 0068H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 0069H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 006AH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 006BH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 006CH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 006DH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 006EH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the

SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 006FH: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 0070H: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 0071H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 0072H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0073H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 0074H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 0075H: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0076H: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0077H: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	Z1/S1[7]	X
Bit 6	R	Z1/S1[6]	X
Bit 5	R	Z1/S1[5]	X
Bit 4	R	Z1/S1[4]	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]:

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable Register). In addition, debouncing can be performed where the register is not loaded until eight of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP bit in the RASE Configuration/Control register.

Z1/S1[7:4]:

The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble. In addition, when the Z1/S1_CAP3 bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when three of the same consecutive lower nibbles are received.

Register 0080H: WANS Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FORCEREAC	0
Bit 2	R/W	AUTOREAC	0
Bit 1	R/W	TIME	0
Bit 0	R/W	PHACOMPEN	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PHACOMPEN:

The Phase Comparison Enable (PHACOMPEN) bit is used to enable the phase comparison process. Setting this bit to a logic 1 will enable the phase comparison process. When set to logic 0, the phase and reference period counters are kept in reset state, further disabling the PLL process

TIME:

The Timer Interrupt Enable (TIME) bit controls the generation of the interrupt signal. When set to logic 1, this bit allows the generation of an interrupt signal at the end of the Phase Detector averaging period. Setting this bit to logic 0 disable the generation of the interrupts but not the TIMI bit itself.

AUTOREAC:

The Auto Reacquisition Mode Select (AUTOREAC) bit can be used to set the WANS to automatic phase reacquisition mode. When operating in this mode, the WANS will automatically align the phase sampling point toward the middle of the Phase Counter period upon detection of two consecutive Phase Sample located on each side of the Phase Counter wrap around value. Setting this bit to logic enables the automatic reacquisition mode.

FORCEREAC:

The Force Phase Reacquisition (FORCEREAC) bit can be used to force a phase reacquisition of the Phase Detector. A logic 0 to logic 1 transition on this bit triggers a phase reacquisition sequence of the Phase Detector. Setting this bit to logic 0 allows the Phase detector to operate normally.

Register 0081H: WANS Interrupt and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RPHALGN	X
Bit 0	R	TIMI	X

TIMI:

The Timer Interrupt (TIMI) bit indicates a Timer Interrupt condition. This bit will be raised at the end of the Phase Detector averaging period. In addition of indicating the interrupt status, this bit can also be polled to implement synchronization of read access to WANS output register. The propagation of the TIMI condition to the interrupt pin INTB can be masked using the TIME bit of the configuration register. A read access to the Interrupt & Status Register resets the value of this bit.

RPHALGN:

The Reference Phase Alignment (RPHALNG) bit indicates a Reference Phase Alignment event. In normal operating mode, this bit remains to logic 0. Upon the occurrence of a Reference Phase Alignment, this bit is set to logic one, indicating that the phase averaging process was aborted and that the value of the Phase Word register is frozen to the previous valid value. This bit is reset to logic 0 after the completion of a valid phase averaging cycle.

Register 0082H: WANS Phase Word LSB

Bit	Type	Function	Default
Bit 7	R	PHAWORD[7]	X
Bit 6	R	PHAWORD[6]	X
Bit 5	R	PHAWORD[5]	X
Bit 4	R	PHAWORD[4]	X
Bit 3	R	PHAWORD[3]	X
Bit 2	R	PHAWORD[2]	X
Bit 1	R	PHAWORD[1]	X
Bit 0	R	PHAWORD[0]	X

Register 0083H: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[15]	X
Bit 6	R	PHAWORD[14]	X
Bit 5	R	PHAWORD[13]	X
Bit 4	R	PHAWORD[12]	X
Bit 3	R	PHAWORD[11]	X
Bit 2	R	PHAWORD[10]	X
Bit 1	R	PHAWORD[9]	X
Bit 0	R	PHAWORD[8]	X

Register 0084H: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[23]	X
Bit 6	R	PHAWORD[22]	X
Bit 5	R	PHAWORD[21]	X
Bit 4	R	PHAWORD[20]	X
Bit 3	R	PHAWORD[19]	X
Bit 2	R	PHAWORD[18]	X
Bit 1	R	PHAWORD[17]	X
Bit 0	R	PHAWORD[16]	X

Register 0085H: WANS Phase Word MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PHAWORD[30]	X
Bit 5	R	PHAWORD[29]	X
Bit 4	R	PHAWORD[28]	X
Bit 3	R	PHAWORD[27]	X
Bit 2	R	PHAWORD[26]	X
Bit 1	R	PHAWORD[25]	X
Bit 0	R	PHAWORD[24]	X

PHAWORD[30:0]:

The Phase Word (PHAWORD[30:0]) bits are the output bus of the Phase Detector. This bus outputs the result of the Phase Count Averaging function. Depending on the number of samples included in the averaging, from 0 to 15 of the LSB(s) of the PHAWORD bus may represent the fractional part of the average value while the 16 following bits hold the integer part. This value can be used to externally implement in software the PLL filtering function and bypass the Digital Loop Filter block.

Register 0089H: WANS Reference Period LSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[7]	0
Bit 6	R/W	REFPER[6]	0
Bit 5	R/W	REFPER[5]	0
Bit 4	R/W	REFPER[4]	0
Bit 3	R/W	REFPER[3]	0
Bit 2	R/W	REFPER[2]	0
Bit 1	R/W	REFPER[1]	0
Bit 0	R/W	REFPER[0]	0

Register 008AH: WANS Reference Period MSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[15]	0
Bit 6	R/W	REFPER[14]	0
Bit 5	R/W	REFPER[13]	0
Bit 4	R/W	REFPER[12]	0
Bit 3	R/W	REFPER[11]	0
Bit 2	R/W	REFPER[10]	0
Bit 1	R/W	REFPER[9]	0
Bit 0	R/W	REFPER[8]	0

REFPER[15:0]:

The Reference Period REFPER[15:0] bits are used to program the timing reference period of the Phase Detector. These bits are used to set the end of count of the Reference Period Counter. The Reference Period Counter is reset on the next clock cycle following the detection of its end of count. The Reference Period Counter counts (Nref) is equal to the REFPER value plus 1.

Nref = REFPER + 1

Register 008BH: WANS Phase Counter Period LSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[7]	0
Bit 6	R/W	PHCNTPER[6]	0
Bit 5	R/W	PHCNTPER[5]	0
Bit 4	R/W	PHCNTPER[4]	0
Bit 3	R/W	PHCNTPER[3]	0
Bit 2	R/W	PHCNTPER[2]	0
Bit 1	R/W	PHCNTPER[1]	0
Bit 0	R/W	PHCNTPER[0]	0

Register 008CH: WANS Phase Counter Period MSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[15]	0
Bit 6	R/W	PHCNTPER[14]	0
Bit 5	R/W	PHCNTPER[13]	0
Bit 4	R/W	PHCNTPER[12]	0
Bit 3	R/W	PHCNTPER[11]	0
Bit 2	R/W	PHCNTPER[10]	0
Bit 1	R/W	PHCNTPER[9]	0
Bit 0	R/W	PHCNTPER[8]	0

PHCNTPER[15:0]:

The Phase Counter Period (PHCNTPER15:0]) bits are used to program the Phase Counter period of the Phase Detector. These bits are used to set the end of count of the Phase Counter. The Phase Counter is reset on the next clock cycle following the detection of its end of count. The Phase Counter count (Nphcnt) is equal to the PHCNTPER value plus 1.

Nphcnt = PHCNTPER + 1

For the system to operate properly, Nphcnt need to be greater than 1023.

Register 008DH: WANS Phase Average Period

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	AVGPER[3]	0
Bit 2	R/W	AVGPER[2]	0
Bit 1	R/W	AVGPER[1]	0
Bit 0	R/W	AVGPER[0]	0

AVGPER[3:0]:

The Phase Average Period (AVGPER [3:0]) bits are used to set the number of consecutive valid Phase Samples accumulated together to form the Phase Word. The number of samples is expressed as a power of 2, i.e.:

$$Navg = 2^{AVGPER}$$

To avoid abnormal behavior of the WANS, the AVGPER value should be programmed into the WANS prior to enabling the phase comparison process (setting the PHACOMPEN bit to logic 1).

Register 0090H: RTOC Overhead Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	X
Bit 6	R/W	RX_GAPSEL	0
Bit 5	R/W	ROH_TS	1
Bit 4	R/W	ROH_SEL[1]	0
Bit 3	R/W	ROH_SEL[0]	0
Bit 2	R/W	RLD_TS	1
Bit 1	R/W	RSLD_TS	1
Bit 0	R/W	RSLDSEL	0

The RTOC Control Register is used to control the receive section and line overhead outputs of the SPECTRA-622.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

RSLDSEL:

The receive data section or line select (RSLDSEL) bit determines the contents of the outgoing RSLD stream. When RSLDSEL is low, the RSLD stream contains the section DCC (D1-D3). When RSLDSEL is high, the RSLD stream contains the line DCC (D4-D12).

RSLD_TS:

The register bit can be used to control the tri-stating of the RSLD and RSLDCLK outputs. Setting RSLD_TS to logic one tri-states the outputs. Setting this bit to logic zero allows normal functioning. RSLD_TS defaults to logic one so that RSLD and RSLDCLK would be tri-stated after reset.

RLD_TS:

The register bit can be used to control the tri-stating of the RLD and RLDCLK outputs. Setting RLD_TS to logic one tri-states the outputs. Setting this bit to logic zero allows normal functioning. RSLD_TS defaults to logic one so that RLD and RLDCLK would be tri-stated after reset.

ROHSEL[1:0]:

The receive overhead select (ROHSEL[1:0]) bus determines the contents of the out going ROH stream and the frequency of the ROHCLK. The decoded ROHSEL settings are listed below.

ROHSEL[1:0]	Contents	ROHCLK
00	Section Order Wire (E1)	Nominal 64 kHz
01	Section User Channel (F1)	Nominal 64 kHz
10	Line Order Wire (E2)	Nominal 64 kHz
11	APS Bytes (K1/K2)	Nominal 128 kHz

ROH_TS:

The register bit can be used to control the tri-stating of the ROH, RFPO and ROHCLK outputs. Setting ROH_TS to logic one tri-states the outputs. Setting this bit to logic zero allows normal functioning. The bit defaults to logic one so that ROH, RFPO and ROHCLK would be tri-stated after reset.

RX_GAPSEL:

The Receive Gap Select (RX_GAPSEL) bit controls the clocking mode for the RSOW, RLOW, RSUC, ROH, RSLD and RLD serial outputs. Setting this bit to logic 0 selects the serial streams to be output with smooth and continuous clocks (ROWCLK, ROHCLK, RSLDCLK and RLDCLK). The RTOHFP may also sampled by these clocks to identify the MSB of each serial stream. Setting this bit to logic one selects a gapped serial output. Gap detection is needed to identify the start of a new overhead on each serial stream.

Register 0091H: RTOC AIS Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LINE_AISEN(2)	0
Bit 4	R/W	LINE_AISEN(1)	0
Bit 3	R/W	LINE_AISEN(0)	0
Bit 2	R/W	SECT_AISEN(2)	0
Bit 1	R/W	SECT_AISEN(1)	0
Bit 0	R/W	SECT_AISEN(0)	0

The RTOC AIS Control Register is provided to explicitly force the receive section and line overhead outputs.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

SECT_AISEN(2:0):

The SECT_AISEN(2:0) bits enable the explicit insertion of all ones on RSOW, RSUC, ROH, RSLD when carrying section DCC and the section overhead on RTOH. Each bit enables a separate group of alarms to force the section overhead outputs to all ones. Setting a bit to logic one enables a declared alarm in that bit's group to force the output section overhead to all ones. Alarms in that group will not explicitly force the section overhead outputs to all ones when the bit is set to logic low.

SECT_AIS_EN	Grouped Alarms
[0]	LOS & LOF
[1]	LAIS
[2]	RTIM

LINE_AISEN(:0):

The LINE_AISEN(2:0) bits enable the explicit insertion of all ones on RLOW, RLD, ROH and RSLD when carrying line overhead and the line overhead on RTOH. Each bit enables a separate group of alarms to force the line overhead outputs to all ones. Setting a bit to logic one enables a declared alarm in that bit's group to force the output line overhead to all ones. Alarms in that group will not explicitly force the line overhead outputs to all ones when the bit is set to logic low. Other SPECTRA-622 top level bits may control the

insertion of LAIS on certain alarms and hence affect the line overhead outputs when all ones insertion is disabled here.

LINE_AIS_EN	Grouped Alarms
[0]	LOS & LOF
[1]	LAIS
[2]	RTIM

Register 00A2H: Transmit DLL Reset Register

	W	Reserved	
	W	Reserved	
	W	Reserved	
	W	Reserved	
	W	Reserved	
	W	Reserved	
	W	Reserved	

Writing to this register performs a software reset of the DLL. A software reset should be applied after setting the device in parallel transmit mode and the TDCK input is frequency stable.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

Register 00A3H: Transmit DLL Control Status

Bit	Type	Function	Default
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	0
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found a delay line tap in which the TX parallel interface timings will be met. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a system reset or a software reset (writing to register 00A2H).

CHANGE:

The delay line tap change register bit CHANGE indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight TDCLK cycles when the DLL moves to a new delay line tap. A fixed value of 1 indicates that the DLL has not locked to a frequency and should be reset.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. ERROR is set low when the DLL captures lock again. The DLL should be reset by writing to register 00A2H if the ERROR condition persist.

CHANGEI:

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has changed value. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 00A4H: DROP Bus DLL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0

Bit	Type	Function	Default
Bit 4	R/W	OVERRIDE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W		0
Bit 0	R/W		0

The DLL Configuration Register controls the basic operation of the DLL.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

OVERRIDE:

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DROP bus clock (DCK) is processed by the DLL before clocking the DROP interface logic. The DLL must not be overridden (set low) in 77.76 MHz DROP interface mode if the specified propagation delays are to be met for the interface. When OVERRIDE is set high, the DROP bus clock (DCK) is not processed by the DLL before clocking the DROP interface logic. The DLL must be overridden (set high) in 19.44 MHz DROP interface mode if the specified propagation delays are to be met for the interface. The DLL does not function at 19.44

Register 00A6H: DROP Bus DLL Reset Register

Bit	Type	Function	Default
Bit 7		Reserved	X
Bit 6	W	Reserved	
Bit 5	W	Reserved	
Bit 4	W	Reserved	
Bit 3	W	Reserved	
Bit 2	W	Reserved	
Bit 1	W	Reserved	
Bit 0	W	Reserved	

Writing to this register performs a software reset of the DLL. A software reset should be applied after when setting the device in 77.76 MHz DROP interface mode and the DCK input is frequency stable.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

Register 00A7H: DROP Bus DLL Control Status

Bit	Type	Function	Default
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	0
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found a delay line tap in which the DROP interface timings will be met at 77.76 Mhz interface mode. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1. The RUN register bit is cleared only by a system reset or a software reset (writing to register 00A6H).

CHANGE:

The delay line tap change register bit CHANGE indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight DCK cycles when the DLL moves to a new delay line tap. A fixed value of 1 indicates that the DLL has not locked to a frequency and should be reset.

ERROR:

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. ERROR is set low, when the DLL captures lock again. The DLL should be reset by writing to register 00A6H if the ERROR condition presist.

CHANGEI:

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to

logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

ERRORI:

The delay line error event register bit (ERRORI) indicates the ERROR register bit has changed value. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 00B0H: CSPI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ROOLI	X

The CSPI Configuration register is provided to configure the operation of the CSU-622 clock synthesizer.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOL output and the ROOLV register changes state, indicating that either the PLL is locked to the reference clock REFCLK or in out of lock. ROOLI is cleared when this register is read. If the ROOLE interrupt enable is high, the INTB output is also asserted with ROOLI asserted.

Register 00B1H: CSPI Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	ROOLV	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ROOLE	0

The Status register is provided to determine the status of the CSU-622 clock synthesizer.

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOL output and the ROOLV register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

ROOLV:

The transmit reference out of lock status indicates the clock synthesis phase lock loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the divided down synthesized clock frequency is not within 488ppm of the REFCLK frequency. At startup, ROOLV may remain high for several hundred millisecond while the PLL obtains lock. The CSU tracks slow rate changes in REFCLK.

Register 00B4H: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	DC1	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-622.

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set high, the TSOP inserts line AIS into the transmit stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

DC1:

The DC1 bit controls the overwriting of the identity bytes (J0/Z0). When DC1 is logic one, the values inserted by the TTOC during the J0/Z0 byte positions are passed through the transmit section overhead processor unaltered. Note that all 11 (STS-12/STM-4) identification bytes are passed through unaltered. When DC1 is logic zero, the identity bytes are programmed as specified in the North American references: STS-1 (STM-0) #1 J0 = 01H, STS-1 (STM-0) #2 Z0 = 02H, and STS-1 (STM-0) #N Z0 = N decimal. Setting this bit to one can generate long strings of zeros (> 88 bits) on the output stream depending on the TTOC programming.

DS:

The disable scrambling (DS) bit controls the scrambling of the transmit stream. When a logic one is written to the DS bit position, the scrambler is disabled. When a logic zero is written to the DS bit position, the scrambler is enabled.

Register 00B5H: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DB1	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. If DFP is set high the A1 bytes are set to 76H instead of F6H.

DB1:

The DB1 bit controls the insertion of bit errors continuously in the B1 section overhead byte. When DB1 is set high the B1 byte value is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit outgoing stream. When DLOS is set high the transmit stream is forced low.

Register 00B8H: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

Reserved:

The Reserved bits must be set low for proper operation of SPECTRA-622.

LRDI:

The LRDI bit controls the insertion of transmit line remote defect indication (RDI). When LRDI is a logic one, line RDI is inserted into the transmit stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte. Line RDI may also be inserted using the TLRDI input (when the ring control ports are disabled) or using the transmit ring control port (when it is enabled). When LRDI is logic zero, bit 6, 7, and 8 of the K2 byte are not modified by the transmit line overhead processor.

Line RDI may also be inserted into the transmit stream, when receive line AIS is detected, by setting LAISINS bit to high in the SPECTRA-622 Line RDI Control register. Setting of this register bit is also required for line RDI insertion via the transmit ring control port.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, the transmit APS channel is inserted by the TTOC block from the bit serial input TOH which is shifted in on the rising edge of TOHCLK. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Register 00B9H: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DB2	0

DB2:

The DB2 bit controls the insertion of bit errors continuously in each of the line BIP-8 bytes (B2 bytes). When DB2 is set high, each bit of every B2 byte is inverted.

Register 00BAH: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 00BBH: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 00C0H: TTOC Transmit Overhead Output Control

Bit	Type	Function	Default
Bit 7	R/W	TX_GAPSEL	0
Bit 6	R/W	TOH_TS	1
Bit 5	R/W	TOH_SEL[1]	0
Bit 4	R/W	TOH_SEL[0]	0
Bit 3	R/W	TLD_TS	1
Bit 2	R/W	TSLD_TS	1
Bit 1	R/W	TSLD_VAL	X
Bit 0	R/W	TSLD_SEL	0

TSLD_SEL:

The transmit data line select (TSLD_SEL) bit determines the content of the incoming TSLD stream. When TSLD_SEL is low, the TSLD stream contains the section DCC (D1-D3). When TSLD_SEL is high, the TSLD stream contains the line DCC (D4-D12). When TSLD_SEL selects the line DCC on TSLD, section DCC (D1-D3) can be controlled using the TTOH input or can be forced to an all ones or all zeros pattern using the TSLD_VAL.

TSLD_VAL:

The transmit section/line DCC value (TSDVAL) bit selects an all ones or all zeros value on the section DCC data (D1, D2, D3) when TSLD_SEL register bit selects the TSLD input to provide the line DCC. Setting TSDVAL to high will force the section data link (D1, D2, D3) to all ones and setting the bit to low will force the data to all zeros. In such a case, the section DCC still can be controlled using the TTOH input.

TSLD_TS:

The transmit section/line data link tri-state (TSLD_TS) bit controls the tri-stating of the TSLDCLK output. TSLD_TS defaults to logic one so that TSLDCLK will be tri-stated after a reset.

TLD_TS:

The transmit line data link tri-state (TLD_TS) bit controls the tri-stating of the TLDCLK output. TLD_TS defaults to logic one so that TLDCLK will be tri-stated after a reset.

TOH_SEL[1:0]:

The transmit overhead select (TOH_SEL[1:0]) bus determines the contents of the incoming TOH stream and the frequency of the TOHCLK. The decoded TOH_SEL settings are listed below.

TOH_SEL[1:0]	Contents	TOHCLK
00	Section Order Wire (E1)	Nominal 64 kHz
01	Section User Channel (F1)	Nominal 64 kHz
10	Line Order Wire (E2)	Nominal 64 kHz
11	APS Bytes (K1/K2)	Nominal 128 kHz

By default the TOH input will overwrite the TSOW input. To prevent this, the TOH_SEL needs to be set to '11'. Setting TAPS_SEL (reg 00C1h) will prevent to overwritting of K1/K2 by TOH.

TOH_TS:

The transmit overhead tri-state (TOH_TS) bit controls the tri-stating of the TFP and TOHCLK outputs. TOH_TS defaults to logic one so that TFP and TOHCLK will be tri-stated after a reset.

TX_GAPSEL:

The Transmit Gap Select (TX_GAPSEL) bit is used to select the interface mode of the various transmit overhead ports (TSOW, TSUC, TLOW, TSLD, TLD and TOH). When TX_GAPSEL is a logic zero the TOWCLK, TSLDCLK, TLDCLK and TOHCLK are smooth clocks and the TTOHFP signal may be used to identify the byte alignment on the associated serial inputs. When TX_GAPSEL is a logic one the TOWCLK, TSLDCLK, TLDCLK and TOHCLK are gapped clocks and a gap detection using a higher speed clock is needed to detect the byte alignment on the associated serial inputs. TFP may also be used an asynchronous reset to find the byte alignment when TX_GAPSEL is set to logic one.

Register 00C1H: TTOC Transmit Overhead Byte Control

Bit	Type	Function	Default
Bit 7	R/W	TREN	1
Bit 6	R/W	REI_EN	0
Bit 5	R/W	TAPS_SEL	0
Bit 4	R/W	Z0INS	0
Bit 3	R/W	UNUSED_EN	0
Bit 2	R/W	UNUSED_V	0
Bit 1	R/W	NAT_EN	0
Bit 0	R/W	NAT_V	0

NAT_V:

The NAT_V bit determines the value to insert into the national use transport overhead bytes when the NAT_EN register bit is programmed to overwrite these bytes. When NAT_V is set high, the national use transport overhead bytes are set to FFH. When NAT_V is set low, the national use transport overhead bytes are set to 00H. This register bit has not effect when the NAT_EN register bit is set to logic zero.

NAT_EN:

The NAT_EN bit enables overwriting the national use transport overhead bytes with an all ones or all zeros pattern. The national use TOH bytes affected when NAT_EN is set high are the F1 and E2 bytes of STS-1 (STM-0/AU3) #2 to #12 and the Z0 bytes of STS-1 #5 to #12, as specified by ITU. When this bit is high, these bytes are overwritten with an all ones pattern or all zeros pattern as controlled by the NAT_V bit. When NAT_EN is set low, the national use TOH bytes are controlled by the TTOHEN input or Z0INS register bit. The Z0INS register bit has precedence over NAT_EN for the setting of Z0. NAT_EN has precedence over TTOHEN for all three bytes. Since the Z0 byte is not scrambled, setting this bit will generate very long gap without transition on the output stream.

UNUSED_V:

The UNUSED_V bit determines the value to insert into the unused transport overhead bytes when the UNUSED_EN register bit is programmed to overwrite these bytes. When UNUSED_V is set high, the unused transport overhead bytes are set to FFH. When UNUSED_V is set low, the unused transport overhead bytes are set to 00H. This register bit has not effect when the UNUSED_EN register bit is set to logic zero.

UNUSED_EN:

The UNUSED_EN bit enables overwriting the unused transport overhead bytes with an all ones or all zeros pattern. When UNUSED_EN is set high, the unused transport overhead bytes (B1 byte positions of STS-1 #N for 2≤N≤12, D1 to D3 byte positions of STS-1 #N for 2≤N≤12, K1 and K2 byte positions of STS-1 #N for 2≤N≤12, D4 to D12 byte positions of STS-1 #N for 2≤N≤12, Z1 byte positions of STS-1 #N for 2≤N≤12, Z2 byte positions of STS-1 #N for 4≤N≤12 and N=2) are overwritten with an all ones pattern or all zeros pattern as controlled by the UNUSED_V bit. When UNUSED_EN is set low, the unused transport overhead bytes are controlled by the TTOHEN input. When UNUSED_EN and TTOHEN are both high, the UNUSED_EN has precedence.

Z0INS:

The Z0INS bit controls the values inserted in the transmit Z0 bytes. When Z0INS is logic 1, the value contained in the TTOC Transmit Z0 register is inserted in the Z0 bytes of STS-1 #2 to #12 as specified by Bellcore. ZOINS has precedence over the NAT_EN register bit, TTOH/TTOHEN inputs and the TSOP Control Register DC1 register bit. When Z0INS is logic 0, the Z0 bytes may be inserted via the NAT_EN register bit or TTOH/TTOHEN. Leaving the Z0 bytes undefined and programming the DC1 bit in the TSOP Control register to logic zero will allow an incremental count of 2 to 12 to be inserted into the Z0 bytes.

TAPS_SEL:

The transmit APS select (TAPS_SEL) bit selects the source of the transmit APS (K1/K2) bytes. When TAPS_SEL is low, the TTOHEN or TOH is used as source for the APS bytes. TTOH has precedence over TOH. When TAPS_SEL is high, the APS bytes are sourced from Transmit alarm port (TAP).

REI_EN:

The REI_EN bit enables the TTOHREI input and the insertion of an REI error count into the transmit M1 byte position. When this bit is set high, the REI count to be inserted into the M1 byte is supplied via the TTOHREI input. For each REI error, a logic 1 must be sampled on TTOHREI. The high samples (pulses) in between TTOHFP pulses are counted and the count inserted into the M1 byte. When REI_EN is set low, the M1 byte may be supplied via the TTOH and TTOHEN inputs.

TREN:

The transmit trace enable (TREN) bit enables the insertion of the section trace message programmed in the SSTB. Setting this bit to logic one will enable the insertion of the SSTB stored message into the transmit stream. When setting this bit to logic zero, the section trace message may be inserted byte by byte using the TTOH and TTOHEN overhead inputs. When not asserting TTOHEN for the insertion of J0 or enabling TREN, the TSOP DC1 register bit in the TSOP Control Register may be used to insert the 01h value into the J0 byte position.

Register 00C2H: TTOC Transmit Z0

Bit	Type	Function	Default
Bit 7	R/W	Z0[7]	1
Bit 6	R/W	Z0[6]	1
Bit 5	R/W	Z0[5]	0
Bit 4	R/W	Z0[4]	0
Bit 3	R/W	Z0[3]	1
Bit 2	R/W	Z0[2]	1
Bit 1	R/W	Z0[1]	0
Bit 0	R/W	Z0[0]	0

Z0[7:0]:

Z0[7:0] contains the value inserted in Z0 bytes of the transmit stream when the Z0INS register bit is logic 1. Z0[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z0[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The Z0 byte defaults to “11001100b”.

Register 00C3H: TTOC Transmit S1

Bit	Type	Function	Default
Bit 7	R/W	S1[7]	0
Bit 6	R/W	S1[6]	0
Bit 5	R/W	S1[5]	0
Bit 4	R/W	S1[4]	0
Bit 3	R/W	S1[3]	0
Bit 2	R/W	S1[2]	0
Bit 1	R/W	S1[1]	0
Bit 0	R/W	S1[0]	0

S1[7:0]:

The value written into these register bits is inserted in the first S1/Z1 (S1) byte position of the transmit stream when a byte is not . The S1 byte is used to carry synchronization status messages between line terminating network elements. S1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. S1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The TTOHEN input takes precedence over the contents of this register.

Register 0100H: SPECTRA-622 RPPS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MASTER	1
Bit 6	R/W	STM1-CONCAT	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved Unused	0
Bit 3	R/W	Reserved Unused	0
Bit 2	R/W	Reserved Unused	0
Bit 1	R/W	Reserved Unused	0
Bit 0	R/W	Reserved	0

This register allows the operational mode of the SPECTRA-622 Receive Path Processing Slice (RPPS) to be configured.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

STM1-CONCAT:

The STM1-CONCAT bit is used to configure the RPPS to be processing TU2, TU11 or TU12 inside an STM-1(VC-4). When configured, TUAIS is properly asserted as defined by the ITUAIS in the RTAL. When set high, the RTAL fixed stuff columns are columns 1, 2 and 3. This supports TU2, TU11 and TU12 payloads in a VC-4. When set low, the RTAL fixed stuff columns are columns 30 and 59. When set low TUAIS can not be inserted properly. This bit can otherwise be set low.

MASTER:

When set high, the MASTER bit enables the RPPS to control and co-ordinate the processing of an STS-1 (STM-0/AU3) or an STS-Nc (STM-1/AU4 OR STM-4-Xc) receive stream as the master. It also enables the RPPS to control and co-ordinate the distributed PRBS payload sequence generation and monitoring. When the MASTER bit is set low, the RPPS operates in a slave mode and its operation is co-ordinated by the associated master RPPS. Setting this bit low (slave mode) does not necessarily mask alarms or errors

which a master slice can only declare. The alarms or errors must be disabled via the appropriate register bits.

Register 0102H: SPECTRA-622 RPPS Path and DS3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	ENDV1	0
Bit 6	R/W	MONRS	0
Bit 5	R/W	ALMJ1V1	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	DS3_SEL52	0

This register allows the operational mode of the SPECTRA-622 RPPS Path and DS3 functions to be configured. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

DS3_SEL52:

The DS3 select 52 clock (DS3_SEL52) bit selects the desynchronizer source clock used by the D3MD block. When DS3_SEL52 is set low, the DS3RICLK input are used as the D3MD source clock. When DS3_SEL52 is set high, an internal 51.84 MHz recovered line clock is used as the D3MD source clock. The REFCLK signal is required to use the recovered line clock.

ALMJ1V1:

When set high, the ALMJ1V1 bit disables the realignment of the Telecombus DROP side J1 and V1 indication on DC1J1V1 when the RPOP block is in the LOP or PAIS state. The J1 and V1 pulses will flywheel at their previous position prior to entry to the LOP or PAIS state.

MONRS:

When set high, the MONRS selects the receive side pointer justification events counters to monitor the receive stream directly. When MONRS is set low, the counters accumulate pointer justification events on the DROP bus.

ENDV1:

When set low, the ENDV1 bit configures the DC1J1V1 output to mark only the frame and synchronous payload envelope (virtual container) alignments (C1

and J1 bytes). DC1J1V1 will not indicate the tributary multiframe alignment. When ENDV1 is set high, DC1J1V1 marks all three of the frame, payload envelope and tributary multiframe alignments. When the RTAL FIFO in set in bypass mode, the V1 pulse is always outputted regardless of the setting of this bit.

Register 0110H: SPECTRA-622 RPPS Path/DS3 AIS Control #1

Bit	Type	Function	Default
Bit 7	R/W	LOMTUAIS	0
Bit 6	R/W	ALMAIS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPAIS	0
Bit 2	R/W	PAISAIS	0
Bit 1	R/W	LOPCONPAIS	0
Bit 0	R/W	PAISCONPAIS	0

This register along with the SPECTRA-622 RPPS Receive Path/DS3 AIS Control #2 register controls the auto assertion of path AIS and DS3 AIS on the DROP bus. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enables path AIS insertion on the DROP bus when Path AIS concatenation (PAISCON) events are detected. When PAISCONPAIS is set low, Path AIS concatenation events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low. The register bit will also force the associated master and slave RPPS's to insert path AIS.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enables path AIS insertion on the DROP bus when loss of pointer concatenation (LOPCON) events are detected. When LOPCONPAIS is set low, loss of pointer concatenation events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low. The register bit will also force the associated master and slave RPPS's to insert path AIS.

PAISAIS:

When set high, the PAISAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path AIS is detected in the receive stream. When PAISAIS is set low, path AIS events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPS's to insert path AIS.

LOPAIS:

When set high, the LOPAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when loss of pointer (LOP) events are detected in the receive stream. When LOPAIS is set low, loss of pointer events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPS's to insert path AIS.

ALMAIS:

When set high, the ALMAIS bit enables path AIS and DS3 AIS assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMAIS is set low, the above events have no effect on path AIS nor DS3 AIS.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPS's to insert path AIS.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the DROP bus when loss of multiframe (LOM) events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. The STM1-CONCAT bit must be set high for TU2, TU11 and TU12 payloads in a VC-4. When LOMTUAIS is set low, loss of multiframe events have no effect on the DROP bus. LOMTUAIS must be set low when processing TU3 or payload not requiring tributary multiframe alignment.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPS's to insert tributary AIS.

Register 0111H: SPECTRA-622 RPPS Path/DS3 AIS Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQAIS	0
Bit 5	R/W	PSLUAIS	0
Bit 4	R/W	PSLMAIS	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	0
Bit 1	R/W	TIUAIS	0
Bit 0	R/W	TIMAIS	0

This register along with the SPECTRA-622 RPPS Path/DS3 AIS Control #1 register controls the auto assertion of path AIS and DS3 AIS on the DROP bus. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

TIMAIS:

When set high, the TIMAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path trace identifier mismatch (TIM) events are detected in the receive stream. When TIMAIS is set low, trace identifier (mode 1) mismatch events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPS's to insert path AIS.

TIUAIS:

When set high, the TIUAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path trace identifier (mode 1) unstable events are detected in the receive stream. When TIUAIS is set low, trace identifier (mode 1) unstable events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPS's to insert path AIS.

PSLMAIS:

When set high, the PSLMAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMAIS is set low, path signal label mismatch events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPS's to insert path AIS.

PSLUAIS:

When set high, the PSLUAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUAIS is set low, path signal label unstable events have no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPS's to insert path AIS.

UNEQAIS:

When set high, the UNEQAIS bit enables path AIS and DS3 AIS insertion on the DROP bus when path signal label in the receive stream indicates unequipped status (UNEQ). When UNEQAIS is set low, the path signal label unequipped status has no effect on the DROP bus.
NOTE: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPS's to insert path AIS.

Register 0114H: SPECTRA-622 RPPS Path REI/RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	AUTOPREI	0
Bit 6	R/W	ALMPRDI	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPRDI	0
Bit 2	R/W	PAISPRDI	0
Bit 1	R/W	LOPCONPRDI	0
Bit 0	R/W	PAISCONPRDI	0

This register along with the SPECTRA-622 RPPS Path REI/RDI Control #2 register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP or a mate TPOP (via the RAD PRDI5 bit position) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PAISCONPRDI:

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONPRDI:

When set high, the LOPCONPRDI bit enables path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPRDI is set low, loss of pointer concatenation events have no effect on path RDI.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

PAISPRDI:

When set high, the PAISPRDI bit enables path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When PAISPRDI is set low, PAIS states have no effect on path RDI.

LOPPRDI:

When set high, the LOPPRDI bit enables path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPRDI is set low, loss of pointer events have no effect on path RDI.

ALMPRDI:

When set high, the ALMPRDI bit enables path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMPRDI is set low, the above events have no effect on path RDI.

AUTOPREI:

The AUTOPREI bit enables the automatic insertion of path REI events in the local or mate transmitter. When AUTOPREI is a logic one, receive B3 errors detected by the SPECTRA-622 are automatically inserted in the G1 byte of the local transmit stream (as enabled using the RXSEL[1:0] bits in the SPECTRA-622 TPPS Configuration register). In addition, REI events are indicated on the RAD output. When AUTOPREI is a logic zero, path REI events are not automatically inserted in the local transmit stream. In addition, REI events are not indicated on the RAD output.

Register 0115H: SPECTRA-622 RPPS Path REI/RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQPRDI	0
Bit 5	R/W	PSLUPRDI	0
Bit 4	R/W	PSLMPRDI	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TIUPRDI	0
Bit 0	R/W	TIMPRDI	0

This register along with the SPECTRA-622 RPPS Path REI/RDI Control #1 register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP or a mate TPOP (via the RAD PRDI5 bit position) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

TIMPRDI:

When set high, the TIMPRDI bit enables path RDI assertion when path trace identifier (mode 1) mismatch (TIM) events are detected in the receive stream. When TIMPRDI is set low, trace identifier (mode 1) mismatch events have no effect on path RDI.

TIUPRDI:

When set high, the TIUPRDI bit enables path RDI assertion when path trace identifier (mode 1) unstable (TIU) events are detected in the receive stream. When TIUPRDI is set low, trace identifier (mode 1) unstable events have no effect on path RDI.

PSLMPRDI:

When set high, the PSLMPRDI bit enables path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPRDI is set low, path signal label mismatch events have no effect on path RDI.

PSLUPRDI:

When set high, the PSLUPRDI bit enables path RDI assertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPRDI is set low, path signal label unstable events have no effect on path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

Register 0118H: SPECTRA-622 RPPS Path Enhanced RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	PERDI_EN	0
Bit 6	R/W	ALMPERDI	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPERDI	0
Bit 2	R/W	PAISPERDI	0
Bit 1	R/W	LOPCONPERDI	0
Bit 0	R/W	PAISCONPERDI	0

This register along with SPECTRA-622 Path Enhanced RDI Control #2 register controls the auto assertion of path enhanced RDI (G1 bits 5,6,7) in the local TPOP or a mate TPOP (via the RAD PRDI5, PRDI6 and PRDI7 bit positions) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PAISCONPERDI:

When set high, the PAISCONPERDI bit enabled path enhanced RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. PAISCONPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI.

When PAISCONPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI and the associated alarm states.

NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONPERDI:

When set high, the LOPCONPERDI bit enables path enhanced RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the

RAD output PRDI7 bit position) is set high. LOPCONPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI.

When LOPCONPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI and the associated alarm states.

NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

PAISPERDI:

When set high, the PAISPERDI bit enables path enhanced RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. PAISPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI.

When PAISPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI and the associated alarm states.

LOPPERDI:

When set high, the LOPPERDI bit enables path enhanced RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. LOPPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI.

When LOPPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI and the associated alarm states.

ALMPERDI:

When set high, the ALMPERDI bit enables path enhanced RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set

high. ALMPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI.

When ALMPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIU2PERDI, TIMPERDI and UNEQERDI and the associated alarm states.

PERDI_EN:

The PERDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter or in a mate transmitter via the RAD output. When PERDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register and in the SPECTRA-622 Path Enhanced RDI Control #2 register. When PERDI_EN is a logic zero, path enhanced RDI is not automatically inserted in the transmit stream.

Register 0119H: SPECTRA-622 RPPS Path Enhanced RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQPERDI	0
Bit 5	R/W	PSLUPERDI	0
Bit 4	R/W	PSLMPERDI	0
Bit 3	R/W	Unused	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TIUPERDI	0
Bit 0	R/W	TIMPERDI	0

This register along with SPECTRA-622 Path Enhanced RDI Control #1 register controls the auto assertion of path enhanced RDI (G1 bits 5,6,7) in the local TPOP or a mate TPOP (via the RAD PRDI5, PRDI6 and PRDI7 bit positions) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

TIMPERDI:

When set high, the TIMPERDI bit enables path enhanced RDI assertion when path trace identifier (mode 1) mismatch (TIM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIMPERDI is set low, trace identifier (mode 1) mismatch events have no effect on path RDI. In addition, this bit has no effect when PERDI_EN is set low.

TIUPERDI:

When set high, the TIUPERDI bit enables path enhanced RDI assertion when path trace identifier (mode 1) unstable (TIU) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUPERDI is set low, trace identifier (mode 1) unstable events have no effect on path RDI. In addition, this bit has no effect when PERDI_EN is set low.

PSLMPERDI:

When set high, the PSLMPERDI bit enables path enhanced RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLMPERDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when PERDI_EN is set low.

PSLUPERDI:

When set high, the PSLUPERDI bit enables path enhanced RDI assertion when path signal label unstable (PSLU) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLUPERDI is set low, path signal label unstable events have no effect on path RDI. In addition, this bit has no effect when PERDI_EN is set low.

UNEQPERDI:

When set high, the UNEQPERDI bit enables path enhanced RDI assertion when the path signal label in the receive stream indicates unequipped status. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When UNEQPERDI is set low, path signal label unequipped status has no effect on path enhanced RDI.

Register 011CH: SPECTRA-622 RPPS RALM Output Control #1

Bit	Type	Function	Default
Bit 7	R/W	LOMRALM	0
Bit 6	R/W	PRDIRALM	0
Bit 5	R/W	PERDIRALM	0
Bit 4	R/W	ALMRALM	0
Bit 3	R/W	LOPRALM	0
Bit 2	R/W	PAISRALM	0
Bit 1	R/W	LOPCONRALM	0
Bit 0	R/W	PAISCONRALM	0

This register along with SPECTRA-622 RALM Output Control #2 register controls the receive path alarm output (RALM) signal. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

PAISCONRALM:

The path alarm indication signal concatenation (PAISCON) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONRALM:

The loss of pointer concatenation (LOPCON) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

PAISRALM:

The path alarm indication signal (PAIS) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

LOPRALM:

The loss of pointer (LOP) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PERDIRALM:

The path enhanced remote defect indication (PERDI) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PRDIRALM:

The path remote defect indication (PRDI) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

ALMRALM:

The loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

LOMRALM:

The loss of multiframe (LOM) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

Register 011DH: SPECTRA-622 RPPS RALM Output Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQRALM	0
Bit 5	R/W	PSLURALM	0
Bit 4	R/W	PSLMRALM	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	TIURALM	0
Bit 0	R/W	TIMRALM	0

This register along with SPECTRA-622 RALM Output Control #1 register controls the receive path alarm output (RALM) signal. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

TIMRALM:

The path trace identifier mismatch (TIM) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

TIURALM:

The path trace identifier (mode 1) unstable (TIU) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PSLMRALM:

The path signal label mismatch (PSLM) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PSLURALM:

The path signal label unstable (PSLU) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

UNEQRALM:

The path unequipped (UNEQ) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

Register 0128H: SPECTRA-622 RPPS Path/DS3 Interrupt Status

Bit	Type	Function	Default
Bit 7	R	DPAIS	X
Bit 6	R	RPOPI	X
Bit 5	R	RTALI	X
Bit 4	R	SPTBI	X
Bit 3	R	D3MDI	X
Bit 2		Unused	X
Bit 1	R	DPGMI	X
Bit 0		Unused	X

This register, together with the SPECTRA-622 Section/Line Interrupt Status register, allows the source of an active interrupt for the receive side to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source. These register bits are not cleared on read.

DPGMI:

The DPGMI bits are high when an interrupt request is active from the DPGM block.

D3MDI:

The D3MDI bit is high when an interrupt request is active from the D3MD block.

SPTBI:

The SPTBI bit is high when an interrupt request is active from the SPTB block.

RTALI:

The RTALI bits is high when an interrupt request is active from the RTAL block.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block.

DPAIS:

The DROP bus alarm indication signal (DPAIS) bit is set high when path AIS is inserted in the DROP bus. DROP bus Path AIS assertion can be automatic using the SPECTRA-622 RPPS Path AIS Control #1 and #2 registers or manual using the RTAL Control registers. Note, DPAIS is not an interrupt bit.

Register 012CH: SPECTRA-622 RPPS Auxiliary Path Interrupt Enable #1

Bit	Type	Function	Default
Bit 7	R/W	PRDIE	0
Bit 6	R/W	PAISE	0
Bit 5	R/W	PSLUE	0
Bit 4	R/W	PSLME	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	LOME	0
Bit 1	R/W	TIUE	0
Bit 0	R/W	TIME	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #1 register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #1 register.

These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

TIME:

The path trace identifier (mode 1) mismatch (TIM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIM interrupt status.

TIUE:

The path trace identifier (mode 1) unstable (TIU) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIU interrupt status.

LOME:

The loss of multiframe (LOM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOM interrupt status.

LOPE:

The loss of pointer (LOP) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOP interrupt status.

PSLME:

The path signal label mismatch (PSLM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PSLM interrupt status.

PSLUE:

The path signal label unstable (PSLU) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PSLU interrupt status.

PAISE:

The path alarm indication signal (PAIS) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAIS interrupt status.

PRDIE:

The path remote defect indication (PRDI) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PRDI interrupt status.

Register 012DH: SPECTRA-622 RPPS Auxiliary Path Interrupt Enable #2

Bit	Type	Function	Default
Bit 7	R/W	LOPCONE	0
Bit 6	R/W	PAISCONE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TIU2E	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PERDIE	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #2 register. Note, these enable bits do not affect the actual interrupt status bits found in the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #2 register.

These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PERDIE:

The path enhanced remote defect indication (PERDI) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PERDI interrupt status.

TIU2E:

The path trace identifier mode 2 unstable (TIU2) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIU2 interrupt status.

PAISCONE:

The path alarm indication signal concatenation (PAISCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAISCON interrupt status.
NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONE:

The loss of pointer concatenation (LOPCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOPCON interrupt status. NOTE: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

Register 0130H: SPECTRA-622 RPPS Auxiliary Path Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R/W	PRDII	X
Bit 6	R/W	PAISI	X
Bit 5	R/W	PSLUI	X
Bit 4	R/W	PSLMI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	TIUI	X
Bit 0	R/W	TIMI	X

This register, along with the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #2 register, replicates the path interrupts that can be found in the RPOP and the SPTB registers. However, unlike the RPOP and the SPTB interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

TIMI:

The path trace identifier mismatch interrupt status bit (TIMI) is set high on changes in the path trace identifier mismatch status.

TIUI:

The path trace identifier (mode 1) unstable interrupt status bit (TIUI) is set high on changes in the path trace identifier (mode 1) unstable status (TIU).

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status.

LOPI:

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PSLMI:

The path signal label mismatch interrupt status bit (PSLMI) is set high on changes in the path signal label mismatch status.

PSLUI:

The path signal label unstable interrupt status bit (PSLUI) is set high on changes in the path signal label unstable status.

PAISI:

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PRDII:

The path RDI interrupt status bit (PRDII) is set high on changes in the path remote defect indication status.

Register 0131H: SPECTRA-622 RPPS Auxiliary Path Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R/W	LOPCONI	X
Bit 6	R/W	PAISCONI	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	TIU2I	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	PERDII	X

This register, along with the SPECTRA-622 RPPS Auxiliary Path Interrupt Status #1 register, replicates the path interrupts that can be found in the RPOP and the SPTB registers. However, unlike the RPOP and the SPTB interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PERDII:

The path enhanced remote defect indication interrupt (PERDII) bits are set high when the RPOP detects a change in the path enhanced remote defect state.

TIU2I:

The path trace identifier unstable mode 2 interrupt status bit (TIU2I) is set high on changes in the path trace identifier unstable status for mode 2 operation.

PAISCONI:

The path AIS concatenation interrupt (PAISCONI) bit is set high when there is a change of the path AIS concatenation state. This auxiliary interrupt status corresponds to the AU3PAISCONI status in the RPOP Alarm Interrupt Status register.

LOPCONI:

The loss of pointer concatenation interrupt (LOPCONI) bit is set high when there is a change of the pointer concatenation state. This auxiliary interrupt

status corresponds to the AU3LOPCONI status in the RPOP Alarm Interrupt Status register.

Register 0134H: SPECTRA-622 RPPS Auxiliary Path Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current filtered value of the enhanced RDI codepoint (G1 bits 5, 6, & 7) for the receive SONET/SDH stream.

Filtering is controlled using the RDI10 bit in the RPOP, Pointer MSB register. This register reflects the same ERDIV[2:0] value that can be found in the RPOP, Status and Control (EXTD=1) register. This register can be used for interrupt handling if it is undesirable to use the EXTD feature.

Register 0150H: RPOP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	AU3LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	AU3PAISCONV	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set low in the RPOP Pointer MSB register.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI:

The NEWPTRI bit is set to logic 1 when a new_point indication is received. This bit (and the interrupt) are cleared when this register is read.

PRDIV:

The path RDI status bit (PRDI) indicates reception of path RDI alarm in the receive stream.

PAISV:

The path AIS status bit (PAISV) indicates reception of path AIS alarm in the receive stream.

AU3PAISCONV:

The AU3 concatenation path AIS status bit (AU3PAISCONV) indicates reception of path AIS alarm in the concatenation indication in the receive STS-1 (STM-0/AU3) or equivalent stream.

LOPV:

The loss of pointer status bit (LOPV) indicates entry to the LOP_state in the RPOP pointer interpreter state machine.

AU3LOPCONV:

The AU3 concatenated loss of pointer status bit (AU3LOPCONV) indicates entry to LOPCON_state for the receive STS-1 (STM-0/AU3) or equivalent stream in the RPOP pointer interpreter.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-622.

Register 0150H: RPOP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set high in the RPOP Pointer MSB register.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, & 7).

PSL5:

The PSL5 bit controls the filtering of the path signal label (PSL) byte (C2). When a 1 is written to PSL5, the PSL is updated when the same value is received for 5 consecutive frames. When a 0 is written to PSL5, the PSL is updated when the same value is received for 3 consecutive frames.

IINVCNT:

When a 1 is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to 0, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

Register 0151H: RPOP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	AU3LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	AU3PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the RPOP Pointer MSB register.

These bits (and the interrupt) are cleared when this register is read.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected.

BIPEI:

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PRDII:

The PRDII interrupt status bit is set high on assertion and removal of the corresponding path remote defect indication status.

PAISI:

The PAISI interrupt status bit is set high on assertion and removal of the corresponding path alarm indication signal status.

AU3PAISCONI:

The AU3PAISCONI interrupt status bit is set high on assertion and removal of the corresponding AU3 path alarm indication signal concatenation status.

LOPI:

The LOPI interrupt status bit is set high on assertion and removal of the corresponding loss of pointer status.

AU3LOPCONI:

The AU3LOPCONI interrupt status bit is set high on assertion and removal of the corresponding AU3 loss of pointer concatenation status.

Register 0151H: RPOP Alarm Interrupt Status (EXTD=1)

Bit	Type	Function	Default
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	ERDII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set high in the RPOP Pointer MSB register.

These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

ERDII:

The ERDII bit is set to logic 1 when a change is detected in the received enhanced RDI state.

Register 0152H: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	Reserved	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	Reserved	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

These bits (and the interrupt) are cleared when this register is read.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

NDFI:

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI:

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the RPOP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

INVNDFI:

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI:

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the RPOP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI:

The illegal justification request interrupt status bit (ILLJREQI) is set high when the RPOP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

Register 0153H: RPOP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	AU3LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	AU3PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the RPOP Pointer MSB register.

PREIE:

When a 1 is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PRDIE:

When a 1 is written to the PRDIE interrupt enable bit position, a change in the path RDI state will activate the interrupt (INTB) output.

PAISE:

When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

AU3PAISCONE:

When a 1 is written to the AU3PAISCONE interrupt enable bit position, a change in the AU3 concatenation path AIS state will activate the interrupt (INTB) output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

AU3LOPCONE:

When a 1 is written to the AU3LOPCONE interrupt enable bit position, a change in the AU3 concatenation loss of pointer state will activate the interrupt (INTB) output.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622.

Register 0153H: RPOP Alarm Interrupt Enable (EXTD=1)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	ERDIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set high in the RPOP Pointer MSB register.

Reserved:

The Reserved bits are status bits and must be ignored when this register is read.

ERDIE:

When a 1 is written to the RDIE interrupt enable bit position, a change in the path enhanced RDI state. will activate the interrupt (INT) output.

Register 0154H: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

NDFE:

When a 1 is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE:

When a 1 is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE:

When a 1 is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

Reserved

The Reserved[2:1] bits must be programmed to logic zero for proper operation of the SPECTRA-622.

INVNDFE:

When a 1 is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE:

When a 1 is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

ILLJREQE:

When a 1 is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Register 0155H: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register 0156H: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4	R	Reserved	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication, the auxiliary remote defect indication and the enhanced remote defect indication. When RDI10 is set high, the RDI and ERDI status is updated when the same value is received in the corresponding bit/bits of the G1 byte for 10 consecutive frames. When RDI10 is set low, the RDI and ERDI status is updated when the same value is received for 5 consecutive frames.

EXTD:

The EXTD bit extends the RPOP registers to facilitate additional mapping. If this bit is set to logic 1 the register mapping, for the RPOP Status and Control

register, the RPOP Alarm Interrupt Status register and the RPOP Alarm Interrupt Enable registers are extended.

NDFPOR:

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8xNDF_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Register 0157H: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register reports the path label byte in the receive stream..

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three or five consecutive frames as selected using the PSL5 bit in the RPOP Status and Control (EXTD=1) register.

Register 0158H: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Register 0159H: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]:

Bits BE[15:0] represent the number of path bit-interleaved parity errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPECTRA-622 Reset and Identity register. The write access transfers the internally accumulated error count to the path BIP-8 registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 015AH: RPOP Path REI LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 015BH: RPOP Path REI MSB

Bit	Type	Function	Default
Bit 7	R	FE[15]	X
Bit 6	R	FE[14]	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[15:0]:

Bits FE[15:0] represent the number of path remote error indications that have been received since the last time the Path REI registers were polled by writing to the SPECTRA-622 Reset and Identity register. The write access transfers the internally accumulated error count to the path REI registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 015CH: RPOP Tributary Multiframe Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	BLKREI	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register reports the status of the multiframe framer and enables interrupts due to framer events.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622 device.

COMAE:

The change of multiframe alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA-622 detect a change in the multiframe phase. When LOME is set high, an interrupt is generated upon change of multiframe alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI:

The change of multiframe alignment interrupt status bit (COMAI) is set high on changes in the multiframe alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

BLKREI:

When set high, the block REI bit (BLKREI) indicates that path REI counts are to be reported and accumulated on a block basis. A single REI error is accumulated if the received REI code is between 1 and 8 inclusive. When BLKREI is set low, REI errors are accumulated literally.

LOME:

The loss of multiframe interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multiframe indication (LOM).

When LOME is set high, an interrupt is generated upon loss of multiframe. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV:

The loss of multiframe status bit (LOMV) reports the current state of the multiframe framer monitoring the receive stream. LOMV is set high when loss of multiframe is declared and is set low when multiframe alignment has been acquired.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Register 015DH: RPOP Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register contains ring control bits.

BLKBIPO:

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported on a block basis. A single BIP error is reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. In inband error reporting mode, the REI count of the G1 byte is set on a block basis. When BLKBIPO is set low, BIP-8 errors are reported on a bit basis. In inband error reporting mode, the REI count of the G1 byte is set on a bit basis.DISFS:

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU3 carrying a VC3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 (STM-0/AU3) stream. This bit must be set low when the RPPS containing the RPOP is processing an STS-Nc (STM-1/AU4 or STM-4-Xc) stream.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic 1 is written to this bit, an incorrect SS bit pattern (i.e.,

b’10) will prevent RPOP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic 0 is written to this bit, the SS bits received do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic 1 is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic 0 is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Register 0174H: PMON Receive Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RPJE[7]	X
Bit 6	R	RPJE[6]	X
Bit 5	R	RPJE[5]	X
Bit 4	R	RPJE[4]	X
Bit 3	R	RPJE[3]	X
Bit 2	R	RPJE[2]	X
Bit 1	R	RPJE[1]	X
Bit 0	R	RPJE[0]	X

This register reports the number of positive pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate positive pointer justifications in the receive stream when the MONRS bit in the SPECTRA-622 RPPS Path/DS3 Configuration register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.

NOTE: Writing to this register initiates a transfer of all performance monitor counter values in the PMON's blocks into its holding registers. This transfer can be monitored with the TIP bit of register 0000H.

RPJE[7:0]:

Bits RPJE[7:0] represent the number of positive pointer justification events observed on the receive stream since the RPJE register was polled by writing to SPECTRA-622 Identity and Reset register. The write access transfers the internally accumulated error count to the RPJE register within 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0175H: PMON Receive Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RNJE[7]	X
Bit 6	R	RNJE[6]	X
Bit 5	R	RNJE[5]	X
Bit 4	R	RNJE[4]	X
Bit 3	R	RNJE[3]	X
Bit 2	R	RNJE[2]	X
Bit 1	R	RNJE[1]	X
Bit 0	R	RNJE[0]	X

This register reports the number of negative pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate negative pointer justifications in the receive stream when the MONRS bit in the SPECTRA-622 RPPS Path/DS3 Configuration register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.
NOTE: Writing to this register initiates a transfer of all performance monitor counter values in the PMON's blocks into its holding registers. This transfer can be monitored with the TIP bit of register 0000H.

RNJE[7:0]:

Bits RNJE[7:0] represent the number of negative pointer justification events observed on the receive side since the RNJE register was polled by writing to SPECTRA-622 Identity and Reset register. The write access transfers the internally accumulated error count to the RNJE register within 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0176H: PMON Transmit Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TPJE [7]	X
Bit 6	R	TPJE [6]	X
Bit 5	R	TPJE [5]	X
Bit 4	R	TPJE [4]	X
Bit 3	R	TPJE [3]	X
Bit 2	R	TPJE [2]	X
Bit 1	R	TPJE [1]	X
Bit 0	R	TPJE [0]	X

This register reports the number of positive pointer justification events that occurred on the corresponding transmit stream in the previous accumulation interval.
NOTE: Writing to this register initiates a transfer of all performance monitor counter values in the PMON's blocks into its holding registers. This transfer can be monitored with the TIP bit of register 0000H.

TPJE[7:0]:

Bits TPJE[7:0] represent the number of positive pointer justification events inserted in the transmit stream since the TPJE register was polled by writing to SPECTRA-622 Identity and Reset register. The write access transfers the internally accumulated error count to the TPJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0177H: PMON Transmit Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TNJE [7]	X
Bit 6	R	TNJE [6]	X
Bit 5	R	TNJE [5]	X
Bit 4	R	TNJE [4]	X
Bit 3	R	TNJE [3]	X
Bit 2	R	TNJE [2]	X
Bit 1	R	TNJE [1]	X
Bit 0	R	TNJE [0]	X

This register reports the number of negative pointer justification events that occurred on the corresponding transmit stream in the previous accumulation interval.
NOTE: Writing to this register initiates a transfer of all performance monitor counter values in the PMON's blocks into its holding registers. This transfer can be monitored with the TIP bit of register 0000H.

TNJE[7:0]:

Bits TNJE[7:0] represent the number of negative pointer justification events inserted in the transmit stream since the TNJE register was polled by writing to SPECTRA-622 Identity and Reset register. The write access transfers the internally accumulated error count to the TNJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0180H: RTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	SSS	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	DPJEE	0
Bit 0	R/W	IPAIS	0

This register allows the operation of the Receive Telecombus Aligner to be configured.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622 device.

IPAIS:

The insert path alarm indication signal (IPAIS) bit controls the insertion of PAIS in the DROP bus. When IPAIS is set high, path AIS is inserted in the DROP bus. The pointer bytes (H1, H2 and H3) and the entire SPE (VC) are set to all-ones. Path RDI indication is reported in the receive alarm port and to the companion TPOP in the SPECTRA-622. Normal operation resumes when the IPAIS bit is set low.

DPJEE:

The DROP bus pointer justification event interrupt enable bit (DPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the DROP bus. When DPJEE is set high, insertion of pointer justification events in the DROP bus will activate the interrupt (INTB) output. When DPJEE is set low, insertion of pointer justification events in the DROP bus will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events affect the

interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

SSS:

The set ss bit (SSS) controls the value of the ss field in the H1 pointer byte in the DROP bus. When SSS is set high, the ss bits are set to 'b10. When SSS is set low, the ss bits are set to 'b00.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the receive stream is placed on the DROP bus unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the RPPS containing the RTAL is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the RTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the receive stream is placed on the DROP bus unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the multiframe framer in the RPOP block.

Register 0181H: RTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

This register allows the control of the DROP bus interface and sensing of interrupt status.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622 device.

DLOP:

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the DROP bus is inverted causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

NPJI:

The DROP bus negative pointer justification interrupt status bit (NPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

PPJI:

The DROP bus positive pointer justification interrupt status bit (PPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

ESEI:

The DROP bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in RTAL underflows or overflows. This will cause the RTAL to reset

itself. It can thus loose the J1, and go out of AIS for a short period of time if it was in AIS state.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds. I.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 11 - Receive ESD[1:0] codepoints.

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definitions:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing negative justifications at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the RTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the RTAL will start generates outgoing positive justification at the rate of 1 in every 4 frames).

The interrupt bits (and the interrupt) are cleared when this register is read.

Register 0182H: RTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	H4AISB	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register reports alarms and controls diagnostics on the DROP bus.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622 device.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the DROP bus. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the DROP bus when a FIFO underflow or overflow has been detected in the elastic store. When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the DROP bus for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS on the DROP bus for VT1.5 (TU11), VT2 (TU12), VT3 and VT6 (TU2) payloads. When ITUAIS is set high, columns in the DROP bus carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the

path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit is not applicable for TU3 tributary payloads and the ITUAIS bit must be set low. The STM1-CONCAT register bit must be set for TU2, TU11 and TU12 payloads in a VC-4.

H4AISB:

The insert H4 AIS bits controls the insertion of the all-ones AIS pattern in the H4 byte. When H4AISB is set low, the H4 byte will be over-written with 'hFF when path AIS is inserted in the DROP bus. When H4AISB is set high, the H4 byte is not over-written during path AIS insertion.

Register 0190H: SPTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUE	0
Bit 4	R/W	RTIME	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive (for RPPS) and transmit (for corresponding TPPS) portions of the SPTB.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is set high, the path trace message length is 16 bytes. When LEN16 is set low, the path trace message length is 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, the RTIM and RTIU alarms are invalid and may cause spurious interrupts.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignore and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit path trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIME:

The receive path trace identifier (mode 1) mismatch interrupt enable bit (RTIME) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIME is set high, changes in match state activates the interrupt (INTB) output. When RTIME is set low, path trace identifier (mode 1) match/mismatch state changes will not affect INTB. This bit is should be disabled in Trace identifier Mode 2 since the RTIM is generate using the Mode 1 algorithm.

RTIUE:

The receive path trace identifier (mode 1) unstable interrupt enable bit (RTIUE) controls the activation of the interrupt output when the receive identifier message state (RTIUV) changes from stable to unstable and vice versa. State changes dependent on the Trace Identifier Mode. When RTIUE is set high, changes in the receive path trace identifier unstable (RTIUV) state will activate the interrupt (INTB) output. When RTIUE is set low, path trace identifier unstable state changes will not affect INTB.

TIMODE**:**

The Trace Identifier Mode is used to set the mode for the received path trace identifier. Setting this bit to low sets the Trace Identifier Mode to Mode 1. In this mode the path trace identifier is defined as a regular 16 or 64 byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message. Setting this bit to high sets the Trace Identifier Mode to Mode2. In this mode the path trace identifier is defined as a 16 byte message with a single repeating byte that is monitored for persistency and errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more byte errors are detected in three consecutive 16 byte windows. RTIM is not defined in this mode.

ZEROEN:

The zero enable bit (ZEROEN) is defined for Trace Identifier Mode 1 only and enables trace identifier mismatch (RTIM) assertion and removal based on an all ZEROs path trace message string. When ZEROEN is set high, all ZEROs path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs path trace message strings are ignored. Trace identifier unstable (RTIU) assertion and removal is not affected by setting this register bit.

Register 0191H: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	UNEQI	X
Bit 4	R	UNEQV	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

The receive path trace identifier mismatch status bit (RTIMV) is set high in Trace Identifier Mode 1 when the accepted message differs from the expected message. The accepted message is the last message to have been received 5 times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted path trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN register bit in the Control register is set. This bit is usually ignored in Trace Identifier Mode 2.

RTIMI:

The receive trace identifier mismatch indication status bit (RTIMI) is set high in Trace Identifier Mode 1 when the match/mismatch status (RTIMV) of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read. This bit is usually ignored in Trace Identifier Mode 2.

RTIUV:

The receive path trace identifier unstable status bit (RTIUV) is dependent on the Trace Identifier Mode. In Mode 1, the bit is set high when 8 trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (3 or 5 consecutive matching messages). RTIUV is set high when the unstable counter reaches 8.

RTIUV is set low and the unstable counter cleared once a persistent message has been received.
In Mode 2, RTIUV is set low during the stable state which is declared after having received the same 16 byte trace message 3 consecutive times (stable trace byte for forty-eight consecutive frames). The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected in three consecutive 16 byte windows. The 16 byte windows do not overlap and start immediately upon the first detected error.

RTIUI:

The receive path trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state. The setting of this bit is dependent on the unstable status (RTIUV) which is dependent on the Trace Identifier Mode. This bit and the interrupt are cleared when this register is read.

UNEQV:

The unequipped status bit (UNEQV) is dependent on the PSL Mode. In Mode 1, this bit is set high when the accepted path signal label indicates that the path connection is unequipped. UNEQV is set low when the accepted path signal label indicates the path connection is not unequipped.
When in PSL Mode 2, the UNEQV is set high upon the reception of five consecutive frames with an unequipped (00h) label. The bit is set low when five consecutive frames are received with a label other than the unequipped label. The five consecutive labels needed to lower the alarm do not need to be the same. The Assertion of UNEQV will automatically deassert the PSLM alarm.

UNEQI:

The unequipped indication status bit (UNEQI) is set high when the equipped/unequipped status (UNEQV) of the path connection changes state. The setting of this bit is dependent on the UNEQV status which is dependent on the PSL Mode. This bit (and the interrupt) is cleared when this register is read.

Register 0192H: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. If RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the addressed specified.

A[7:0]:

The indirect read address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J1 byte of the transmit stream. Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 191 reference the receive capture page while addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

A[7:0]	RAM Contents
0-3Fh	Transmit Trace Message
40h-7Fh	Receive Accepted Trace Message
80h-BFh	Receive Captured Trace Message
C0h-FFh	Receive Expected Trace Message

Register 0193H: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 0194H: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EX_PSL[7]	0
Bit 6	R/W	EX_PSL[6]	0
Bit 5	R/W	EX_PSL[5]	0
Bit 4	R/W	EX_PSL[4]	0
Bit 3	R/W	EX_PSL[3]	0
Bit 2	R/W	EX_PSL[2]	0
Bit 1	R/W	EX_PSL[1]	0
Bit 0	R/W	EX_PSL[0]	0

This register contains the expected path signal label byte in the receive stream.

EX_PSL[7:0]:

The EX_PSL[7:0] bits contain the expected path signal label byte (C2). In PSL Mode 1, EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. In PSL Mode 2, EPSL[7:0] is compared with the received path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if 5 consecutively received PSLs (other than 00h) differ from the expected PSL. If enabled, an interrupt is asserted upon declaration and removal of PSLM.

Register 0195H: SPTB Path Signal Label Control and Status:

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5	R/W	UNEQIE	0
Bit 4	R/W	PSLMODE	0
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV:

The receive path signal label mismatch status bit (RPSLMV) is dependent on the PSL Mode. In Mode 1, this bit reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is set high when the accepted PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL. In Mode 2, this bit reports the match/mismatch status between the expected and the received path signal label. RPSLMV is set high when the received PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL.

RPSLMI:

The receive path signal label mismatch interrupt status bit (RPSLMI) is set high when the match/mismatch (RPSLMV) status between the accepted and the expected path signal label changes state. The setting of this bit is dependent on the unstable status (RPSLMV) which is dependent on the PSL Mode. This bit (and the interrupt) is cleared when this register is read.

RPSLUV:

The receive path signal label unstable status bit (RPSLUV) is independent on the PSL Mode. This bit reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is set high when 5 labels that differ from its immediate predecessor is received. RPSLUV is set low and the unstable label count is reset when 5 consecutive identical labels are received.

RPSLUI:

The receive path signal label unstable interrupt status bit (RPSLUI) is set high when the stable/unstable (RPSLUV) status of the path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

PSLMODE**:**

The PSL Mode is used to set the mode used for the path signal label alarm algorithms. Setting this bit to low sets the PSL Mode to Mode 1. Setting this bit to high sets the PSL Mode to Mode 2.

UNEQE:

The unequipped interrupt enable bit (UNEQE) controls the activation of the interrupt output when the path signal label indicates the path connection has changed state from equipped to unequipped and vice versa. When UNEQE is set high, changes in unequipped state (UNEQI) activates the interrupt (INTB) output. When UNEQE is set low, unequipped state changes will not affect INTB.

RPSLME:

The receive path signal label mismatch interrupt enable bit (RPSLME) controls the activation of the interrupt output when the comparison between accepted and the expected path signal label changes state from match to mismatch and vice versa. When RPSLME is set high, changes in match state (RPSLMI) activates the interrupt (INTB) output. When RPSLME is set low, path signal label state changes will not affect INTB.

RPSLUE:

The receive path signal label unstable interrupt enable bit (RPSLUE) controls the activation of the interrupt output when the received path signal label changes state from stable to unstable and vice versa. When RPSLUE is set high, changes in stable state (RPSLUI)activates the interrupt (INTB) output. When RPSLUE is set low, path signal label state changes will not affect INTB.

Register 0196H: SPTB Path Trace Operation

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. The access will be performed when the SPTB Indirect Address register is written to.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to the path trace RAM has been completed. BUSY is set high upon writing to the SPTB Path Trace Indirect Address register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the SPTB Indirect Data register. The maximum latency for the BUSY to return low is 10 us.

Register 01B0H: D3MD Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	DS3AISGEN	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

DS3AISGEN:

The active high DS3 Alarm Indication Signal enable bit (DS3AISGEN) configures the D3MD to generate a DS3 AIS signal. Any data on the STS-1 (STM-0/AU3) SPE is lost due to the assertion of DS3AISGEN. DS3AISGEN bit is logically ORed with the associated time-slot of the DPAIS input and internal alarm indications as controlled using the SPECTRA-622 RPPS Path/DS3 AIS Control register.

Register 01B1H: D3MD Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

UFLI

When set high, this bit indicates that an underflow condition has occurred in the D3MD elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When set high, this bit indicates that an overflow condition has occurred in the D3MD elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 01B2H: D3MD Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLE	0
Bit 0	R/W	UFLE	0

UFLE:

When set high, this bit enables generation of an interrupt if a D3MD elastic store underflow condition occurs (UFLI='1').

OFLE:

When set high, this bit enables generation of an interrupt if a D3MD elastic store overflow condition occurs (OFLI='1').

Register 01D0H: DPGM Generator Control #1

Bit	Type	Function	Default
Bit 7	R/W	GEN_A1A2_EN	0
Bit 6	R/W	GEN_INV_PRBS	0
Bit 5	R/W	GEN_AUTO	0
Bit 4	R/W	GEN_FERR	0
Bit 3	R/W	GEN_SIGE	0
Bit 2	R/W	GEN_FSENB	0
Bit 1	R/W	GEN_REGEN	0
Bit 0	R/W	GEN_EN	0

GEN_EN:

The Generator Enable (GEN_EN) bit enables the insertion of a pseudo random bit sequence (PRBS) into the DROP Bus payload. When GEN_EN is set high, the PRBS bytes will overwrite the processed payload data. When GEN_EN is set low, the incoming payload is unaltered. This bit has not effect in Autonomous Input Mode. When set, it is recommended to set the GEN_SIGE bit in slave slices to detect DFP frame realigment. This mode can not be used in the STS-12c configuration when in DTMODE.

GEN_REGEN:

The Generator Regenerate (GEN_REGEN) bit can be used to re-initialize the generator LFSR and begin regenerating the pseudo random bit sequence (PRBS) from the known reset state. The LFSR reset state is dependent on the set sequence number. Setting this bit in a master generator will automatically force all slaves to reset at the same time. This bit will clear itself when the operation is complete. Upon a frame realignment on the DROP bus the Generators must be regenerated.

GEN_FSENB:

The Generator Fixed Stuff Enable (GEN_FSENB) bit determines whether the pseudo random bit sequence (PRBS) is inserted into the (STS-1/STM0) fixed stuff bytes of the processed payload. When set to logic one, the PRBS is not inserted into the fixed stuff bytes and the bytes are outputted unaltered. When set to logic zero, the PRBS is inserted into the fixed stuff bytes. The fixed stuff columns are columns 30 and 59 of the STS-1 payload. GEN_FSEN should be disabled when using the generator in master/slave configuration to support de-multiplexed concatenated payloads.

GEN_SIGE:

The Generator Signature Interrupt Enable (GEN_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When GEN_SIGE is set high, a change in the signature verification state (GEN_SIGV) will trigger an interrupt. When GEN_SIGE is set low, no interrupt will be asserted. When in generator or autonomous mode, and for STS-3c and STS-12c only, DFP frame realigment can be detected by setting this bit for slave slices.

GEN_FERR:

The Generator Force Error (GEN_FERR) bit is used to force bit errors in the inserted pseudo random bit sequence (PRBS). When logic one is written to this bit, the MSB of the PRBS byte will be inverted, inducing a single bit error. The register bit will clear itself when the operation is complete.
A second forced error must not be attempted for at least three GCLK clock cycles after this bit has been read back to ‘0’.

GEN_AUTO:

The Generator Autonomous Mode (GEN_AUTO) bit places the Generator in the Autonomous Input Mode. In this mode the payload frame is forced to an active offset of zero. The generated frame will have all zeros TOH and POH bytes. The H1, H2 pointer bytes are set to indicate an active SPE/VC offset of zero, the SS bits are also both set to zero. The payload will be filled with a PRBS. When a logic zero is written to this bit, the active offset is determined by the received stream. When set, it is recommended to set the GEN_SIGE bit in slave slices to detect DFP frame realigment. This mode can not be used in the STS-12c configuration when in DTMODE. It can not also be used in bypass mode, when the RESBYP bit of register 0n00H is set.

GEN_INV_PRBS:

The Generator Invert PRBS (GEN_INV_PRBS) bit is used to invert the calculated PRBS byte before insertion into the payload. Setting this bit to logic 1 enables the logic inversion of all PRBS bits before insertion into the payload. Setting this bit to logic 0 does not invert the generated PRBS.

GEN_A1A2_EN:

The Generator Framing A1/A2 Enable (GEN_A1A2_EN) bit enables the insertion of the F6h and 28h bit pattern in the A1 and A2 respective byte positions of the processed stream. Setting to logic 1 this bit enables the A1 and A2 byte insertion. Setting this bit to logic 0 passes through the input A1 & A2 bytes unaltered. This feature has priority over the all zero A1/A2 generated in Autonomous Input Mode.

Register 01D1H: DPGM Generator Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	GEN_H4_EN	0
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

GEN_H4_EN:

The Generator multi-frame indicator H4 Enable (GEN_H4_EN) bit enables the insertion of the H4 indicator into the H4 byte position of the processed payload. Setting to logic 1 this bit enables the insertion of a valid H4 byte. The inserted value of H4 is derived from the received stream H4 byte. This feature is duplicated in the RTAL block. By default RTAL should be used to insert H4. This bit should only be used when the RTAL FIFO is bypassed.

Register 01D2H: DPGM Generator Concatenate Control

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	GEN_SEQ[3]	1
Bit 4	R/W	GEN_SEQ[2]	1
Bit 3	R/W	GEN_SEQ[1]	1
Bit 2	R/W	GEN_SEQ[0]	1
Bit 1	R/W	GEN_GMODE[1]	0
Bit 0	R/W	GEN_GMODE[0]	0

GEN_GMODE[1:0]:

The GEN_GMODE[1:0] bits control the operational mode of the pseudo random sequence generator as summarized in the table below. When GEN_GMODE[1:0] is set to 'b00, the generator will generate the complete sequence for an STS-1 (STM-0/AU3) stream. When GEN_GMODE[1:0] is set to 'b01, the generator will generate one third or 1 in 3 bytes of the complete sequence for an STS-1 (STM-0/AU3) equivalent in an STS-3c (STM-1/AU4) stream. When GEN_GMODE[1:0] is set to 'b10, the generator will generate one twelfth or 1 in 12 bytes of the complete sequence for an STS-1 (STM-0/AU3) equivalent in an STS-12c (STM-4-4c) stream.

GEN_GMODE [1:0]	Generator Gap Mode Description
00	**1in1 Gap Mode**. Generator inserts the complete PRBS.
01	**1in3 Gap Mode**. Generator generates 1 of 3 (1in3) PRBS bytes. The generator will also generate 1in2 bytes to skip over POH columns.
10	**1in12 Gap Mode**. The generator generates 1 of 12 (1in12) PRBS bytes. The generator will also generate 1in8 bytes to skip over POH or fixed stuff columns.
11	Reserved

GEN_SEQ[3:0]

The Generator Sequence (GEN_SEQ[3:0]) sets the reset state of the LFSR and places the generator in the master or slave mode. The sequence number identifies the multiplexing order of the outgoing data into the concatenating stream. The sequence number also affects the signature bit calculation.

GEN_SEQ [3:0]	Mode	Signature bit	Reset Value
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.	All Ones.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.	Master+8 states
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.	Master+16 states
0011	Slave3	72nd PRBS bit from current state. MSB of 9th PRBS byte.	Master+24 states
0100	Slave4	64th PRBS bit from current state. MSB of 8th PRBS byte.	Master+32 states
0101	Slave5	56th PRBS bit from current state. MSB of 7th PRBS byte.	Master+40 states
0110	Slave6	48th PRBS bit from current state. MSB of 6th PRBS byte.	Master+48 states
0111	Slave7	40th PRBS bit from current state. MSB of 5th PRBS byte.	Master+54 states
1000	Slave8	32nd PRBS bit from current state. MSB of 4th PRBS byte.	Master+64 states
1001	Slave9	24th PRBS bit from current state. MSB of 3rd PRBS byte.	Master+72 states
1010	Slave10	16th PRBS bit from current state. MSB of 2nd PRBS byte.	Master+80 states
1011	Slave11	8th PRBS bit from current state. MSB of next PRBS byte.	Master+88 states
1100-1110		Reserved	
1111		Reserved	

Register 01D3H: DPGM Generator Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	GEN_SIGI	X
Bit 0	R	GEN_SIGV	X

GEN_SIGV:

The Generator Signature Status (GEN_SIGV) bit indicates if the partial pseudo random sequence (PRBS) begin generated is correctly aligned with the partial PRBS begin generated in the master generator. When GEN_SIGV is low, the signature verification is a match, and the partial PRBS is aligned with that of the master. When GEN_SIGV is high, the signature verification is a mismatch, and the partial PRBS is not aligned with that of the master.
If non-alignment persists, a forced re-start of the sequence generation by all generators processing the concatenated stream should be initiated using the GEN_REGEN register bit in the master generator. This bit is only valid in slave generators and when out of alignment may toggle high and low. Persistent reads at low or reading the interrupt at low assures that the signature is correct.

GEN_SIGI:

The Generator Signature Interrupt Status (GEN_SIGI) bit indicates a change in the signature verification state (GEN_SIGV) by a slave generator. When GEN_SIGI is set high, the slave generator has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit will continuously be set when in the out of alignment state since the status GEN_SIGV will toggle. This bit is only valid in slave generators.

Register 01D8H: DPGM Monitor Control #1

Bit	Type	Function	Default
Bit 7	R/W	MON_AUTORESYNC	1
Bit 6	R/W	MON_INV_PRBS	0
Bit 5	R/W	MON_SYNCE	X
Bit 4	R/W	MON_ERRE	0
Bit 3	R/W	MON_FSENB	0
Bit 2	R/W	MON_SIGE	0
Bit 1	R/W	MON_RESYNC	0
Bit 0	R/W	MON_EN	0

MON_EN:

The Monitor Enable (MON_EN) bit enables the monitoring of a pseudo random bit sequence (PRBS) in the processed payload. When MON_EN is set high, the incoming payload is extracted and the data monitored for the PRBS. When MON_EN is set low, no monitoring on the data is done.

MON_RESYNC:

The Monitor Resynchronize (MON_RESYNC) bit allows a forced resynchronization of the monitor to the incoming pseudo random bit sequence (PRBS). When set to logic one, the monitor's will go out of synchronization and begin re-synchronizing the to the incoming PRBS payload. Setting this bit in a master monitor will automatically force all slaves to re-synchronize at the same time. This register bit will clear itself when the re-synchronizing has been triggered.

MON_SIGE:

The Monitor Signature Interrupt Enable (MON_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When MON_SIGE is set high, a change in the signature verification state (MON_SIGV) will trigger an interrupt. When MON_SIGE is set low, no interrupt is reported. Note: This bit is ignored in a master DPGM.

MON_FSENB:

The Monitor Fixed Stuff Enable (MON_FSENB) bit determines whether a PRBS is monitored for in the fixed stuff columns (columns 30 and 59) of the processed payload. When logic one is written to this bit, the PRBS is not monitored for in the fixed stuff columns. When a logic zero is written to this bit, the PRBS is monitored for in the fixed stuff columns. MON_FSENB should be

disabled when using the monitor in master/slave configuration to support de-multiplexed concatenated payloads.

MON_ERRE:

The Monitor Byte Error Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when a PRBS byte error has been detected in the incoming payload. When MON_ERRE is set high, a detected PRBS error in the incoming data will trigger an interrupt. When MON_ERRE is set low, no interrupt is generated.

MON_SYNCE:

The Monitor Synchronize Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when change in the synchronization state of the monitor occurs. When MON_SYNCE is set high, a change in the synchronization state (MON_SYNCV) will trigger an interrupt. When MON_SYNCE is set low, no interrupt is generated.

MON_INV_PRBS:

The Monitor Invert PRBS (MON_INV_PRBS) bit is used to invert the received payload data before monitoring the data for a pseudo random bit sequence (PRBS). When set to logic 1, the incoming payload PRBS bits are inverted before being verified against the monitor expected PRBS. When set to logic 0, the incoming payload PRBS is not inverted and verified as is.

MON_AUTORESYNC:

The Monitor Automatic Resynchronization (MON_AUTORESYNC) bit enables the automatic resynchronization of the monitor after detecting 16 consecutive PRBS byte errors. Setting this bit to logic 1, enables the monitor to automatically fall out of synchronization after 16 consecutive errors. Once out of synchronization, the monitor will attempt to resynchronize to the incoming PRBS and verify the synchronization with 32 consecutive PRBS matches. Setting this bit to logic 0 disables the automatic resynchronization

Register 01D9H: DPGM Monitor Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

Register 01DAH: DPGM Monitor Concatenate Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	MON_SEQ[3]	1
Bit 4	R/W	MON_SEQ[2]	1
Bit 3	R/W	MON_SEQ[1]	1
Bit 2	R/W	MON_SEQ[0]	1
Bit 1	R/W	MON_GMODE[1]	1
Bit 0	R/W	MON_GMODE[0]	1

MON_GMODE[1:0]:

The MON_GMODE[1:0] bits control the operational mode of the pseudo random sequence monitor as summarized in the table below. When MON_GMODE[1:0] is set to 'b00, the monitor expects the complete sequence for an STS-1 (STM-0/AU3) stream. When MON_GMODE[1:0] is set to 'b01, the monitor expects one third or 1 in 3 bytes of the complete sequence in an STS-1 (STM-0/AU3) equivalent of an STS-3c (STM-1/AU4) stream. When MON_GMODE[1:0] is set to 'b10, the monitor expects one twelfth or 1 in 12 bytes of the complete sequence in an STS-1 (STM-0/AU3) equivalent of an STS-12c (STM-4-4c) stream.

MON_GMODE [1:0]	Monitor Gap Mode Description
00	**1in1 Gap Mode**. Monitor monitors for a complete PRBS.
01	**1in3 Gap Mode**. Monitor will monitor for the presence of every 3rd PRBS byte. The Monitor will also monitor for every 2nd PRBS byte after the POH columns.
10	**1in12 Gap Mode**. Monitor will monitor for the presence of every 12th PRBS byte. The Monitor will also monitor for every 8th PRBS byte after the POH and fixed stuff columns.
11	Reserved

MON_SEQ[3:0]

The Monitor Sequence (MON_SEQ[3:0]) sets the Monitor in master or slave mode and is used to identify the multiplexed order of the monitored data in

the concatenated payload. The sequence order affects the signature bit calculation.

MON_SEQ [3:0]	Mode	Signature bit
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.
0011	Slave3	72nd PRBS bit from current state. MSB of 9th PRBS byte.
0100	Slave4	64th PRBS bit from current state. MSB of 8th PRBS byte.
0101	Slave5	56th PRBS bit from current state. MSB of 7th PRBS byte.
0110	Slave6	48th PRBS bit from current state. MSB of 6th PRBS byte.
0111	Slave7	40th PRBS bit from current state. MSB of 5th PRBS byte.
1000	Slave8	32nd PRBS bit from current state. MSB of 4th PRBS byte.
1001	Slave9	24th PRBS bit from current state. MSB of 3rd PRBS byte.
1010	Slave10	16th PRBS bit from current state. MSB of 2nd PRBS byte.
1011	Slave11	8th PRBS bit from current state. MSB of next PRBS byte.
1100-1110		Reserved
1111		Reserved

Register 01DBH: DPGM Monitor Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	MON_ERRI	X
Bit 3	R	MON_SYNCI	X
Bit 2	R	MON_SYNCV	X
Bit 1	R	MONS_SIGI	X
Bit 0	R	MONS_SIGV	X

MON_SIGV:

The Monitor Signature Status (MON_SIGV) bit indicates if the partial pseudo random sequence (PRBS) being monitored for is correctly aligned with the partial PRBS being monitored for by the master generator. When MON_SIGV is low, the signature verification is a match, and the calculated partial PRBS is aligned with that of the master. When MON_SIGV is high, the signature verification is a mismatch, and the calculated partial PRBS is not aligned with that of the master. This bit does not identify if it is the master or the slave that is out of sync, it only says that they are not in sync one relative to the other. If non-alignment persists, a forced re-synchronization of all monitors processing the concatenated stream should be initiated using the MON_RESYNC register bit in the master generator. This bit is only valid in slave generators.

MON_SIGI:

The Monitor Signature Interrupt Status (MON_SIGI) bit indicates a change in the signature verification state (MON_SIGV) by a slave monitor. When MON_SIGI is set high, the Monitor has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit is only valid in slave monitor.

MON_SYNCV:

The Monitor Synchronize Status (MON_SYNCV) is set high when the monitor is out of synchronization. The monitor falls out of synchronization after detecting 16 consecutive mismatched PRBS bytes or being forced to re-synchronize. A forced re-synchronize may be due to setting the MON_RESYNC register bit or a master generator. Once out of synchronization, the Synchronized State can only be achieved after re-

synchronizing to the incoming PRBS and verifying the resynchronization with 32 consecutive non-erred PRBS bytes. This bit is set low when in the Synchronized State. This bit is local to each slice so it should be monitored in the master and all its slaves.

MON_SYNCI:

The Monitor Synchronize Interrupt Status (MON_SYNCI) bit indicates a change in the synchronization state (MON_SYNCV) of the monitor. When MON_SYNCI is set high, the monitor has transitioned from the Synchronized to Out of Synchronization State or vice versa. This bit is cleared when this register is read.

MON_ERRI:

The Monitor Byte Error Interrupt Status (MON_ERRI) bit indicates that an error has been detected in the received PRBS byte while the monitor was in the Synchronized State. MON_ERRI is set high, when one or more PRBS bit errors have been detected in the received PRBS data byte. This bit is cleared when this register is read.

Register 01DCH: DPGM Monitor Error Count #1

Bit	Type	Function	Default
Bit 7	R	PRSE[7]	X
Bit 6	R	PRSE[6]	X
Bit 5	R	PRSE[5]	X
Bit 4	R	PRSE[4]	X
Bit 3	R	PRSE[3]	X
Bit 2	R	PRSE[2]	X
Bit 1	R	PRSE[1]	X
Bit 0	R	PRSE[0]	X

Register 01DDH: DPGM Monitor Error Count #2

Bit	Type	Function	Default
Bit 7	R	PRSE[15]	X
Bit 6	R	PRSE[14]	X
Bit 5	R	PRSE[13]	X
Bit 4	R	PRSE[12]	X
Bit 3	R	PRSE[11]	X
Bit 2	R	PRSE[10]	X
Bit 1	R	PRSE[9]	X
Bit 0	R	PRSE[8]	X

PRSE[15:0]:

The PRSE[15:0] bits represent the number of PRBS byte errors detected since the last accumulation interval. Errors are only accumulated in the synchronized state and each PRBS data byte can have a maximum of 1 errors. The transfer of the error accumulation counter to these registers is triggered by a write to either of the GPGM Monitor Error Counters, or , to the Accumulation Trigger register (0000H). The content of these registers will be valid only 4 clock cycles after the transfer is triggered. For concatenated payload, the master slice and each slave work independently from one another, thus the error count is the sum of all the slices.

Register 0D01H: SPECTRA-622 DROP Bus STM-1 #1 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU3 #1 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D02H: SPECTRA-622 DROP Bus STM-1 #2 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU3 #1 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D03H: SPECTRA-622 DROP Bus STM-1 #3 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU3 #1 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D04H: SPECTRA-622 DROP Bus STM-1 #4 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU3 #1 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D05H: SPECTRA-622 DROP Bus STM-1 #1 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU3 #2 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D06H: SPECTRA-622 DROP Bus STM-1 #2 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU3 #2 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D07H: SPECTRA-622 DROP Bus STM-1 #3 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU3 #2 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D08H: SPECTRA-622 DROP Bus STM-1 #4 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU3 #2 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D09H: SPECTRA-622 DROP Bus STM-1 #1 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU3 #3 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D0AH: SPECTRA-622 DROP Bus STM-1 #2 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU3 #3 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D0BH: SPECTRA-622 DROP Bus STM-1 #3 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU3 #3 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D0CH: SPECTRA-622 DROP Bus STM-1 #4 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation at the Telecom DROP bus. This register selects an STS-1 (STM-0/AU3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU3 #3 of the DROP bus. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the DROP bus.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 0D30H: SPECTRA-622 DROP Bus Configuration

Bit	Type	Function	Default
Bit 7	R/W	DTMODE	0
Bit 6	R/W	DMODE[1]	0
Bit 5	R/W	DMODE[0]	0
Bit 4	R/W	RESBYP	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ODDPD	0
Bit 1	R/W	INCDPL	0
Bit 0	R/W	INCDC1J1V1	0

This register allows the parity insertion in the DROP bus of the SPECTRA-622 to be configured.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

INCDC1J1V1:

The INCDC1J1V1 bit controls whether the composite timing signals, DC1J1V1[4:1], on the DROP buses are used to calculate the corresponding parity signals, DDP[4:1]. When INCDC1J1V1 is set high, the parity signal set includes the DC1J1V1[4:1] signals. When INCDC1J1V1 is set low, parity is calculated without regard to the state of the corresponding DC1J1V1 signal on the DROP bus.

INCDPL:

The INCDPL bit controls whether the payload active signals, DPL[4:1], on the DROP buses are used to calculate the corresponding parity signals, DDP[4:1]. When INCDPL is set high, the parity signal set includes the DPL[4:1] signals. When INCDPL is set low, parity is calculated without regard to the state of the corresponding DPL signal on the DROP bus.

ODDPD:

The ODDPD bit controls the parity placed on the DROP bus parity signals, DDP[4:1]. When set high, the ODDPD bit configures the bus parity to be odd. When set low, the ODDPD bit configures the bus parity to be even.

RESBYP:

When set high, the RESBYP bit forces the elastic store (RTAL) in the Receive Path Processing Slices to be bypassed. The DROP bus stream will be synchronous to the receive stream. The DCK input must be connected to the PGMRCLK output. The transport frame on the DROP bus will be locked to the receive stream and the DFP input is ignored. Once in bypass mode, the V1 pulse will always be outputted on the DROP bus and the autonomous mode of the DPGM is no longer functional. See section 11.7.3.3

DTMODE:

The DROP Telecom bus mode select (DTMODE) bit is used to select the operation of the DROP Bus system side interface when Telecom mode is enabled. When the DTMODE bit is set low, the single (STM-4) 77.76 MHz byte Telecom DROP Bus Interface is supported. When the DTMODE bit is set high, the four (STM-1) 19.44 MHz byte Telecom DROP Bus Interface is supported.. Note that when in 19.44 MHz telecombus mode, drop bus DLL 00A4H override bit should be set to 1

DMODE:[1:0]

The DROP bus mode select (DMODE[1:0]) bits are used to select the operation of the DROP Bus system side interface. The interface may be configured as Telecom mode only, DS3 mode only or Dual Telecom and DS3 mode. In Telecom mode, only the Telecom DROP bus interface is active. The DROP DS3 blocks are held in reset and the DS3 interface output signals are forced low. In DS3 mode, only the DS3 DROP bus interface is active. The DS3 Telecom blocks are held in reset and the Telecom interface output signals are forced low. In Dual mode, both the DROP Telecom and DS3 interfaces are enabled and all DROP blocks are functioning. The DROP bus mode may also be set via the DMODE[1:0] inputs. The DMODE[1:0] register bits override the mode set via the DMODE[1:0] input pins. By default the input pins are used to set the DROP bus mode.

DMODE[1:0]	Selected DROP Mode
01	Telecom Mode
10	DS3 Mode
11	Dual Mode
00	Mode selected via DMODE[1:0] inputs

Register 1030H: SPECTRA-622 ADD Bus Configuration

Bit	Type	Function	Default
Bit 7	R/W	AFPEN	0
Bit 6	R/W	ATMODE	0
Bit 5	R/W	TESBYP	0
Bit 4	R/W	ATSICLK_RST	0
Bit 3	R/W	ATSICLK_ISOLATE	0
Bit 2	R/W	ODDPA	0
Bit 1	R/W	INCAPL	0
Bit 0	R/W	INCAC1J1V1	0

This register allows the ADD bus of the SPECTRA-622 to be configured.

INCAC1J1V1:

The INCAC1J1V1 bit controls whether the composite timing signals (AC1J1V1[4:1]) in the ADD buses are used to calculate the corresponding parity signals (ADP[4:1]). When INCAC1J1V1 is set high, the parity signal set includes the AC1J1V1[4:1] signals. When INCAC1J1V1 is set low, parity is calculated without regard to the state of the corresponding AC1J1V1 signal.

INCAPL:

The INCAPL bit controls whether the payload active signals (APL[4:1]) in the ADD busses are used to calculate the corresponding parity signals (ADP[4:1]) and whether the payload active signals (APL[4:1]) in the ADD busses are included in the condition to set high the ACA[4:1] activity monitors. When INCAPL is set high, the parity signal set includes the APL[4:1] signals and the condition to set the ACA[4:1] activity monitors bits includes these signals. When INCAPL is set low, parity is calculated without regard to the state of the corresponding APL signal and the activity monitor will be set high even when the APL signals do not toggle.

ODDPA:

The ODDPA bit controls the parity expected on the ADD bus parity signal (ADP[4:1]). When set high, the ODDPA bit configures the ADD bus parity to be odd. When set low, the ODDPA bit configures the ADD bus parity to be even.

ATSICLK_ISOLATE

The ATSI_ISOLATE bit is used to disable the realignment by AC1J1V1/AFP[1] ADD BUS pin on the generated system side clocks of the 12 TPPS slices in the ADD TSI. This bit should only be used when all 12 TPPS slices are placed in Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) ADD BUS interface can not maintain a constant frame alignment (C1 or FP moving around). Programming this bit to logic one will mask low AC1J1V1/AFP[1] pin and the generated clocks will fly-wheel on the last C1 or FP received on AC1J1V1/AFP[1]. The data from the ADD Bus can thus not be analyzed or monitored. Programming this bit to logic zero has not affect. This bit is mainly for diagnostic purpose and to let the user isolate the 12 TPPS slices from the ADD bus.

ATSICLK_RST

The ATSICLK_RST bit is used to force a constant realignment of the system side clocks generated in the TPPS's. This bit can be used in conjunction with ATSICLK_ISOLATE to force the alignment of the generated clocks. When programmed high the generated clocks are disabled and realign. Upon programming the bit to logic zero, the generated clocks will start again in a known sequence with slice #1 clocked first.

TESBYP:

When set high, the TESBYP bit forces the elastic store (TTAL) in the Transmit Path Processing Slice (TPPS) to be bypassed. The transmit stream will be synchronous to the ADD bus. The ACK input must be connected to the PGMTCLK output. The transport frame in the transmit stream will be locked to that on the ADD bus and the TFPI input is ignored. See section 11.8.4.3. After a reset this bit or the TCLKEN bit of register 0004H needs to be set for a few clock cycle to activate the TX line interface.

ATMODE:

The ADD Telecom bus mode select (ATMODE) bit is used to select the operation of the ADD Bus system side interface when Telecom mode is enabled. When the ATMODE bit is set low, the single (STM-4) 77.76 MHz byte Telecom ADD Bus Interface is supported. When the AMTODE bit is set high, the four (STM-1) 19.44 MHz byte Telecom ADD Bus Interface is supported. In this mode, all the four AC1J1V1[4:1]/AFP[4:1] must be aligned

AFPEN:

The ADD bus reference frame position input enable (AFPEN) bit controls the interpretation of the AC1J1V1[4:1]/AFP[4:1] input signals. When set high, the AC1J1V1[4:1]/AFP[4:1] signals provide the ADD bus reference frame position

(AFP) indications to the corresponding ADD buses. When set low, the AC1J1V1[4:1]/AFP[4:1] signals provide the ADD bus composite timing signals (AC1J1V1) to the corresponding ADD buses. (See Table 8 System Side Add Bus Configuration Operation for the programming of this bit). In both cases, all the four AC1J1V1[4:1/AFP[4:1] must be aligned.

Register 1032H: SPECTRA-622 ADD Bus Parity Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	APE1	0
Bit 6	R/W	APE2	0
Bit 5	R/W	APE3	0
Bit 4	R/W	APE4	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

APEn:

The ADD bus parity interrupt enable (APIEn) bit controls the assertion of an interrupt when a parity error event is indicated by the corresponding parity interrupt status in the SPECTRA-622 ADD Bus Parity Interrupt Status register. When APEn is set high, an interrupt will be asserted (INTB set low) on a parity error event indication. When APEn is set low, parity error events will not affect the interrupt output (INTB).

Register 1034H: SPECTRA-622 ADD Bus Parity Interrupt Status

Bit	Type	Function	Default
Bit 7	R	API1	X
Bit 6	R	API2	X
Bit 5	R	API3	X
Bit 4	R	API4	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register reports the parity interrupt status of the SPECTRA-622 Telecom ADD buses #1 (AD[7:0]), #2 (AD[15:8]), #3 (AD[23:16]) and #4 (AD[31:24]).

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

APIn:

The ADD bus parity interrupt status (APIn) bit reports parity error events detected at the ADD bus #n. APIn is set high on detection of a parity error event on the ADD bus #n. This bit and the interrupt are cleared when this register is read. The occurrence of parity error events is an indication of mis-configured parity generation/detection or actual hardware problem at the ADD bus input.

Register 1036H: SPECTRA-622 System Side Clock Activity Monitor

Bit	Type	Function	Default
Bit 7	R	ACKA	X
Bit 6	R	DCKA	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	DS3RICLKA	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides activity monitoring on SPECTRA-622 system-side clock inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

DS3RICLKA:

The DS3RICLK active (DS3RICLKA) bit monitors for low to high transitions on the DS3RICLK input. DS3RICLKA is set high on a rising edge of DS3RICLK, and is set low when this register is read.

DCKA:

The DCK active (DCKA) bit monitors for low to high transitions on the DCK input. DCKA is set high on a rising edge of DCK, and is set low when this register is read.

ACKA:

The ACK active (ACKA) bit monitors for low to high transitions on the ACK input. ACKA is set high on a rising edge of ACK, and is set low when this register is read.

Register 1037H: SPECTRA-622 ADD Bus Signal Activity Monitor

Bit	Type	Function	Default
Bit 7	R	ADA1	X
Bit 6	R	ACA1	X
Bit 5	R	ADA2	X
Bit 4	R	ACA2	X
Bit 3	R	ADA3	X
Bit 2	R	ACA3	X
Bit 1	R	ADA4	X
Bit 0	R	ACA4	X

This register provides activity monitoring on SPECTRA-622 signal and data inputs for byte ADD Telecombus operation. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

ACAn:

The ADD bus control active (ACAn) bit monitors for low to high transitions on the corresponding APL[n], AC1J1V1[n] and ADP[n] inputs. ACAn is set high when rising edges have been observed on all these signals, and is set low when this register is read In applications where APL may be tied low, APL may be excluded from the activity monitor status using the INCAPL register bit. If ADP is tied low or high, no activity will be detected on these bits.

ADAn:

The ADD bus data active (ADAn) bit monitors for low to high transitions on the corresponding AD[7:0] (#1), AD[15:8] (#2), AD[23:16] (#3) or AD[31:24] (#4) bus when configured for byte Telecom ADD bus mode. ADAn is set high when rising edges have been observed on all the required signals in the corresponding Telecom ADD bus, and is set low when this register is read.

Register 1061H: SPECTRA-622 ADD Bus STM-1 #1 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #1 AU3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) ADD bus stream as summarized in the table below.

STM1SEL[1:0]	STM-1 ADD bus stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1062H: SPECTRA-622 ADD Bus STM-1 #2 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #2 AU3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1063H: SPECTRA-622 ADD Bus STM-1 #3 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #3 AU3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1064H: SPECTRA-622 ADD Bus STM-1 #4 AU3 #1 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #4 AU3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1065H: SPECTRA-622 ADD Bus STM-1 #1 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #1 AU3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1066H: SPECTRA-622 ADD Bus STM-1 #2 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #2 AU3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1067H: SPECTRA-622 ADD Bus STM-1 #3 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #3 AU3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1068H: SPECTRA-622 ADD Bus STM-1 #4 AU3 #2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	0
Bit 0	R/W	AU3SEL[0]	1

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #4 AU3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1069H: SPECTRA-622 ADD Bus STM-1 #1 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #1 AU3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 106AH: SPECTRA-622 ADD Bus STM-1 #2 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #2 AU3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 106BH: SPECTRA-622 ADD Bus STM-1 #3 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #3 AU3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 106CH: SPECTRA-622 ADD Bus STM-1 #4 AU3 #3 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU3SEL[1]	1
Bit 0	R/W	AU3SEL[0]	0

This is a configuration register for the Time-Slot Interchange operation on the Telecom ADD bus. This register selects an STS-1 (STM-0/AU3) or equivalent on the ADD bus for insertion in time-slot STM-1 #4 AU3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the ADD bus to the transmit stream.

AU3SEL[1:0]:

The AU3SEL[1:0] bits select one of three STS-1 (STM-0/AU3) streams on the STS-3 (STM-1) ADD bus stream selected by the STM1SEL[1:0] bits. The AU3SEL[1:0] options are summarized in the table below.

AU3SEL[1:0]	AU3 receive stream #
00	STS-1 (STM-0/AU3) #1
01	STS-1 (STM-0/AU3) #2
10	STS-1 (STM-0/AU3) #3
11	Reserved

STM1SEL[1:0]:

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1100H: SPECTRA-622 TPPS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MASTER	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	STM1-CONCAT	0
Bit 4	R/W	SLLBEN	0
Bit 3	R/W	DS3SLLBEN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RXSEL[1]	0
Bit 0	R/W	RXSEL[0]	0

This register allows the operational mode of the SPECTRA-622 Transmit Path Processing Slice (TPPS) to be configured.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

RXSEL[1:0]:

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to ‘b00, the receive section is chosen to be one in the local SPECTRA-622. The path REI count and path RDI status of the transmit stream is derived from the local RPOP. When RXSEL[1:0] is set to ‘b01, a remote receive section is chosen and it reports the detected path BIP-8 error count and the path AIS status of its DROP bus via the transmit alarm port. The path status byte in the transmit stream carries the path REI and path RDI indications reported in the transmit alarm port. When RXSEL[1:0] is set to ‘b10, inband error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected and path AIS status. The SPECTRA-622 does not support inband error reporting of enhanced RDI codes. To enable inband reporting of non-enhanced RDI codes, the SPECTRA-622 must be configured to generate path AIS on the drop bus for all events which can cause RDI. The local transmit section pass the path REI and path RDI bits on the ADD bus to the transmit stream unmodified. When RXSEL[1:0] is set to ‘b11, the path status byte in the transmit stream is not associate with any receive stream. No path REI nor path RDI will be reported.

Table 12 - RXSEL[1:0] codepoints for STS-1 and STS-Nc.

RXSEL[1:0]	Source
00	local SPECTRA-622
01	remote receive (TAP port)
10	Inband reporting
11	no reporting

DS3SLLBEN:

When set high, the DS3 system side line loopback enable bit (DS3SLLBEN) activates line loopback of the receive DS3 data stream processed by the corresponding RPPS. The receive DS3 data stream replaces the transmit DS3 data stream from the ADD interface. When DS3SLLBEN is set low, system side line loopback of the corresponding receive DS3 data stream is disabled, the DS3 data stream from the ADD interface is processed normally. The DS3 system side line loopback can only be enabled when the DS3 ADD Bus stream is selected via the DS3ADDSEL register bit in the SPECTRA-622 TPPS Path and DS3 configuration register. DS3SLLBEN has not effect when DS3ADDSEL is set low.

SLLBEN:

When set high, the system side line loopback enable bit (SLLBEN) activates line loopback of the receive STS-1 (STM-0/AU3) or equivalent stream processed by the corresponding RPPS. The receive stream replaces the transmit STS-1 (STM-0/AU3) or equivalent stream from the ADD bus. When SLLBEN is set low, system side line loopback of the corresponding receive stream is disabled, the data stream from the ADD bus is processed normally. The system side line loopback can only be enabled when the DS3 ADD Bus stream is disabled via the DS3ADDSEL register bit in the SPECTRA-622 TPPS Path and DS3 configuration register. SLLBEN has not effect when DS3ADDSEL is set high. When SLLBEN is low, TPIP is held in reset – TPIP registers cannot be accessed.

STM1-CONCAT:

The STM1-CONCAT bit is used to configure the TPPS to be processing TU2, TU11 or TU12 inside an STM-1(VC-4). When configured, TUAIS is properly asserted as defined by the ITUAIS in the TTAL. When set high, the TTAL fixed stuff columns are columns 1, 2 and 3. This supports TU2, TU11 and TU12 payloads in a VC-4. When set low, the TTAL fixed stuff columns are columns 30 and 59. When set low TUAIS can not be inserted properly. This bit can otherwise be set low.

MASTER:

When set high, the MASTER bit enables the TPPS to control and co-ordinate the processing of an STS-1 (STM-0/AU3) or an STS-Nc (STM-1/AU4 OR STM-4-Xc) transmit stream as the master. It also enables the TPPS to control and co-ordinate the distributed PRBS payload sequence generation and monitoring. When the MASTER bit is set low, the TPPS operates in a slave mode and its operation is co-ordinated by the associated master TPPS.

Register 1102H: SPECTRA-622 TPPS Path and DS3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	DISJ1V1	0
Bit 1	R/W	DS3ADDSEL	0
Bit 0	R/W	DS3TICLKB	0

This register allows the operational mode of the SPECTRA-622 TPPS Path and DS3 functions to be configured. These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

DS3TICLKB:

The DS3 TICLK invert (DS3TICLKB) bit controls the edge of DS3TICLK used to sample DS3TDAT when DS3ADDSEL bit is set high. When DS3TICLKB is set low, DS3TDAT are sampled on the rising edge of DS3TICLK. When DS3TICLKB is set high, DS3TDAT is sampled on the falling edge of DS3TICLK.

DS3ADDSEL:

The DS3 ADD bus stream select (DS3ADDSEL) bit controls the selection between the Telecom ADD bus stream or the DS3 ADD interface stream for transmission in the corresponding STS-1 (STM-0/AU3) or equivalent stream. When DS3ADDSEL is set low, the Telecom ADD bus stream is selected for transmission, the DS3MA is held in reset and non-functional. When DS3ADDSEL is set high, the DS3 ADD bus stream is selected for transmission. When set high the TPIP, APGM and TTAL blocks are held in reset and non-functional. A mix of Telecom bus and DS3 interface is not supported in bypass mode; all slices need to be programmed the same.

DISJ1V1:

When set high, the DISJ1V1 bit configures the SPECTRA-622 to only expect C1 byte indications on the AC1J1V1 input. When only C1 byte indications are provided, the SPECTRA-622 will interpret the pointer of the ADD bus to identify the J1 and V1 byte positions. When set low, the SPECTRA-622 expects the AC1J1V1 input to indicate C1, J1 and V1. This bit must be programmed in all the slaves to the same value as the master slice.

DISJ1V1 is only valid for Telecombus operation. See Table 8 System Side ADD Bus Configuration for programming of this bit.

In bypass mode, all the twelve slices must have the same DISJ1V1 setting.

Register 1106H: SPECTRA-622 TPPS Path Transmit Control

Bit	Type	Function	Default
Bit 7	R/W	ADDUEV	0
Bit 6	R/W	ADDUE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TDIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TPTBEN	0

This register controls the insertion of path overhead and unequipped payload pattern (FFH, 00H) in the transmit stream.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

TPTBEN:

The TPTBEN bit controls whether the path trace message stored in the TPTB (in SPTB) block is inserted in the transmit stream. When TPTBEN is set high, the message in the corresponding transmit path trace buffer (TPTB) is inserted in the transmit stream. When TPTBEN is set low, the path trace message is supplied by the TPOP block or via the corresponding TPOH input. The TPTBEN bit must be set low and the serial TPOH stream must be disable to prevent path trace insertion at intermediate tandem connection nodes. NOTE: This register bit should normally be set low when the TPPS is configured as a slave.

TDIS:

The TDIS bit controls the insertion of path overhead bytes in the transmit stream. When TDIS is set high, the path overhead bytes of the corresponding transmit stream is sourced from the ADD bus. Serial path overhead insertion and modification via the TPOH input is still available. Modification applies to the B3 and H4 byte. Setting TPOHEN high during the B3 or H4 byte field modifies the transmitted byte in an unpredictable fashion. All other POH bytes may be inserted via the TPOH input as controlled by the TPOHEN input normally. When TDIS is set low, path overhead is processed normally. The TDIS bit must be set high and the TPOHEN input set low to disable path

overhead insertion at intermediate tandem connection and at line (multiplexed section) terminating nodes.

ADDUE:

When set high, the ADDUE bit configures the corresponding transmit stream from the ADD bus as unequipped. Payload bytes are overwritten with all ones or all zeros as controlled using the ADDUEV bit. When ADDUE is set low, the transmit stream is equipped and carrying valid data.

ADDUEV:

When set high, the ADDUEV bit selects the all ones pattern as the overwrite pattern when payload overwrite is enabled using the ADDUE bit. When set low, the ADDUEV bit selects the all zeros pattern as the overwrite pattern when payload overwrite is enabled using the ADDUE bit.

Register 1108H: SPECTRA-622 TPPS DS3 Activity Monitor

Bit	Type	Function	Default
Bit 7	R	DS3TDATA	X
Bit 6	R	DS3TICLKA	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides activity monitoring on SPECTRA-622 system ADD side DS3 clock and data inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

DS3TICLKA:

The DS3TICLK active (DS3TICLKA) bit monitors for low to high transitions on the DS3TICLK input for the TPPS. DS3TICLKA is set high on a rising edge of the DS3TICLKA input, and is set low when this register is read.

DS3TDATA:

The DS3TDAT active (DS3TDATA) bit monitors for low to high transitions on the sampled DS3TDAT input for the TPPS. The DS3TDAT input is sampled by the corresponding DS3TICLK before being monitored for transitions. DS3TDATA is set high on a rising edge of the sampled DS3TDAT input, and is set low when this register is read.

Register 1110H: SPECTRA-622 TPPS Path AIS Control

Bit	Type	Function	Default
Bit 7	R/W	LOMTUAIS	0
Bit 6	R/W	TPAIS_EN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPAIS	0
Bit 2	R/W	PAISPAIS	0
Bit 1	R/W	LOPCONPAIS	0
Bit 0	R/W	PAISCONPAIS	0

This register controls the auto assertion of transmit path/TU AIS. These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enable path AIS insertion on the transmit stream when path AIS concatenation event is detected. When this bit is set low, the corresponding event has no effect on the transmit stream.
NOTE: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enable path AIS insertion on the transmit stream when loss of concatenated pointer (LOPCON) event is detected. When this bit is set low, the LOPCON event has no effect on the transmit stream.
NOTE: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

PAISPAIS:

When set high, the PAISPAIS bit enables path AIS insertion on the transmit stream when path AIS is detected on the ADD bus. When PAISPAIS is set low, path AIS events have no effect on the transmit stream.

TPAIS_EN:

When set high, the TPAIS_EN bit enables path AIS insertion into the transmit stream via the corresponding time-slot of the TPAIS input signal. When TPAIS_EN is set low, the TPAIS input signal have no effect on the transmit stream.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the transmit stream when loss of pointer (LOP) events are detected on the ADD bus. When LOPPAIS is set low, loss of pointer events have no effect on the transmit stream.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the transmit stream when loss of multiframe (LOM) events are detected on the ADD bus. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events have no effect on the transmit stream. LOMTUAIS must be set low when transmitting VT3 (TU3) payloads because the loss of multiframe condition does not exist.

Register 1128H: SPECTRA-622 TPPS Path/DS3 Interrupt Status

Bit	Type	Function	Default
Bit 7	R	TPAIS	X
Bit 6	R	Unused	X
Bit 5	R	TTALI	X
Bit 4	R	TPIPI	X
Bit 3	R	D3MAI	X
Bit 2	R	Unused	X
Bit 1	R	APGMI	X
Bit 0	X	Unused	X

This register, together with the SPECTRA-622 Section/Line Interrupt Status register, allows the source of an active interrupt for the transmit side to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

APGMI:

The APGMI bits are high when an interrupt request is active from the APGM block.

D3MAI:

The D3MAI bit is high when an interrupt request is active from the D3MA block.

TPIPI:

The TPIPI bit is high when an interrupt request is active from the TPIP block.

TTALI:

The TTALI bits is high when an interrupt request is active from the TTAL block.

TPAIS

The transmit stream alarm indication signal (TPAIS) bit is set high when path AIS is inserted in the transmit stream being processed by the TPPS. Transmit Path AIS assertion is controlled using the TTAL Control register or the TPOP Control register or the SPECTRA-622 TPPS Path AIS Control register with the ADD bus pointer interpretation enabled. Note, TPAIS is not an interrupt bit.

These register bits are not cleared on read.

Register 112CH: SPECTRA-622 TPPS Auxiliary Path Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOPCONE	0
Bit 6	R/W	PAISCONE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PAISE	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	LOME	0
Bit 1	R/W	Unused	0
Bit 0	R/W	Unused	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the SPECTRA-622 TPPS Auxiliary Path Interrupt Status register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-622 TPPS Auxiliary Path Interrupt Status register.

These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

LOME:

The loss of multiframe (LOM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOM interrupt status.

LOPE:

The loss of pointer (LOP) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOP interrupt status.

PAISE:

The path alarm indication signal (PAIS) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAIS interrupt status.

PAISCONE:

The path alarm indication signal concatenation (PAISCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAISCON interrupt status.

NOTE: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONE:

The loss of pointer concatenation (LOPCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOPCON interrupt status. NOTE: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

Register 1130H: SPECTRA-622 TPPS Auxiliary Path Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	LOPCONI	X
Bit 6	R/W	PAISCONI	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	PAISI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

This register replicates the path interrupts that can be found in the TPIP register. However, unlike the TPIP interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status.

LOPI:

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PAISI:

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PAISCONI:

The path AIS concatenation interrupt (PAISCONI) bit is set high when there is a change of the path AIS concatenation state. This auxiliary interrupt status corresponds to the AU3PAISCONI status in the TPIP Alarm Interrupt Status register.

LOPCONI:

The loss of pointer concatenation interrupt (LOPCONI) bit is set high when there is a change of the pointer concatenation state. This auxiliary interrupt status corresponds to the AU3LOPCONI status in the TPIP Alarm Interrupt Status register.

Register 1150H: TPOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PERDIEN	0
Bit 5	R/W	PERDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	EXCFS	0
Bit 2	R/W	DH4	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

The register controls the operation of the transport overhead processor for downstream diagnostics.

PAIS:

The PAIS bit controls the insertion of path alarm indication signal in the transmit stream. When a logic one is written to this bit, the synchronous payload envelope and the pointer bytes (H1 – H3) are set to all-ones. When a logic zero is written to this bit, the SPE and pointer bytes are processed normally. Upon de-activation of path AIS, a new data flag accompanies the first valid pointer.

DB3:

The diagnose BIP-8 enable bit (DB3) controls the inversion of the path BIP-8 byte (B3) in the transmit stream. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. This bit overrides the state of the B3 error insertion mask controlled by the corresponding TPOHEN primary input.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the transmit stream. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

EXCFS:

The fixed stuff column BIP-8 exclusion bit (EXCFS) controls the inclusion of bytes in the fixed stuff columns of the STS-1 (STM-0/AU3) payload carrying tributaries in path BIP-8 calculations. When EXCFS is set high, the value of bytes in the fixed stuff columns do not affect the path BIP-8 byte (B3). When EXCFS is set low, data in the fixed stuff bytes are included in path BIP-8 calculations. This bit must be set low when the TPPS containing the TPOP is processing an STS-Nc (STM-1/AU4 or STM-4-Xc) stream.

PERSIST:

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

PERDISRC:

The path enhanced remote defect indication source (PERDISRC) bit controls the source of the path enhanced RDI code. When PERDISRC is set high, the path enhanced RDI code is sourced from internal receive side alarms as controlled by the SPECTRA-622 RPPS Path REI/RDI Control (#1, #2) and SPECTRA-622 RPPS Path Enhanced RDI Control (#1, #2) registers. When PERDISRC is set low, the path enhanced RDI code is sourced from the TPOP Path Status register.

PERDIEN:

The path enhanced remote defect indication enable (PERDIEN) bit controls path RDI insertion. When PERDIEN is set high, path enhanced RDI assertion (bits 5,6,7 of the G1 byte) is enabled while normal path RDI (bit 5 of the G1 byte) and auxiliary path RDI (bit 6 of the G1 byte) are disabled. When PERDIEN is set low, path enhanced RDI assertion is disabled while normal path RDI and auxiliary path RDI are enabled.

Register 1151H: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	NDF	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls the pointer generation in the transmit stream.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

NDF:

The NDF insert bit (NDF) controls the insertion of new data flags in the payload pointer. When a logic one is written to this bit, the pattern contained in the NDF[3:0] bits in the TPOP Payload Pointer MSB register is inserted continuously in the payload pointer of the transmit stream. When a logic zero is written to this bit, the normal pattern (‘b0110) is inserted in the payload pointer.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated. If FTPTR is set to logic 1, the APTR[9:0] bits of the TPOP Payload Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. When FTPTR is set and immediately reset at least one Arbitrary Pointer substitution is guaranteed to be sent . If FTPTR is a logic 0, a valid pointer is inserted.

Register 1153H: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

Register 1154H: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:0]:

The CPTR[9:0] bits reflect the value of the active offset on the transmit stream as indicated by pulses on the AC1J1V1 signal. It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 1155H: TPOP Payload Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

Register 1156H: TPOP Payload Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

APTR[9:0]:

The APTR[9:0] bits are used to set an arbitrary active offset value in the transmit stream. The arbitrary pointer value is transferred by writing a logic one to the FTPTR bit in the TPOP Pointer Control Register. A legal value (i.e. $0 \leq$ pointer value ≤ 782) results in a new pointer in the transmit stream. A value of greater than 782 has no effect.

S1-S0:

The payload pointer size bits (S[1:0]) are inserted in the S[1:0] bit positions in the payload pointer in the transmit stream.

NDF[3:0]:

The new data flag bits (NDF[3:0]) are inserted in the NDF bit positions when the TPOP makes a discontinuous change in active offset or when the NDF bit in the TPOP Pointer Control register is set to logic one.

Register 1157H: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register contains the value to be inserted in the path trace byte (J1) of the transmit stream when the Transmit Path Trace Buffer block is disabled (TPTBEN set low).

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream when the associated SPTB block is disabled and corresponding TPOHEN input is low during the path trace bit positions in the path overhead input stream, TPOH.

Register 1158H: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register contains the value to be inserted in the path signal label byte (C2) of the transmit stream.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when the corresponding TPOHEN input is low during the path signal label bit positions in the path overhead input stream, TPOH. Upon reset, the register value defaults to 01H, which represents “Equipped – Non Specific Payload.”

Register 1159H: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	PREI[3]	0
Bit 6	R/W	PREI[2]	0
Bit 5	R/W	PREI[1]	0
Bit 4	R/W	PREI[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	PERDI6	0
Bit 1	R/W	PERDI7	0
Bit 0	R/W	G1[0]	0

This register reflects the value inserted in the path status byte (G1) of the transmit stream.

G1[0]:

The G1[0] bit is inserted in the unused bit positions in the path status byte the corresponding TPOHEN input is low during the unused bit positions in the corresponding path overhead input stream, TPOH.

PERDI6, PERDI7:

The PERDI6 and PERDI7 bits control the insertion of the STS path receive defect indication alarm (PRDI6 and PRDI7, respectively) when PERDIEN is logic one, and are inserted in the unused bit positions G1[2:1] in the path status byte when PERDIEN is logic zero, or when the primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH. The function is described in the table below.

Table 13 -Transmit RDI control

TPOHEN	PERDIEN	IBER	PERDISRC	Tx G1 bit 5	tx G1 bit 6	tx G1 bit 7
0	0	0	0	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	0	0	1	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	0	1	0	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
0	0	1	1	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
0	1	0	0	Reg[3]	Reg[2]	Reg[1]
0	1	0	1	PRDI5	PRDI6	PRDI7
0	1	1	0	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
0	1	1	1	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
1	0	0	0	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	0	0	1	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]

1	0	1	0	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	0	1	1	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	1	0	0	Reg[3]	Reg[2]	Reg[1]
1	1	0	1	PRDI5	PRDI6	PRDI7
1	1	1	0	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
1	1	1	1	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]

Table 31 Notes:

1. IBER = 1 when inband reporting is enabled. Inband error reporting is enabled when RXSEL[1:0] = ”10” in the SPECTRA-622 TPPS Configuration register (bits 7:6).
2. SPE_G1[7:5] = bits 7 through 5 of the G1 byte on the ADD bus
3. PRDI7, PRDI6, PRDI5 = bits 7 through 5 of the G1 byte from the associated RPOP or the transmit alarm port of the SPECTRA-622
4. Reg[3:1] = PRDI, PERDI6, PERDI7 register bit values, respectively
5. TPOH_G1[7:5] = the TPOH port values during the time slots reserved for bits 7 through 5 of the G1 byte

PRDI:

The PRDI bit controls the insertion of the STS path receive defect indication alarm. The function is described in the table above. This bit has no effect when the primary input TPOHEN is high during the path PRDI alarm bit position in the path overhead input stream, TPOH, in which case the value to taken from TPOH.

PREI[3:0]:

The path remote error indication count (PREI[3:0]) is inserted in the path REI bit positions in the path status byte when the corresponding TPOHEN input is low during the path status REI bit positions in the corresponding path overhead input stream, TPOH. The value contained in PREI[3:0] is cleared after being inserted in the path status byte. Any non-zero PREI[3:0] value overwrites the value that would normally have been inserted based on the number of PREIs accumulated from the BIP-8 errors detected by the companion RPOP in the SPECTRA-622 during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 115AH: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register contains the value to be inserted in the path user channel byte (F2) of the transmit stream.

F2[7:0]:

The F2[7:0] bits are inserted in the F2 byte position in the transmit stream when the corresponding TPOHEN input is low during the path user channel bit positions in the corresponding path overhead input stream, TPOH.

Register 115BH: TPOP Path Growth #1

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register contains the value to be inserted in the path growth byte #1 (Z3) of the transmit stream.

Z3[7:0]:

The Z3[7:0] bits are inserted in the Z3 byte position in the transmit stream when the corresponding TPOHEN input is low during the path growth #1 bit positions in the corresponding path overhead input stream, TPOH.

Register 115CH: TPOP Path Growth #2

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register contains the value to be inserted in the path growth byte #2 (Z4) of the transmit stream.

Z4[7:0]:

The Z4[7:0] bits are inserted in the Z4 byte position in the transmit stream when the corresponding TPOHEN input is low during the path growth #2 bit positions in the corresponding path overhead input stream, TPOH.

Register 115DH: TPOP Tandem Connection Maintenance

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register contains the value to be inserted in the tandem connection maintenance byte (Z5) of the transmit stream.

Z50-Z57:

The Z5[7:0] bits are inserted in the Z5 byte position in the transmit stream when the corresponding TPOHEN input is low during the tandem connection maintenance byte positions in the corresponding path overhead input stream, TPOH.

Register 1180H: TTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	Reserved_High	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	PJEE	0
Bit 0	R/W	Reserved	0

This register allows the operation of the Transmit Telecombus Aligner to be configured.

Reserved_High:

The Reserved_High bits must be set high for proper operation of the SPECTRA-622.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PJEE:

The pointer justification event interrupt enable bit (PJEE) controls the activation of the interrupt output when a pointer justification is inserted in the transmit stream. When PJEE is set high, insertion of pointer justification events in the transmit stream will activate the interrupt (INTB) output. When PJEE is set low, insertion of pointer justification events in the transmit stream will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events will affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a

logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the ADD bus is placed on the transmit stream unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the TPPS containing the TTAL is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the TTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the ADD bus is placed in the transmit stream unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence ‘Hfc, ‘Hfd, ‘Hfe and ‘Hff. The phase of the four frames in the multiframe is synchronized by the V1 pulse in AC1J1V1 input.

Register 1181H: TTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	Reserved	0

This register allows the control of the transmit stream and sensing of interrupt status.

The interrupt bits (and the interrupt) are cleared when this register is read.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622.

NPJI:

The transmit stream negative pointer justification interrupt status bit (NPJI) is set high when the TTAL inserts a negative pointer justification event in the transmit stream.

PPJI:

The transmit stream positive pointer justification interrupt status bit (PPJI) is set high when the TTAL inserts a positive pointer justification event in the transmit stream.

ESEI:

The ADD bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in TTAL underflows or overflows. This will cause the TTAL to reset itself. It can thus lose the J1, and go out of AIS for a short period of time if it was in AIS state.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds i.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 14 - Transmit ESD[1:0] codepoints.

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definition:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing negative justification at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the TTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the TTAL will start generates outgoing positive justification at the rate of in 1 every 4 frames).

Register 1182H: TTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register controls the tributary format on the transmit stream.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-622.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the TRANSMIT stream. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit stream when a FIFO underflow or overflow has been detected in the elastic store . When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the transmit stream for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS in the transmit stream when transmitting VT11 (TU11), VT12 (TU12) and VT2 (TU2) payloads. When ITUAIS is set high, columns in the transmit stream carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected.

Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit does not work for VT3 (TU3) tributary payloads and the ITUAIS bit must be set low. The STM1-CONCAT register bit must be set for TU2, TU11 and TU12 payloads in a VC-4.

Register 1190H: TPIP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	AU3LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	AU3PAISCONV	X
Bit 3	R	PAISV	X
Bit 2	R	Reserved	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding TPIP if the EXTD bit is set low in the TPIP Pointer MSB register.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output. Must be set only in master slices.

NEWPTRI:

The NEWPTRI bit is set to logic 1 when a new_point indication is received. This bit (and the interrupt) are cleared when this register is read. Only valid in master slices

PAISV:

The path AIS status bit (PAIS) indicates reception of path AIS alarm in the receive stream. Only valid in master slices

AU3PAISCONV:

The AU3 concatenation path AIS status bit (AU3PAISCONV) indicates reception of path AIS alarm in the concatenation indication in the transmit STS-1 (STM-0/AU3) or equivalent stream. Only valid in slave slices.

LOPV:

The loss of pointer status bit (LOPV) indicates entry to the LOP_state in the TPIP pointer interpreter state machine. Only valid in master slices

AU3LOPCONV:

The AU3 concatenated loss of pointer status bit (AU3LOPCONV) indicates entry to LOPCON_state for the transmit STS-1 (STM-0/AU3) or equivalent stream in the TPIP pointer interpreter. Only valid in slave slices.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-622.

Register 1190H: TPIP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register provides configuration of the corresponding TPIP if the EXTD bit is set high in the TPIP Pointer MSB register.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

IINVCNT:

When a 1 is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to 0, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected. Must only be used in master slices.

Register 1191H: TPIP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	AU3LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	AU3PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the TPIP Pointer MSB register.

These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected. Only valid in master slices.

PAISI:

The PAISI interrupt status bit is set high on assertion and removal of the corresponding path alarm indication signal status. Only valid in master slices.

AU3PAISCONI:

The AU3PAISCONI interrupt status bit is set high on assertion and removal of the corresponding AU3 path alarm indication signal concatenation status. Only valid in slave slices.

LOPI:

The LOPI interrupt status bit is set high on assertion and removal of the corresponding loss of pointer status. Only valid in master slices.

AU3LOPCONI:

The AU3LOPCONI interrupt status bit is set high on assertion and removal of the corresponding AU3 loss of pointer concatenation status. Only valid in slave slices.

Register 1192H: TPIP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	Reserved	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

These bits (and the interrupt) are cleared when this register is read.

Reserved:

The Reserved bits are interrupt status bits and must be ignored when this register is read.

NDFI:

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream. Only valid in master slices.

PSEI, NSEI:

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the TPIP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream. Only valid in master slices.

INVNDFI:

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream. Only valid in master slices.

DISCOPAI:

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the TPIP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication). Only valid in master slices.

CONCATI:

The concatenation indication error interrupt status bit (CONCATI) is set high when the SPECTRA-622 is operating in concatenation mode and an error is detected in the concatenation indicators. Only valid in slave slices.

ILLJREQI:

The illegal justification request interrupt status bit (ILLJREQI) is set high when the TPIP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable). Only valid in master slices.

Register 1193H: TPIP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	AU3LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	AU3PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the TPIP Pointer MSB register.

Reserved:

The Reserved bits must be set to 0 for proper operation of the SPECTRA-622

PREIE:

When a 1 is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output. Must only be set in master slices.

PAISE:

When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output. Must only be set in master slices.

AU3PAISCONE:

When a 1 is written to the AU3PAISCONE interrupt enable bit position, a change in the AU3 concatenation path AIS state will activate the interrupt (INTB) output. Must only be set in slave slices.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output. Must only be set in master slices.

AU3LOPCONE:

When a 1 is written to the AU3LOPCONE interrupt enable bit position, a change in the AU3 concatenation loss of pointer state will activate the interrupt (INTB) output. Must only be set in slave slices.

Register 1194H: TPIP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

Reserved

The Reserved bits must be set to 0 for proper operation of the SPECTRA-622

NDFE:

When a 1 is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output. Must only be set in master slices.

PSEE:

When a 1 is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output. Must only be set in master slices.

NSEE:

When a 1 is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output. Must only be set in master slices.

INVNDFE:

When a 1 is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output. Must only be set in master slices.DISCOPAE:

When a 1 is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output. Must only be set in master slices.

CONCATE:

When a 1 is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output. Must only be set in slave slices.

ILLJREQE:

When a 1 is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output. Must only be set in master slices.

Register 1195H: TPIP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the TPIP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register 1196H: TPIP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	Reserved1	0
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

CONCAT:

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don’t care in the size field, and all-ones in the pointer offset field).

Reserved1:

The Reserved1 bit is a status bit and must be ignored when this register is read.

EXTD:

The EXTD bit extends the TPIP registers to facilitate additional mapping. If this bit is set to logic 1 the register mapping, for the TPIP Status and Control register, the TPIP Alarm Interrupt Status register and the TPIP Alarm Interrupt Enable registers are extended.

NDFPOR:

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8Xndf_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Register 119CH: TPIP Tributary Multiframe Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	Reserved	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0	R	Reserved	X

This register reports the status of the multiframe framer and enables interrupts due to framer events.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

COMAE:

The change of multiframe alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA-622 detect a change in the multiframe phase. When LOME is set high, an interrupt is generated upon change of multiframe alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI:

The change of multiframe alignment interrupt status bit (COMAI) is set high on changes in the multiframe alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

LOME:

The loss of multiframe interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multiframe indication (LOM). When LOME is set high, an interrupt is generated upon loss of multiframe. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV:

The loss of multiframe status bit (LOMV) reports the current state of the multiframe framer monitoring the receive stream. LOMV is set high when loss

of multiframe is declared and is set low when multiframe alignment has been acquired.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Register 11B0H: D3MA Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RBSO	0
Bit 0	R/W	DS3AISGEN	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

DS3AISGEN:

The active high DS3 Alarm Indication Signal enable bit (DS3AISGEN) configures the D3MA to generate a DS3 AIS signal. Any data on the STS-1 (STM-0/AU3) SPE is lost due to the assertion of DS3AISGEN. DS3AISGEN bit is logically ORed with the corresponding time-slot of the TPAIS input.

RBSO:

When RBSO is high, the R bits of the DS3 mapping or the STS-1 (STM-0/AU3) mapping are set to ‘1’s. If RBSO bit is Low, R bits are set to ‘0’s. This bit is valid for both Serial DS3 and Serial Data Mode operation.

Register 11B1H: D3MA Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

UFLI

When set High, this bit indicates that an underflow condition has occurred in the D3MA elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When set High, this bit indicates that an overflow condition has occurred in the D3MA elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 11B2H: D3MA Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLE	0
Bit 0	R/W	UFLE	0

UFLE:

When set High, this bit enables generation of an interrupt if an elastic store underflow condition occurs (UFLI='1').

OFLE:

When set High, this bit enables generation of an interrupt if an elastic store overflow condition occurs (OFLI='1').

Register 11D0H: APGM Generator Control #1

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	GEN_INV_PRBS	0
Bit 5	R/W	GEN_AUTO	0
Bit 4	R/W	GEN_FERR	0
Bit 3	R/W	GEN_SIGE	0
Bit 2	R/W	GEN_FSENB	0
Bit 1	R/W	GEN_REGEN	0
Bit 0	R/W	GEN_EN	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

GEN_EN:

The Generator Enable (GEN_EN) bit enables the insertion of a pseudo random bit sequence (PRBS) into the Transmit payload. When GEN_EN is set high, the PRBS bytes will overwrite the processed payload data. When GEN_EN is set low, the incoming payload is unaltered. This bit has not effect in Autonomous Input Mode. This mode can not be used in the STS-12c configuration when in ATMODE (19 MHz clock).

GEN_REGEN:

The Generator Regenerate (GEN_REGEN) bit can be used to re-initialize the generator LFSR and begin regenerating the pseudo random bit sequence (PRBS) from the known reset state. The LFSR reset state is dependent on the set sequence number. Setting this bit in a master generator will automatically force all slaves to reset at the same time. This bit will clear itself when the operation is complete. Upon a frame realignment on the ADD BUS #1 (AC1J1V1_AFP[1]) the Generators must be regenerated.

GEN_FSENB:

The Generator Fixed Stuff Enable (GEN_FSENB) bit determines whether the pseudo random bit sequence (PRBS) is inserted into the (STS-1/STM0) fixed stuff bytes of the processed payload. When set to logic one, the PRBS is not inserted into the fixed stuff bytes and the bytes are outputted unaltered. When set to logic zero, the PRBS is inserted into the fixed stuff bytes. The Fixed stuff columns are columns 30 and 59 of the STS-1 payload.

GEN_FSEN should be disabled when using the generator in master/slave configuration to support de-multiplexed concatenated payloads..

GEN_SIGE:

The Generator Signature Interrupt Enable (GEN_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When GEN_SIGE is set high, a change in the signature verification state (GEN_SIGV) will trigger an interrupt. When GEN_SIGE is set low, no interrupt will be asserted.

GEN_FERR:

The Generator Force Error (GEN_FERR) bit is used to force bit errors in the inserted pseudo random bit sequence (PRBS). When logic one is written to this bit, the MSB of the PRBS byte will be inverted, inducing a single bit error. The register bit will clear itself when the operation is complete.
A second forced error must not be attempted for at least three GCLK clock cycles after this bit has been read back to ‘0’.

GEN_AUTO:

The Generator Autonomous Mode (GEN_AUTO) bit places the Generator in the Autonomous Input Mode. In this mode the payload frame is forced to an active offset of zero. The generated frame will have all zeros TOH and POH bytes. The H1, H2 pointer bytes are set to indicate an active SPE/VC offset of zero and the payload will be filled with a PRBS. When a logic zero is written to this bit, the active offset is determined by the received stream. The autonomous mode can not be used in the STS-12c configuration when in ATMODE (19 MHz clock).
When all 12 slices are in autonomous mode, and only then, the ATSI bits in the ADD Bus Configuration register (1030H) can be used for situations where the ADD bus does not provide a valid frame pulse.

GEN_INV_PRBS:

The Generator Invert PRBS (GEN_INV_PRBS) bit is used to invert the calculated PRBS byte before insertion into the payload. Setting this bit to logic 1 enables the logic inversion of all PRBS bits before insertion into the payload. Setting this bit to logic 0 does not invert the generated PRBS.

Register 11D1H: APGM Generator Control #2

Bit	Type	Function	Default
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	Unused	0
Bit 3	R/W	Unused	0
Bit 2	R/W	Unused	0
Bit 1	R/W	GEN_H4_EN	0
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

GEN_H4_EN:

The Generator multi-frame indicator H4 Enable (GEN_H4_EN) bit enables the insertion of the H4 indicator into the H4 byte position of the processed payload. Setting to logic 1 this bit enables the insertion of a valid H4 byte. The inserted value of H4 is derived from the received stream H4 byte. This feature is duplicated in the TTAL block. By default TTAL should be used to insert H4. This bit should only be used when the TTAL FIFO is bypassed.

Register 11D2H: APGM Generator Concatenate Control

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	GEN_SEQ[3]	1
Bit 4	R/W	GEN_SEQ[2]	1
Bit 3	R/W	GEN_SEQ[1]	1
Bit 2	R/W	GEN_SEQ[0]	1
Bit 1	R/W	GEN_GMODE[1]	0
Bit 0	R/W	GEN_GMODE[0]	0

GEN_GMODE[1:0]:

The GEN_GMODE[1:0] bits control the operational mode of the pseudo random sequence generator as summarized in the table below. When GEN_GMODE[1:0] is set to 'b00, the generator will generate the complete sequence for an STS-1 (STM-0/AU3) stream. When GEN_GMODE[1:0] is set to 'b01, the generator will generate one third or 1 in 3 bytes of the complete sequence for an STS-1 (STM-0/AU3) equivalent in an STS-3c (STM-1/AU4) stream. When GEN_GMODE[1:0] is set to 'b10, the generator will generate one twelfth or 1 in 12 bytes of the complete sequence for an STS-1 (STM-0/AU3) equivalent in an STS-12c (STM-4-4c) stream.

GEN_GMODE [1:0]	Generator Gap Mode Description
00	**1in1 Gap Mode**. Generator inserts the complete PRBS.
01	**1in3 Gap Mode**. Generator generates 1 of 3 (1in3) PRBS bytes. The generator will also generate 1in2 bytes to skip over POH columns.
10	**1in12 Gap Mode**. The generator generates 1 of 12 (1in12) PRBS bytes. The generator will also generate 1in8 bytes to skip over POH or fixed stuff columns.
11	Reserved

GEN_SEQ[3:0]

The Generator Sequence (GEN_SEQ[3:0]) sets the reset state of the LFSR and places the generator in the master or slave mode. The sequence number identifies the multiplexing order of the outgoing data into the concatenating stream. The sequence number also affects the signature bit calculation.

GEN_SEQ [3:0]	Mode	Signature bit	Reset Value
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.	All Ones.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.	Master+8 states
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.	Master+16 states
0011	Slave3	72nd PRBS bit from current state. MSB of 9th PRBS byte.	Master+24 states
0100	Slave4	64th PRBS bit from current state. MSB of 8th PRBS byte.	Master+32 states
0101	Slave5	56th PRBS bit from current state. MSB of 7th PRBS byte.	Master+40 states
0110	Slave6	48th PRBS bit from current state. MSB of 6th PRBS byte.	Master+48 states
0111	Slave7	40th PRBS bit from current state. MSB of 5th PRBS byte.	Master+54 states
1000	Slave8	32nd PRBS bit from current state. MSB of 4th PRBS byte.	Master+64 states
1001	Slave9	24th PRBS bit from current state. MSB of 3rd PRBS byte.	Master+72 states
1010	Slave10	16th PRBS bit from current state. MSB of 2nd PRBS byte.	Master+80 states
1011	Slave11	8th PRBS bit from current state. MSB of next PRBS byte.	Master+88 states
1100-1110		Reserved	
1111		Reserved	

Register 11D3H: APGM Generator Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	GEN_SIGI	X
Bit 0	R	GEN_SIGV	X

GEN_SIGV:

The Generator Signature Status (GEN_SIGV) bit indicates if the partial pseudo random sequence (PRBS) begin generated is correctly aligned with the partial PRBS begin generated in the master generator. When GEN_SIGV is low, the signature verification is a match, and the partial PRBS is aligned with that of the master. When GEN_SIGV is high, the signature verification is a mismatch, and the partial PRBS is not aligned with that of the master.
If non-alignment persists, a forced re-start of the sequence generation by all generators processing the concatenated stream should be initiated using the GEN_REGEN register bit in the master generator. This bit is only valid in slave generators and when out of alignment may toggle high and low. Persistent reads at low or reading the interrupt at low assures that the signature is correct.
.

GEN_SIGI:

The Generator Signature Interrupt Status (GEN_SIGI) bit indicates a change in the signature verification state (GEN_SIGV) by a slave generator. When GEN_SIGI is set high, the slave generator has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit will continuously be set when in the out of alignment state since the status GEN_SIGV will toggle. This bit is only valid in slave generators.

Register 11D8H: APGM Monitor Control #1

Bit	Type	Function	Default
Bit 7	R/W	MON_AUTORESYNC	1
Bit 6	R/W	MON_INV_PRBS	0
Bit 5	R/W	MON_SYNCE	X
Bit 4	R/W	MON_ERRE	0
Bit 3	R/W	MON_FSENB	0
Bit 2	R/W	MON_SIGE	0
Bit 1	R/W	MONM_RESYNC	0
Bit 0	R/W	MON_EN	0

MON_EN:

The Monitor Enable (MON_EN) bit enables the monitoring of a pseudo random bit sequence (PRBS) in the processed payload. When MON_EN is set high, the incoming payload is extracted and the data monitored for the PRBS. When MON_EN is set low, no monitoring on the data is done.

MON_RESYNC:

The Monitor Resynchronize (MON_RESYNC) bit allows a forced resynchronization of the monitor to the incoming pseudo random bit sequence (PRBS). When set to logic one, the monitor's will go out of synchronization and begin re-synchronizing the to the incoming PRBS payload. Setting this bit in a master monitor will automatically force all slaves to re-synchronize at the same time. This register bit will clear itself when the re-synchronizing has been triggered.

MON_FSENB:

The Monitor Fixed Stuff Enable (MON_FSENB) bit determines whether a PRBS is monitored for in the fixed stuff columns (columns 30 and 59) of the processed payload. When logic one is written to this bit, the PRBS is not monitored for in the fixed stuff columns. When a logic zero is written to this bit, the PRBS is monitored for in the fixed stuff columns. MON_FSENB should be disabled when using the monitor in master/slave configuration to support de-multiplexed concatenated payloads.

MON_SIGE:

The Monitor Signature Interrupt Enable (MON_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When MON_SIGE is set high, a change in the signature verification state

(MON_SIGV) will trigger an interrupt. When MON_SIGE is set low, no interrupt is reported. Note: This bit is ignored in a master APGM.

MON_ERRE:

The Monitor Byte Error Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when a PRBS byte error has been detected in the incoming payload. When MON_ERRE is set high, a detected PRBS error in the incoming data will trigger an interrupt. When MON_ERRE is set low, no interrupt is generated.

MON_SYNCE:

The Monitor Synchronize Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when change in the synchronization state of the monitor occurs. When MON_SYNCE is set high, a change in the synchronization state (MON_SYNCV) will trigger an interrupt. When MON_SYNCE is set low, no interrupt is generated.

MON_INV_PRBS:

The Monitor Invert PRBS (MON_INV_PRBS) bit is used to invert the received payload data before monitoring the data for a pseudo random bit sequence (PRBS). When set to logic 1, the incoming payload PRBS bits are inverted before being verified against the monitor expected PRBS. When set to logic 0, the incoming payload PRBS is not inverted and verified as is.

MON_AUTORESYNC:

The Monitor Automatic Resynchronization (MON_AUTORESYNC) bit enables the automatic resynchronization of the monitor after detecting 16 consecutive PRBS byte errors. Setting this bit to logic 1, enables the monitor to automatically fall out of synchronization after 16 consecutive errors. Once out of synchronization, the monitor will attempt to resynchronize to the incoming PRBS and verify the synchronization with 32 consecutive PRBS matches. Setting this bit to logic 0 disables the automatic resynchronization

Register 11D9H: APGM Monitor Control #2

Bit	Type	Function	Default
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	Unused	0
Bit 3	R/W	Unused	0
Bit 2	R/W	Unused	0
Bit 1	R/W	Unused	0
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

Register 11DAH: APGM Monitor Concatenate Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	MON_SEQ[3]	1
Bit 4	R/W	MON_SEQ[2]	1
Bit 3	R/W	MON_SEQ[1]	1
Bit 2	R/W	MON_SEQ[0]	1
Bit 1	R/W	MON_GMODE[1]	1
Bit 0	R/W	MON_GMODE[0]	1

MON_GMODE[1:0]:

The MON_GMODE[1:0] bits control the operational mode of the pseudo random sequence monitor as summarized in the table below. When MON_GMODE[1:0] is set to 'b00, the monitor expects the complete sequence for an STS-1 (STM-0/AU3) stream. When MON_GMODE[1:0] is set to 'b01, the monitor expects one third or 1 in 3 bytes of the complete sequence in an STS-1 (STM-0/AU3) equivalent of an STS-3c (STM-1/AU4) stream. When MON_GMODE[1:0] is set to 'b10, the monitor expects one twelfth or 1 in 12 bytes of the complete sequence in an STS-1 (STM-0/AU3) equivalent of an STS-12c (STM-4-4c) stream.

MON_GMODE [1:0]	Monitor Gap Mode Description
00	**1in1 Gap Mode**. Monitor monitors for a complete PRBS.
01	**1in3 Gap Mode**. Monitor will monitor for the presence of every 3rd PRBS byte. The Monitor will also monitor for every 2nd PRBS byte after the POH columns.
10	**1in12 Gap Mode**. Monitor will monitor for the presence of every 12th PRBS byte. The Monitor will also monitor for every 8th PRBS byte after the POH and fixed stuff columns.
11	Reserved

MON_SEQ[3:0]

The Monitor Sequence (MON_SEQ[3:0]) sets the Monitor in master or slave mode and is used to identify the multiplexed order of the monitored data in

the concatenated payload. The sequence order affects the signature bit calculation.

MON_SEQ [3:0]	Mode	Signature bit
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.
0011	Slave3	72nd PRBS bit from current state. MSB of 9th PRBS byte.
0100	Slave4	64th PRBS bit from current state. MSB of 8th PRBS byte.
0101	Slave5	56th PRBS bit from current state. MSB of 7th PRBS byte.
0110	Slave6	48th PRBS bit from current state. MSB of 6th PRBS byte.
0111	Slave7	40th PRBS bit from current state. MSB of 5th PRBS byte.
1000	Slave8	32nd PRBS bit from current state. MSB of 4th PRBS byte.
1001	Slave9	24th PRBS bit from current state. MSB of 3rd PRBS byte.
1010	Slave10	16th PRBS bit from current state. MSB of 2nd PRBS byte.
1011	Slave11	8th PRBS bit from current state. MSB of next PRBS byte.
1100-1110		Reserved
1111		Reserved

Register 11DBH: APGM Monitor Status

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	MON_ERRI	X
Bit 3	R	MON_SYNCI	X
Bit 2	R	MON_SYNCV	X
Bit 1	R	MONS_SIGI	X
Bit 0	R	MONS_SIGV	X

Reserved:

The Reserved bits reflect interrupt reads and must be ignored.

MON_SIGV:

The Monitor Signature Status (MON_SIGV) bit indicates if the partial pseudo random sequence (PRBS) being monitored for is correctly aligned with the partial PRBS being monitored for by the master generator. When MON_SIGV is low, the signature verification is a match, and the calculated partial PRBS is aligned with that of the master. When MON_SIGV is high, the signature verification is a mismatch, and the calculated partial PRBS is not aligned with that of the master. This bit does not identify if it is the master or the slave that is out of sync, it only says that they are not in sync one relative to the other. If non-alignment persists, a forced re-synchronization of all monitors processing the concatenated stream should be initiated using the MON_RESYNC register bit in the master generator. This bit is only valid in slave generators.

MON_SIGI:

The Monitor Signature Interrupt Status (MON_SIGI) bit indicates a change in the signature verification state (MON_SIGV) by a slave monitor. When MON_SIGI is set high, the Monitor has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit is only valid in slave monitor.

MON_SYNCV:

The Monitor Synchronize Status (MON_SYNCV) is set high when the monitor is out of synchronization. The monitor falls out of synchronization after detecting 16 consecutive mismatched PRBS bytes or being forced to re-

synchronize. A forced re-synchronize may be due to setting the MON_RESYNC register bit or a master generator. Once out of synchronization, the Synchronized State can only be achieved after re-synchronizing to the incoming PRBS and verifying the resynchronization with 32 consecutive non-erred PRBS bytes. This bit is set low when in the Synchronized State. This bit is local to each slice so it should be monitored in the master and all its slaves.

MON_SYNCI:

The Monitor Synchronize Interrupt Status (MON_SYNCI) bit indicates a change in the synchronization state (MON_SYNCV) of the monitor. When MON_SYNCI is set high, the monitor has transitioned from the Synchronized to Out of Synchronization State or vice versa. This bit is cleared when this register is read.

MON_ERRI:

The Monitor Byte Error Interrupt Status (MON_ERRI) bit indicates that an error has been detected in the received PRBS byte while the monitor was in the Synchronized State. MON_ERRI is set high, when one or more PRBS bit errors have been detected in the received PRBS data byte. This bit is cleared when this register is read.

Register 11DCH: APGM Monitor Error Count #1

Bit	Type	Function	Default
Bit 7	R	PRSE[7]	X
Bit 6	R	PRSE[6]	X
Bit 5	R	PRSE[5]	X
Bit 4	R	PRSE[4]	X
Bit 3	R	PRSE[3]	X
Bit 2	R	PRSE[2]	X
Bit 1	R	PRSE[1]	X
Bit 0	R	PRSE[0]	X

Register 11DDH: APGM Monitor Error Count #2

Bit	Type	Function	Default
Bit 7	R	PRSE[15]	X
Bit 6	R	PRSE[14]	X
Bit 5	R	PRSE[13]	X
Bit 4	R	PRSE[12]	X
Bit 3	R	PRSE[11]	X
Bit 2	R	PRSE[10]	X
Bit 1	R	PRSE[9]	X
Bit 0	R	PRSE[8]	X

PRSE[15:0]:

The PRSE[15:0] bits represent the number of PRBS byte errors detected since the last accumulation interval. Errors are only accumulated in the synchronized state and each PRBS data byte can have a maximum of 1 errors. The transfer of the error accumulation counter to these registers is triggered by a write to either of the GPGM Monitor Error Counters, or , to the Accumulation Trigger register (0000H). The contents of these registers will be valid only 4 clock cycles after the transfer is triggered. For concatenated payload, the master slice and each slave work independently from one another, thus the error count is the sum of all the slices.

13 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the SPECTRA-622. Test mode registers (as opposed to normal mode registers) are selected when A[13] is high.

Test mode registers may also be used for board or module level testing. When all of the constituent TSBs within the SPECTRA-622 are placed in test mode 0, device inputs may be observed, and device outputs may be controlled via the microprocessor interface (refer to the “Test Mode 0” section below for details).

In addition, the SPECTRA-622 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 15 -Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000H	Master Test Register
2001H	Master Test Slice Select
2000H-3FFFH	Reserved For Test

13.1 Master Test and Test Configuration Registers

Notes on Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Register Address 2000H: Master Test

Bit	Type	Function	Default
Bit 7	R/W	MOTOTST	0, by rstb low
Bit 6	R/W	Reserved	0, by csb high
Bit 5	R/W	PMCATST	0, by csb high and rstb low
Bit 4	R/W	PMCTST	0, by csb high
Bit 3	R/W	DBCTRL	0, by rstb low
Bit 2	R/W	IOTST	0, by rstb low
Bit 1	R/W	HIZDATA	0, by rstb low
Bit 0	R/W	HIZIO	0, by rstb low

This register is used to enable SPECTRA-622 test features. All bits, except PMCTST and PMCATST are reset to zero by a reset of the SPECTRA-622 using either the RSTB input or the Master Reset register. PMCTST is reset when CSB is logic 1. PMCATST is reset when both CSB is high and RSTB is low. PMCTST and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-622.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the SPECTRA-622. While the HIZIO bit is a logic one, all output pins of the SPECTRA-622 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the SPECTRA-622 for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST

are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the SPECTRA-622 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the SPECTRA-622 for PMC's manufacturing tests. When PMCTST is set to logic one, the SPECTRA-622 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the SPECTRA-622 for PMC's manufacturing tests.

MOTOTST:

The MOTOTST bit is used to test the Motorola interface. When the MOTOTST bit is logic one and the MBEB input is logic zero, the SCPI[0] and SCPI[1] inputs are used to replace the E and RWB inputs respectively. This is done because the fixed waveform shapes assigned to the RDB/E and WRB/RWB inputs can not be used to test the Motorola type microprocessor interface logic. This mode permits testing of the D.C. drive capability of the D[7:0] device pins.

Register Address 2001H: RX Analog Test Register

Bit	Type	Function	Default
Bit 7	W	RXATSTIN1	0, by csb high
Bit 6	W	RXATSTIN0	0, by csb high
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	W	RXC	0, by csb high
Bit 1	W	RXD	0, by csb high
Bit 0	W	REFCLK	0, by csb high

The Receive Analog Test Register supplies the analog test control signals for the PECL ABC cells in the receive side.

REFCLK:

When REFCLK ATSTDIS is low, the REFCLK PECL Receiver can be put into analog test mode by the PMCATST bit (of register 0x100). When REFCLK ATSTDIS is set high, PMCATST has no effect on the REFCLK PECL Receiver.

RXD:

When RXD ATSTDIS is low, the RXD PECL Receiver can be put into analog test mode by the PMCATST bit (of register 0x100). When RXD ATSTDIS is set high, PMCATST has no effect on the RXD PECL Receiver.

RXC:

When RXC ATSTDIS is low, the RXC PECL Receiver can be put into analog test mode by the PMCATST bit (of register 0x100). When RXC ATSTDIS is set high, PMCATST has no effect on the RXC PECL Receiver.

RX ATSTIN:

The Receive Analog Test In Bus (RX ATSTIN) provides test mode controls to the REFCLK, RXD, and RXC PECL cells.

Register Address 2002H: TX Analog Test Register

Bit	Type	Function	Default
Bit 7	W	TXATSTIN1	0, by csb high
Bit 6	W	TXATSTIN0	0, by csb high
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	W	TXD	0, by csb high

The Transmit Analog Test Register supplies the analog test control signals for the PECL ABC cells in the transmit side.

TXD:

When TXD ATSTDIS is low, the TXD PECL Transmitter can be put into analog test mode by the PMCATST bit (of register 0x100). When TXD ATSTDIS is set high, PMCATST has no effect on the TXD PECL Transmitter.

TX ATSTIN:

The Transmit Analog Test In Bus (TX ATSTIN) provides test mode controls to the TXD, TXC, and ETXC PECL cells.

Register Address 2003H: Master Test Slice Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SLICE_SEL[3]	0, by csb high
Bit 2	R/W	SLICE_SEL[2]	0, by csb high
Bit 1	R/W	SLICE_SEL[1]	0, by csb high
Bit 0	R/W	SLICE_SEL[0]	0, by csb high

SLICE_SEL[3:0]:

The slice select (SLICE_SEL[3:0) bits can be used to control the address of the microprocessor accesses to the device. The code-points of SLICE_SEL[3:0] are summarized in the table below. When SLICE_SEL[3:0] is set to 0H, the internally addressed register is directly controlled by the address bus A[13:0]. When SLICE_SEL[3:0] is other than 0H and the PMCTST or the IOTST bit in the SPECTRA-622 Master Test register is set high, the microprocessor address bits A[11:8] are forced to the values of the SLICE_SEL[3:0] respectively. The SLICE_SEL[3:0] bits can be used to directly select which RPPS or TPPS address space is accessed. The SLICE_SEL[3:0] bits are cleared by setting CSB to logic 1 and the register must be reset to disable the address bus controlling..

Table 16 - Master Test Slice Select, SLICE_SEL[3:0] code-points.

SLICE_SEL[3:0]	Address[13:0]	Internal Address
0	XXXXh	XXXXh
n	XXXXh	XnXXh

13.2 JTAG Test Port

The SPECTRA-622 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can

be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 17 -Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 18 -Identification Register

Length	32 bits
Version number	1H
Part Number	5313H
Manufacturer's identification code	0CDH
Device identification	153130CDH

Table 19 -Boundary Scan Register Length - 277 bits

Pin / Enable	Register Bit	Cell Type	Pin / Enable	Register Bit	Cell Type
hiz	277	IN_CELL	Dc1j1v1[2]	138	OUT_CELL
scpo_oeb	276	IN_CELL	Dd[8]	137	OUT_CELL
scpo[1]	275	OUT_CELL	Dd[9]	136	OUT_CELL
scpo[0]	274	OUT_CELL	dd[10]	135	OUT_CELL
scpi[0]	273	IN_CELL	ad[13]	134	IN_CELL
scpi[1]	272	IN_CELL	ad[14]	133	IN_CELL
scpi[2]	271	IN_CELL	ad[15]	132	IN_CELL
scpi[3]	270	IN_CELL	adp[2]	131	IN_CELL
prefen	269	IN_CELL	ad[10]	130	IN_CELL
peclv	268	IN_CELL	ad[11]	129	IN_CELL
pin[3]	267	IN_CELL	ad[12]	128	IN_CELL
Piclk	266	IN_CELL	ddp[1]	127	OUT_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
pin[2]	265	IN_CELL		apl[2]	126	IN_CELL
pin[1]	264	IN_CELL		Ac1j1v1_afp[2]	125	IN_CELL
pin[6]	263	IN_CELL		ad[8]	124	IN_CELL
pin[0]	262	IN_CELL		dd[3]	123	OUT_CELL
pin[5]	261	IN_CELL		ad[9]	122	IN_CELL
pin[4]	260	IN_CELL		dd[4]	121	OUT_CELL
Fpin	259	IN_CELL		dd[5]	120	OUT_CELL
pin[7]	258	IN_CELL		dd[6]	119	OUT_CELL
Tpl	257	OUT_CELL		dpl[1]	118	OUT_CELL
tclk	256	OUT_CELL		dd[7]	117	OUT_CELL
oof	255	OUT_CELL		Dc1j1v1[1]	116	OUT_CELL
tc1j1v1_tfpo	254	OUT_CELL		dd[0]	115	OUT_CELL
td[0]	253	OUT_CELL		dd[1]	114	OUT_CELL
td[1]	252	OUT_CELL		ad[5]	113	IN_CELL
td[2]	251	OUT_CELL		dd[2]	112	OUT_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
td[3]	250	OUT_CELL		ad[6]	111	IN_CELL
td[4]	249	OUT_CELL		ad[7]	110	IN_CELL
tfpi	248	IN_CELL		adp[1]	109	IN_CELL
td[5]	247	OUT_CELL		ad[1]	108	IN_CELL
td[6]	246	OUT_CELL		ad[2]	107	IN_CELL
td[7]	245	OUT_CELL		ack	106	IN_CELL
tdp	244	OUT_CELL		ad[3]	105	IN_CELL
tdck	243	IN_CELL		apl[1]	104	IN_CELL
ds3roclk[3]	242	OUT_CELL		ad[4]	103	IN_CELL
ds3roclk[2]	241	OUT_CELL		ac1j1v1_afp[1]	102	IN_CELL
ds3roclk[1]	240	OUT_CELL		ad[0]	101	IN_CELL
ds3rdat[4]	239	OUT_CELL		updoeb	100	IN_CELL
ds3roclk[4]	238	OUT_CELL		roh_oeb	99	IN_CELL
ds3rdat[3]	237	OUT_CELL		toh_oeb	98	IN_CELL
ds3rdat[2]	236	OUT_CELL		rld_oeb	97	IN_CELL
ds3rdat[1]	235	OUT_CELL		rsld_oeb	96	IN_CELL
ds3ticlk[2]	234	IN_CELL		tld_oeb	95	IN_CELL
ds3ticlk[1]	233	IN_CELL		tsld_oeb	94	IN_CELL
ds3ticlk[3]	232	IN_CELL		tfp	93	OUT_CELL
ds3ticlk[4]	231	IN_CELL		tack	92	IN_CELL
ds3tdat[4]	230	IN_CELL		pgmrclk	91	OUT_CELL
ds3tdat[3]	229	IN_CELL		tafp	90	IN_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
ds3tdat[2]	228	IN_CELL		Tad	89	IN_CELL
ds3tdat[1]	227	IN_CELL		rad	88	OUT_CELL
ds3roclk[5]	226	OUT_CELL		ttohclk	87	OUT_CELL
ds3roclk[6]	225	OUT_CELL		ttohen	86	IN_CELL
ds3roclk[7]	224	OUT_CELL		ttohfp	85	OUT_CELL
ds3roclk[8]	223	OUT_CELL		ttoh	84	IN_CELL
ds3rdat[8]	222	OUT_CELL		tohclk	83	OUT_CELL
ds3rdat[7]	221	OUT_CELL		toh	82	IN_CELL
ds3rdat[6]	220	OUT_CELL		tlow	81	IN_CELL
ds3rdat[5]	219	OUT_CELL		tsuc	80	IN_CELL
ds3ticlk[5]	218	IN_CELL		tsow	79	IN_CELL
ds3ticlk[6]	217	IN_CELL		towclk	78	OUT_CELL
ds3ticlk[7]	216	IN_CELL		tldclk	77	OUT_CELL
ds3ticlk[8]	215	IN_CELL		tld	76	IN_CELL
ds3tdat[5]	214	IN_CELL		tsldclk	75	OUT_CELL
ds3tdat[6]	213	IN_CELL		tsld	74	IN_CELL
ds3tdat[7]	212	IN_CELL		ttohrei	73	IN_CELL
ds3tdat[8]	211	IN_CELL		rfpo	72	OUT_CELL
ds3roclk[9]	210	OUT_CELL		rclk	71	OUT_CELL
ds3roclk[10]	209	OUT_CELL		rtohclk	70	OUT_CELL
ds3roclk[11]	208	OUT_CELL		rtohfp	69	OUT_CELL
ds3roclk[12]	207	OUT_CELL		rtoh	68	OUT_CELL
ds3rdat[12]	206	OUT_CELL		rohclk	67	OUT_CELL
ds3rdat[9]	205	OUT_CELL		roh	66	OUT_CELL
ds3rdat[10]	204	OUT_CELL		rlow	65	OUT_CELL
ds3rdat[11]	203	OUT_CELL		rsuc	64	OUT_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
ds3ticlk[9]	202	IN_CELL		rsow	63	OUT_CELL
ds3ticlk[10]	201	IN_CELL		rowclk	62	OUT_CELL
ds3ticlk[11]	200	IN_CELL		rldclk	61	OUT_CELL
ds3ticlk[12]	199	IN_CELL		rld	60	OUT_CELL
ds3tdat[9]	198	IN_CELL		rsldclk	59	OUT_CELL
ds3riclk	197	IN_CELL		rsld	58	OUT_CELL
ds3tdat[10]	196	IN_CELL		ralm	57	OUT_CELL
ds3tdat[11]	195	IN_CELL		salm	56	OUT_CELL
dmode[0]	194	IN_CELL		lof	55	OUT_CELL
ds3tdat[12]	193	IN_CELL		lais_rrcpdat	54	OUT_CELL
dmode[1]	192	IN_CELL		los_rrcpfp	53	OUT_CELL
dck	191	IN_CELL		lrdi_rrcpclk	52	OUT_CELL
dfp	190	IN_CELL		rlais_trcpclk	51	IN_CELL
ddp[4]	189	OUT_CELL		tlais_trcpdat	50	IN_CELL
dd[31]	188	OUT_CELL		tlrdi_trcpfp	49	IN_CELL
dd[30]	187	OUT_CELL		pgmtclk	48	OUT_CELL
dd[28]	186	OUT_CELL		gnd	47	IN_CELL
dd[29]	185	OUT_CELL		gnd	46	IN_CELL
dd[27]	184	OUT_CELL		rpoh	45	OUT_CELL
dd[26]	183	OUT_CELL		rpohen	44	OUT_CELL
dd[25]	182	OUT_CELL		rpohfp	43	OUT_CELL
dc1j1v1[4]	181	OUT_CELL		rpohclk	42	OUT_CELL
dd[24]	180	OUT_CELL		b3e	41	OUT_CELL
dpl[4]	179	OUT_CELL		tpohrdy	40	OUT_CELL
adp[4]	178	IN_CELL		tpoh	39	IN_CELL
ad[31]	177	IN_CELL		tpohen	38	IN_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
ad[30]	176	IN_CELL		Tpohfp	37	OUT_CELL
ad[29]	175	IN_CELL		dpais	36	IN_CELL
ad[28]	174	IN_CELL		tpohclk	35	OUT_CELL
ad[26]	173	IN_CELL		tpais	34	IN_CELL
ad[27]	172	IN_CELL		tpaisfp	33	IN_CELL
ad[25]	171	IN_CELL		tpaisck	32	IN_CELL
ad[24]	170	IN_CELL		dpaisfp	31	IN_CELL
ac1j1v1_afp[4]	169	IN_CELL		dpaisck	30	IN_CELL
apl[4]	168	IN_CELL		d[7]	29	IO_CELL
ddp[3]	167	OUT_CELL		d[6]	28	IO_CELL
dd[23]	166	OUT_CELL		d[5]	27	IO_CELL
dd[22]	165	OUT_CELL		d[4]	26	IO_CELL
dd[21]	164	OUT_CELL		d[3]	25	IO_CELL
dd[20]	163	OUT_CELL		d[2]	24	IO_CELL
dd[19]	162	OUT_CELL		d[1]	23	IO_CELL
dd[18]	161	OUT_CELL		d[0]	22	IO_CELL
dd[17]	160	OUT_CELL		intb	21	OUT_CELL
dd[16]	159	OUT_CELL		a[13]	20	IN_CELL
dc1j1v1[3]	158	OUT_CELL		a[11]	19	IN_CELL
dpl[3]	157	OUT_CELL		a[12]	18	IN_CELL
adp[3]	156	IN_CELL		a[10]	17	IN_CELL
ad[23]	155	IN_CELL		a[9]	16	IN_CELL
ad[22]	154	IN_CELL		a[8]	15	IN_CELL
ad[21]	153	IN_CELL		a[6]	14	IN_CELL
ad[20]	152	IN_CELL		a[7]	13	IN_CELL
ad[19]	151	IN_CELL		a[5]	12	IN_CELL
ad[18]	150	IN_CELL		a[4]	11	IN_CELL
ad[17]	149	IN_CELL		a[3]	10	IN_CELL
ad[16]	148	IN_CELL		a[1]	9	IN_CELL
ac1j1v1_afp[3]	147	IN_CELL		a[2]	8	IN_CELL
apl[3]	146	IN_CELL		a[0]	7	IN_CELL
ddp[2]	145	OUT_CELL		csb	6	IN_CELL

Pin / Enable	Register Bit	Cell Type		Pin / Enable	Register Bit	Cell Type
dd[11]	144	OUT_CELL		ale	5	IN_CELL
dd[12]	143	OUT_CELL		rdb_e	4	IN_CELL
dd[13]	142	OUT_CELL		mbeb	3	IN_CELL
dd[14]	141	OUT_CELL		wrb_rwb	2	IN_CELL
dd[15]	140	OUT_CELL		rstb	1	IN_CELL
dpl[2]	139	OUT_CELL				

NOTES:

1. updoeb is the active low output enable for D[7:0].
2. roh_oeb is the active low output enable for ROH, ROHCLK and RFPO.
3. toh_oeb is the active low output enable for TOHCLK and TFP.
4. rld_oeb is the active low output enable for RLD and RLDCLK.
5. rsld_oeb is the active low output enable for RSLD and RSLDCLK.
6. tld_oeb is the active low output enable for TLDCLK.
7. tsld_oeb is the active low output enable for TSLDCLK.
8. scpo_oeb is the active low output enable for SCPO[1:0]
9. hiz is the active low output enable for all cells of type OUT_CELL, EXCEPT those listed above.
10. RSTB is the first bit of the boundary scan chain.

13.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 17 -Input Observation Cell (IN_CELL)

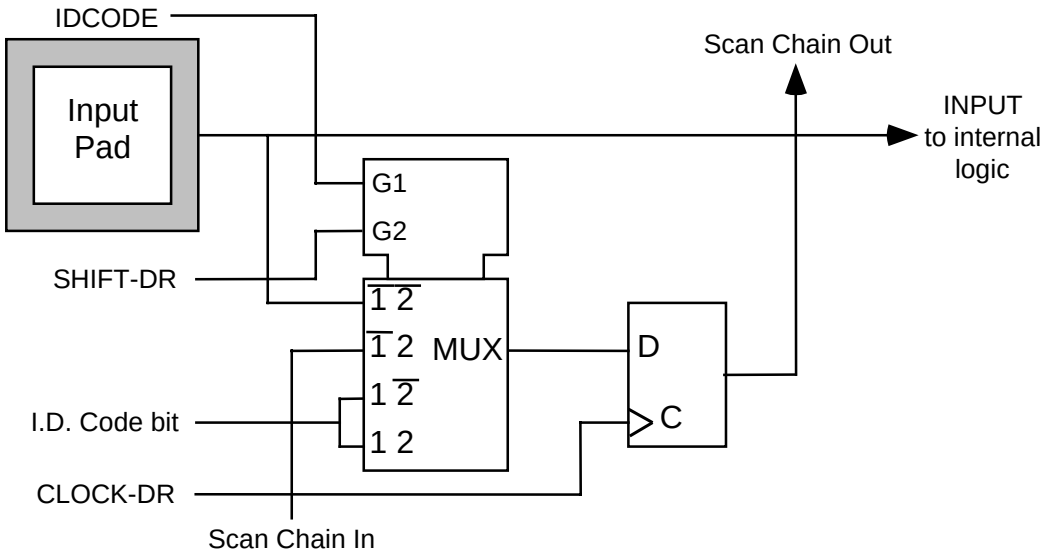


Figure 18 -Output Cell (OUT_CELL

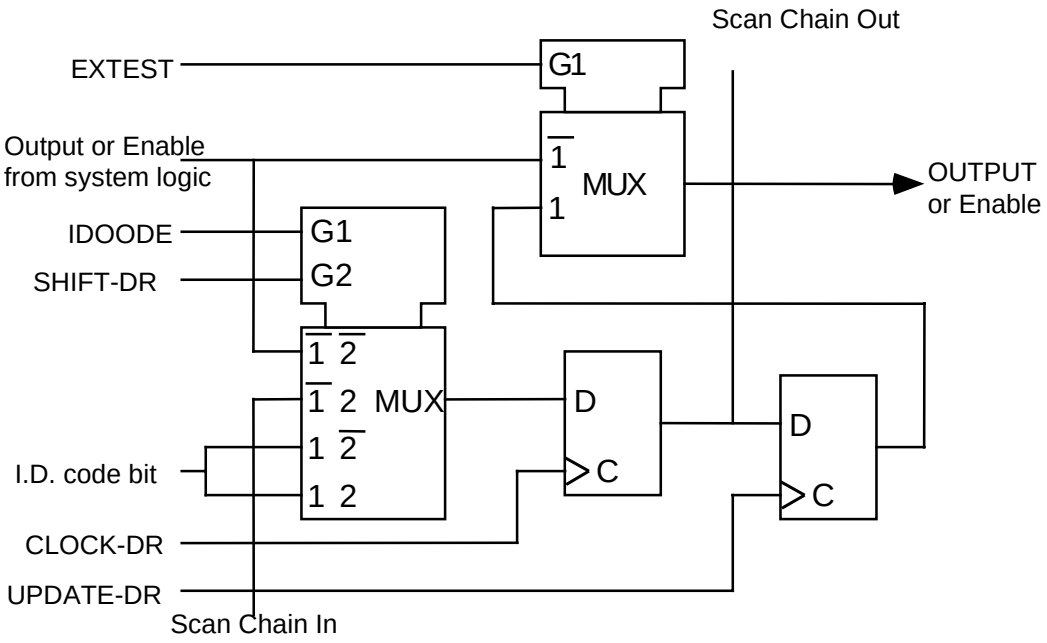
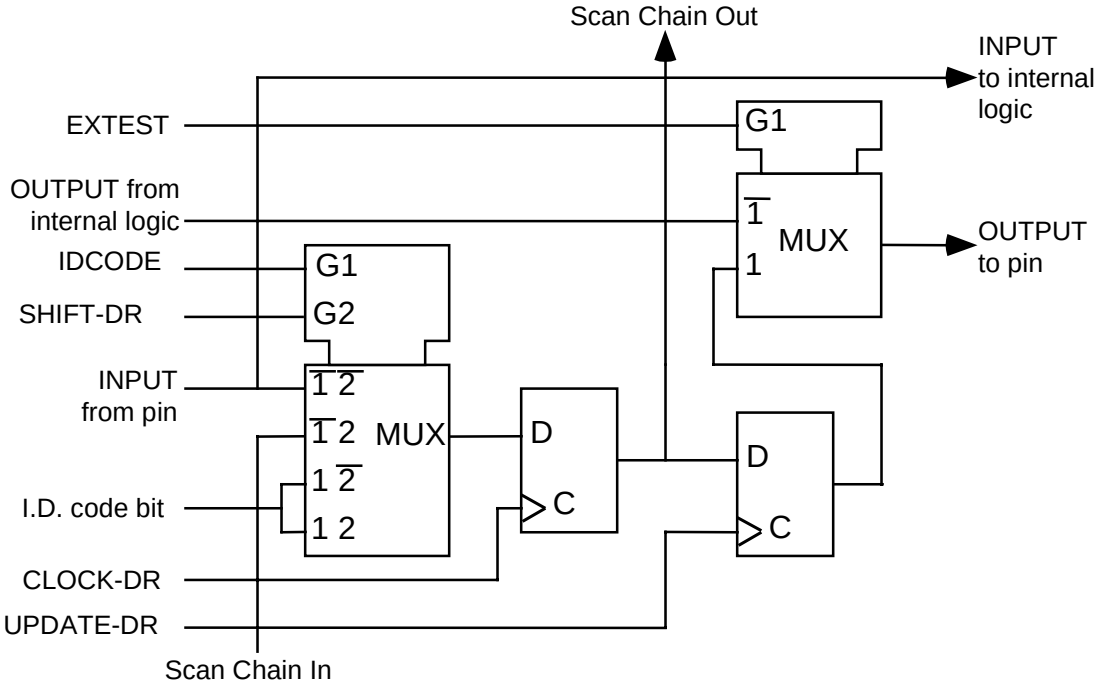
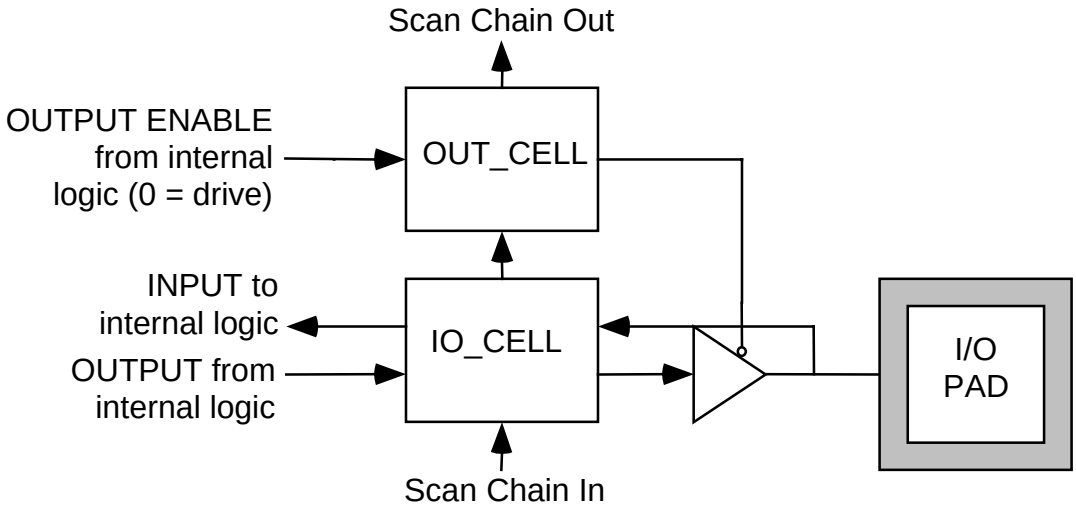


Figure 19 -Bi-directional Cell (IO_CELL)



-Layout of Output Enable and Bi-directional Cells



14 OPERATION

This section presents Configuration Options, PCB design recommendations, operating details for the JTAG boundary scan feature and interface details for system side devices.

The SPECTRA-622 is a SONET/SDH PAYLOAD EXTRACTOR/ALIGNER device. It processes the section, line, path overhead of an STS-12/12c (STM-4/AU3/AU4/AU4-Xc) stream. The SPECTRA-622 supports a rich set of line, path and system configuration options. The SPECTRA-622 also supports mapping and demapping of DS3 streams from SONET STS-1 payloads.

14.1 Software Initialization Sequence

After every reset or power up, the following operation need to be performed.

In order to activate the TX line interface, the TCLK must be enabled for a few clock cycles or the TX bypass mode must be enabled by setting the TESBYP bit in register 1030H. Either of those writes will activate the TX line interface, once done, those bits can be reprogrammed at any value.

The OUTDATA bit in register 0033H must be set to one for the accurate operation of the CRSI. This has to be done after every hardware or software reset and only once.

If no other registers are programmed, the device will start in the following mode. All slice will be in master mode, i.e. twelve STS-1. The APGM and DPGM are disabled, all interrupts are disabled and the line interface is programmed in serial mode, both RX and TX. The ADD and DROP bus will be running at 77.76 MHz and the ADD bus will be expecting a C1, J1 and V1 pulse.

14.2 Transport and Path Overhead Bytes

Under normal operating conditions, the SPECTRA-622 processes the complete transport overhead present in an STS-12/12c/STM-4/-4c stream. The byte positions processed by the SPECTRA-622 are indicated below.

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the serial or parallel stream. These bytes can also used to byte align the byte parallel received data.

J0 The J0 byte is currently defined as the section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler. The received section trace message is processed by the SSTB block and also available on the RTOH port. The transmit section trace message can be programmed in the SSTB, via the TTOH port or the TSOP block.

Z0: The Z0 bytes are currently defined as the section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler. The received section growth bytes are extracted and available on the RTOH port. The transmit section growth bytes can be programmed in the TTOC or optionally in the and TSOP blocks.

B1: The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the SPECTRA-622 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the SPECTRA-622 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in the error event counter of the RSOP .

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TLD and/or TSLD. Section DCC can also be inserted via the TTOH port controlled by the TTOC block.

In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RLD and/or RSLD. Section DCC is also extracted via onto the RTOH port via the RTOC block.

H1, H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the SPECTRA-622 TPOP block inserts a valid pointer with pointer adjustments to accommodate plesiochronous timing offsets between the references. The

concatenation indication must be programmed in the slave slices via the TPOP registers.

In the receive direction, the pointer is interpreted by the RPOP to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the SPECTRA-622 TLOP block calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the SPECTRA-622 RLOP block calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the K1 and K2 bytes can be inserted via the TTOH, TOH and TAD ports. The SPECTRA-622 also provides register control for the K1 and K2 bytes in the TLOP block.

In the receive direction, the SPECTRA-622 RASE block provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined by the RLOP block to determine the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the line DCC byte is inserted from a dedicated 576 kbit/s input, TLD. Line DCC can also be inserted via the TTOH port controlled by the TTOC block.

In the receive direction, the line DCC is extracted on a dedicated 576 kbit/s output, RLD. Line DCC is also extracted via onto the RTOH port via the RTOC block.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the SONET/SDH signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the SPECTRA-622 TTOC and TLOP blocks provide specific register control for the synchronization status byte.

In the receive direction, the SPECTRA-622 SSTB block provides register access to the synchronization status byte. The SSTB block also provides circuitry to detect synchronization status mismatch and unstable alarms. The RTOH provides access to the received S1 byte.

Z1: The Z1 bytes are allocated for future growth.

In the transmit direction, the SPECTRA-622 TTOC and TLOP blocks provide register control for the growth bytes.

In the receive direction, the SPECTRA-622 provides access to all growth bytes via the RTOH port.

M1: The M1 byte is provides a line far end block error function for remote performance monitoring.

In the transmit direction, the SPECTRA-622 the M1 byte is internally generated. The number of B2 errors detected in the previous interval is insert. The insertion may be overwritten via the TTOHREI or Ring control port.

In the receive direction, a legal M1 byte value is added to the line REI (FEBE) event counter in the RSOP block.

Z2: The Z2 bytes are future growth.

In the transmit direction, Z2 can be inserted with the TTOH port or programmed to be processed by the TTOC.

In the receive direction, Z2 bytes are extracted and made availble on the RTOH port.

Path Overhead Bytes

All receive path overhead bytes are extracted and presented onto the RPOH port. All transmit overhead bytes can be inserted via the TPOH port with exception of the B3 which can be masked via the supplied byte on TPOH.

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET/SDH networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TPOP Path Trace register or the SPTB block. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

B3: The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the SPECTRA-622 calculates the B3 bytes in the master TPOP block. The calculated code is then placed in the next frame.

In the receive direction, the SPECTRA-622 master RPOP block calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

C2: The path signal label indicator identifies the equipped payload type.

In the transmit direction, the SPECTRA-622 inserts the C2 value using the TPOP Path Signal Label register.

In the receive direction, the code is available in the RPOP Path Signal Label register. In addition, the SPTB block also provides circuitry to detect path signal label mismatch and unstable alarms.

G1: The path status byte provides a path REI (FEBE) function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the SPECTRA-622 provides register bits to control the path RDI states in the TPOP block. The path RDI may also be set via the TAD port. For path FEBE, the number of B3 errors detected in the previous interval is inserted either automatically or using a register in the TPOP block. This path FEBE code has 9 legal values, namely 0 to 8 errors. The TAD port may also be used to provide the REI count of a mate SPECTRA.

The TAD port can retrieve up to 15 BIP error for each slice per frame (125 us). Given the timing of the RAD port, a mate SPECTRA-622 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames and the timing makes them appear within one frame period, one count could be lost.

In the receive direction, a legal path FEBE value is accumulated in the path FEBE event counter of the RPOP. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers. The REI (FEBE) count is also available on the RAD port.

H4: The multi-frame indicator byte is a payload specific byte. The byte can be set by the TTAL block in the transmit stream. In the recive stream the RPOP can process the H4 and declare LOM.

Z3 - Z5: The path growth bytes provide three unused bytes for future use.

In the transmit direction the TPOP block and the TPOH port can be used to insert the Z5.

14.3 Line Configuration Options

14.3.1 STS-12/12c (STM-4/AU3/AU4/AU4-Xc) Mode

The SPECTRA-622 terminates and sources the path payload of a duplex STS-12/12c (STM-4/AU3/AU4/AU4-Xc) stream. The configuration options of the Receive/Transmit Path Processing Slices (RPPS/TPPS) to handle the different combinations of constituent STS-1/3/3c (STM-0/AU3 and STM-1/AU3/AU4) streams are described in the Path Processing Slice Configuration Options section below.

The Line side interfaces can be independently configured as serial 622.08 Mhz PECL interfaces or 77.76 Mhz byte parallel interfaces.

14.4 Path Processing Slice Configuration Options

14.4.1 Basic Configuration

The SPECTRA-622 Path Processing Slice architecture allows software to configure the device to handle any combinations of constituent STS-1/3/3c in an STS-12/12c SONET stream. Similarly, the device can be configured to handle any combinations of constituent STM-0/1/AU3/AU4 in an STM-4/4c SDH stream. The Slice Configuration for SDH STM-4 Path Processing table below shows three typical examples of an STM-4 SDH stream and the required configurations for SPECTRA-622 to correctly process them. The first column contains the slice number of the twelve TPPS's (RPPS's) in the SPECTRA-622. The corresponding order of byte transmission (reception) of the TPPS's (RPPS's) is shown in the second column of the table. The third and fourth columns contain the first two configuration examples involving a combination of STM-1/AU3/AU4 streams in an STM-4 being processed by the SPECTRA-622. The fifth column contains the third configuration example involving an STM-4-4c concatenated stream. In the third, fourth and fifth columns, the corresponding STM-0 stream in an STM-1 being processed by each TPPS (RPPS) is listed for each configuration example. The STM-0 stream label is highlighted and marked with a (M) symbol if the corresponding TPPS (RPPS) is configured as a master. Otherwise, it is only marked with a (S) symbol.

Table 20 - Slice Configuration for SDH STM-4 Path Processing

Slice #n	Tx/Rx Order	STM-4 AU3/AU4/AU3/AU3 Example 1	STM-4 AU4/AU4/AU3/AU4 Example 2	STM-4 AU4-4c Example 3
1	1	**STM-1 #1 AU3 #1 (M)**	**STM-1 #1 TUG3 #1 (M)**	**STM-1 #1 TUG3 #1 (M)**
5	5	**STM-1 #1 AU3 #2 (M)**	STM-1 #1 TUG3 #2 (S)	STM-1 #1 TUG3 #2 (S)
9	9	**STM-1 #1 AU3 #3 (M)**	STM-1 #1 TUG3 #3 (S)	STM-1 #1 TUG3 #3 (S)
2	2	**STM-1 #2 TUG3 #1 (M)**	**STM-1 #2 TUG3 #1 (M)**	STM-1 #2 TUG3 #1 (S)
6	6	STM-1 #2 TUG3 #2 (S)	STM-1 #2 TUG3 #2 (S)	STM-1 #2 TUG3 #2 (S)
10	10	STM-1 #2 TUG3 #3 (S)	STM-1 #2 TUG3 #3 (S)	STM-1 #2 TUG3 #3 (S)
3	3	**STM-1 #3 AU3 #1 (M)**	**STM-1 #3 AU3 #1 (M)**	STM-1 #3 TUG3 #1 (S)
7	7	**STM-1 #3 AU3 #2 (M)**	**STM-1 #3 AU3 #2 (M)**	STM-1 #3 TUG3 #2 (S)
11	11	**STM-1 #3 AU3 #3 (M)**	**STM-1 #3 AU3 #3 (M)**	STM-1 #3 TUG3 #3 (S)
4	4	**STM-1 #4 AU3 #1 (M)**	**STM-1 #4 TUG3 #1 (M)**	STM-1 #4 TUG3 #1 (S)
8	8	**STM-1 #4 AU3 #2 (M)**	STM-1 #4 TUG3 #2 (S)	STM-1 #4 TUG3 #2 (S)
12	12	**STM-1 #4 AU3 #3 (M)**	STM-1 #4 TUG3 #3 (S)	STM-1 #4 TUG3 #3 (S)

In the first example, the STM-4 stream consists of STM-1/AU3 #1, STM-1/AU4 #2, STM-1/AU3 #3 and STM-1/AU3 #4. To process the individual STM-0/AU3 streams in the STM-1/AU3 #1, #3 and #4, the corresponding TPPS's (RPPS's) (Slice #1, #5, #9, #3, #7, #11, #4, #8, #12) must all be configured as masters via the TPPS (RPPS) Configuration registers. For the STM-1/AU4 #2 concatenated stream, only the TPPS (RPPS) #2 which handles the constituent TUG3 #1 needs to be configured as a master. TPPS (RPPS) #6 and #10 handling TUG3 #2 and TUG3 #3 respectively are configured as slaves.

In the second example, the STM-4 stream consists of STM-1/AU4 #1, STM-1/AU4 #2, STM-1/AU3 #3 and STM-1/AU4 #4. To process the STM-1/AU4 #1, #2 and #4 concatenated streams, only the TPPS's (RPPS's) (Slice #1, #2, #4) which process TUG3 #1 in the STM-1/AU4 streams are configured as masters via the corresponding TPPS (RPPS) Configuration registers. The remaining TPPS's (RPPS's) handling the TUG3 #2 and TUG3 #3 streams are configured as slaves. For the STM-1/AU3 #3, all three associated TPPS's (RPPS's) (#3, #7, #11) need to be configured as masters to process the individual STM-0/AU3 streams.

In the third example, an STM-4-4c stream is being processed by the SPECTRA-622. To process this concatenated stream, only the TPPS (RPPS) #1 which processes TUG3 #1 in the STM-1 #1 stream needs to be configured as the master via the TPPS (RPPS) Configuration register. The rest of the TPPS's

(RPPS's) (Slice #2 - #12) handling the remaining eleven TUG3 streams in the STM-4-4c are configured as slaves.

The equivalent configuration examples for SONET are illustrated in the Slice Configuration for SONET STS-12/12c Path Processing table below.

Table 21 - Slice Configuration for SONET STS-12/12c Path Processing

Slice #n	Tx/Rx Order	STS-12 STS-3/3c/3/3	STS-12 STS-3c/3c/3/3c	STS-12c
1	1	**STS-3 #1 STS-1 #1 (M)**	**STS-3c #1 STS-1 #1 (M)**	**STS-12c STS-1 #1 (M)**
5	5	**STS-3 #1 STS-1 #2 (M)**	STS-3c #1 STS-1 #2 (S)	STS-12c STS-1 #5 (S)
9	9	**STS-3 #1 STS-1 #3 (M)**	STS-3c #1 STS-1 #3 (S)	STS-12c STS-1 #9 (S)
2	2	**STS-3c #2 STS-1 #1 (M)**	**STS-3c #2 STS-1 #1 (M)**	STS-12c STS-1 #2 (S)
6	6	STS-3c #2 STS-1 #2 (S)	STS-3c #2 STS-1 #2 (S)	STS-12c STS-1 #6 (S)
10	10	STS-3c #2 STS-1 #3 (S)	STS-3c #2 STS-1 #3 (S)	STS-12c STS-1 #10 (S)
3	3	**STS-3 #3 STS-1 #1 (M)**	**STS-3 #3 STS-1 #1 (M)**	STS-12c STS-1 #3 (S)
7	7	**STS-3 #3 STS-1 #2 (M)**	**STS-3 #3 STS-1 #2 (M)**	STS-12c STS-1 #7 (S)
11	11	**STS-3 #3 STS-1 #3 (M)**	**STS-3 #3 STS-1 #3 (M)**	STS-12c STS-1 #11 (S)
4	4	**STS-3 #4 STS-1 #1 (M)**	**STS-3c #4 STS-1 #1 (M)**	STS-12c STS-1 #4 (S)
8	8	**STS-3 #4 STS-1 #2 (M)**	STS-3c #4 STS-1 #2 (S)	STS-12c STS-1 #8 (S)
12	12	**STS-3 #4 STS-1 #3 (M)**	STS-3c #4 STS-1 #3 (S)	STS-12c STS-1 #12 (S)

The valid master/slave slice configurations table below provides a list of all valid Path Processing Slice configurations and the corresponding STS-12 (STM-4) SONET/SDH streams being processed. A master Slice is marked with the symbol '**M**' and a slave Slice is marked with the symbol 'S'. (X_a,X_b) represents a pair of master or slave Slices. For example, (X_a,X_b) for Slice #5 and #9 must be a pair of slave Slices when Slice #1-#5-#9 are processing an STS-3c (STM-1/AU4) stream. (X_a,X_b) must be a pair of master Slices when Slice #1-#5-#9 are processing an STS-3 (STM-1/AU3) stream. The notation "3(c)" represents an STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) stream.

Table 22 - Valid Master/Slave Slice Configurations

STS-12 (STM-4)	Path Processing Slice #											
	1	**5**	**9**	**2**	**6**	**10**	**3**	**7**	**11**	**4**	**8**	**12**
STS-12c	**M**	S	S	S	S	S	S	S	S	S	S	S
3(c)/3(c)/3(c)/3(c)	**M**	X_a	X_b	**M**	X_a	X_b	**M**	X_a	X_b	**M**	X_a	X_b
STS-3/3/3/3	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**

In the SPECTRA-622, when a Path Processing Slice #i is configured as a master, it controls all slave Slices #j up to the next intervening master Slice #k. For the STS-12c example in the above table, i =1 and j = {2 .. 12} and there is no intervening master Slice #k. When there is an intervening master Slice #k as in the STS-3(c)/3(c)/3(c)/3(c) example where k = {2, 3, 4}. Slices #j where j = {{5, 9},{6,10},{7,11},{8,12}} will be controlled by Slice #i (i = {1, 2, 3, 4}) respectively. This flexible Slice architecture can be configured to support a wide variety of STS-12 (STM-4) SONET/SDH streams consisting of various combinations of constituent STS-1/3/3c (STM-0/STM-1/AU3/AU4 or AU-4-4c) streams.

14.4.2 Additional Configuration for Transmit Concatenated Stream Support

To support the transmission of a concatenated stream, the TPOP block in the slave Transmit Path Processing Slice (TPPS) must be software configured to transmit a pointer in the H1 and H2 bytes identical to the concatenation indication (H1=93H, H2=FFH). This is achieved by first writing 93H and FFH into the TPOP Payload Pointer MSB and TPOP Payload Pointer LSB registers, respectively. The FTPTR and the NDF bits in the TPOP Pointer Control register must then be set high to activate the new pointer insertion in the transmit stream. The TDIS bit in the SPECTRA-622 TPPS Path Transmit Control register must also be set high to allow the payload bytes which correspond to the “path overhead” bytes of the STS-1 (STM-0/AU3) equivalent stream from the ADD bus to be transmitted with no modification. Transmit path overhead insertion via the TPOH input for the STS-1 (STM-0/AU3) equivalent stream being processed by the slave TPOP must not be enabled.

14.4.3 Concatenated and Non-concatenated Streams detection

Each Receive (Transmit) Path Processing Slice (RPPS/TPPS) processes an STS-1 (STM-0/AU3) or equivalent stream in an STS-3/3c/12/12c (STM-4/AU3/AU4/AU4-Xc) receive (ADD bus) stream. It is capable of detecting error-free and errored pointers as well as error-free and errored concatenation indications in the H1 and H2 pointer bytes concurrently, regardless of whether it is operating as a master or a slave. Errored pointers are indicated with the Loss-

Of-Pointer (LOP) status and errored concatenation indications are reported as an AU3 Loss-Of-Pointer-Concatenation (AU3LOPCON) in the RPOP (TPIP) Status and Control register.

Under normal operating conditions, the LOP status in a master slice is set low while the AU3LOPCON is set high. The opposite is true for a slave slice; the LOP status is set high while the AU3LOPCON status is set low. By monitoring LOP and AU3LOPCON, it is possible to detect for mismatches between the configuration of the receive (ADD bus) stream and the provisioning of the SPECTRA-622.

For ADD bus concatenated/non-concatenated streams detection to function, valid H1 and H2 must be provided in the ADD bus SPE data stream and the ADD bus must be configured to interpret the pointer (see Table 8).

14.4.4 PRBS Generator/Monitor Configuration for Concatenated streams

For an STS-12 (STM-4/AU3) ADD or DROP bus stream, the (APGM/DPGM) PRBS Generator and Monitor, in each Path Processing Slice (PPS) handling an STS-1 (STM-0/AU3), can be independently configured and enabled without affecting the PRBS generation or monitoring performed by other PPS's. However, for concatenated streams such as STS-3c (STM-1/AU4) or STS-12c (STM-4-4c), a group re-start of the PRBS generation is required after all the PRBS Generators within the PPS group have been configured and enabled by setting the GEN_REGEN bit in the (APGM/DPGM) Generator Control register of the master Path Processing Slice. The software group re-start will align all the PRBS Generators to produce a complete and valid sequence for the concatenated stream. Alarm such as Loss-Of-Pointer (LOP) or Path AIS (PAIS) may cause mis-alignment between PRBS Generators in the PPS group and may persist after the alarm has been removed. Mis-alignment is indicated by the signature status (GEN_SIGV) bit in the (APGM/DPGM) Generator/Monitor Status/Interrupt register of a slave Path Processing Slice. A software group re-start is required to recover from this condition.

The PRBS Monitors in a PPS group processing a concatenated stream operate independently of each other. If the monitored PRBS sequence is formed by mis-aligned sub-sequences (due to mis-aligned Generators or incorrect muxing order), the PRBS Monitors in the slave Path Processing Slices will indicate that they have locked on to the corresponding sub-sequences. However, the mis-alignment will be indicated by the signature status (MON_SIGV) bit in the (APGM/DPGM) Generator/Monitor Status/Interrupt register of a slave Path Processing Slice.

14.5 Time Slot Interchange (Grooming) Configuration Options

The Telecom Bus STS-1 (STM-0/AU3) Time-slots (Streams) table below list all the Telecom ADD/DROP bus streams or time-slots for the three different Telecom Bus configurations. The Input/Output order of the STS-1 (STM-0/AU3) streams or time-slots is provided for each Telecom Bus configuration.

Table 23 -Telecom Bus STS-1 (STM-0/AU3) Time-slots (Streams)

"STS-1/AU3" Telecom Bus Time-Slots (Streams)	4 x 19.44 MHz Buses		1x 77.76 MHz Bus	
	I/O Order	Data Bus	I/O Order	Data Bus
STM-1 #1 AU3 #1	1	**AD[7:0] DD[7:0]**	1	**AD[7:0]** **DD[7:0]**
STM-1 #1 AU3 #2	2		5	
STM-1 #1 AU3 #3	3		9	
STM-1 #2 AU3 #1	1	**AD[15:8] DD[15:8]**	2	
STM-1 #2 AU3 #2	2		6	
STM-1 #2 AU3 #3	3		10	
STM-1 #3 AU3 #1	1	**AD[23:16] DD[23:16]**	3	
STM-1 #3 AU3 #2	2		7	
STM-1 #3 AU3 #3	3		11	
STM-1 #4 AU3 #1	1	**AD[31:24] DD[31:24]**	4	
STM-1 #4 AU3 #2	2		8	
STM-1 #4 AU3 #3	3		12	

Grooming of STS (AU) streams at the Telecom DROP bus(es) is achieved by selecting an STS-1 (STM-0/AU3) or equivalent receive stream (i.e. time-slot or column in an STS-12/STM-4 frame) for each DROP bus time-slot other than its default. Any receive stream can be selected for DROP bus time-slot STM-1 #i AU3 #j using the STM1SEL[1:0] and AU3SEL[1:0] bits in the corresponding SPECTRA-622 Drop Bus STM-1 #i AU3 #j Select register. Normally, each STS-1 (STM-0/AU3) receive stream is selected only for one DROP bus time-slot. DROP bus multicast is achieved when the same STS-1 (STM-0/AU3) receive stream is selected for multiple DROP bus time-slots.

Similarly, grooming of STS (AU) streams at the Telecom ADD bus(es) is achieved by selecting an STS-1 (STM-0/AU3) or equivalent ADD bus stream (i.e. time-slot or column in an STS-12/STM-4 frame) for each transmit time-slot other than its default. Any ADD bus stream can be selected for transmit time-slot STM-1 #i AU3 #j using the STM1SEL[1:0] and AU3SEL[1:0] bits in the corresponding

SPECTRA-622 Add Bus STM-1 #i AU3 #j Select register. Normally, each ADD bus STS-1 (STM-0/AU3) stream is selected only for a single transmit time-slot. ADD bus multicast is achieved when the same STS-1 (STM-0/AU3) ADD bus stream is selected for multiple transmit time-slots.

The default settings in the SPECTRA-622 Add/Drop Bus STM-1 #i AU3 #j Select registers disable all grooming functions.

14.6 System Interface Configuration Options

14.6.1 Single 77.76 MHz Byte Telecom Bus Mode

The Single 77.76 MHz Byte Telecom Bus Mode is selected by setting the ATMODE bit in the SPECTRA-622 ADD Bus Configuration register to low (for ADD bus) and the DTMODE bit in the SPECTRA-622 DROP Bus Configuration register to low (for DROP bus). In addition for the DROP Bus, the Telecom bus must be enabled by setting the DMODE inputs or register bits to “01b” or “11b”. When operating in this mode, system data is delivered to the SPECTRA-622 via an eight bit ADD bus (AD[7:0]) and is sourced by the SPECTRA-622 via an eight bit DROP bus (DD[7:0]). For the ADD bus, the SPECTRA-622 requires either a composite C1, J1, V1 input or optionally a C1 or AFP signal coupled with a valid H1, H2 pointer.

The ADD bus and the DROP bus timing domains can be asynchronous to each other as well as to the transmit and receive line side interfaces. The SPECTRA-622 compensates for timing differences via pointer justifications.

14.6.2 Four 19.44 MHz Byte Telecom Bus Mode

The Four 19.44 MHz Byte Telecom Bus Mode is selected by setting the ATMODE bit in the SPECTRA-622 ADD Bus Configuration register to high (for ADD bus) and the DTMODE bit in the SPECTRA-622 DROP Bus Configuration register to high (for DROP bus). In addition for the DROP Bus, the Telecom bus must be enabled by setting the DMODE inputs or register bits to “01b” or “11b”. When operating in this mode, system data is delivered to the SPECTRA-622 via four eight bit ADD buses (AD[7:0], AD[15:8], AD[23:16], AD[31:24]) and is sourced by the SPECTRA-622 via four eight bit DROP buses (DD[7:0], DD[15:8], DD[23:16], DD[31:24]). For the ADD buses, the SPECTRA-622 requires either a composite C1, J1, V1 input or optionally a C1 or AFP signal coupled with a valid H1, H2 pointer. All four C1 or AFP signals must always be aligned.

Both the ADD bus and the DROP bus timing domains can be asynchronous to each other as well as to the transmit and receive line side interfaces. The SPECTRA-622 compensates for timing differences via pointer justifications.

14.6.3 Serial DS3 Mode

The Serial DS3 mode for DROP side is configured by setting the DMODE bits in the SPECTRA-622 DROP Bus Configuration register to ‘b10 or ‘b110. The ADD side is configured by setting the DS3ADDSEL bit in the SPECTRA-622 TPPS Path and DS3 Configuration register of the TPPS to high. The SPECTRA-622 may be configured to support up to twelve independent ADD interfaces (DS3TDAT[12:1]) and up to twelve independent DROP interfaces (DS3RDAT[12:1]). In the receive direction, the DS3 de-mapper/framer provides a DS3 output clock (DS3ROCLK[12:1]) which is a gapped version of the SONET line clock or a gapped version of an externally provided 44.928 MHz clock (DS3RICLK). The REFCLK is required to use the SONET line clock. In the transmit direction, the DS3 source clock is provided externally (DS3TICLK[12:1]).

14.6.4 DROP Bus Mode

The DROP Bus interface can be configured to have enabled either the Telecom bus or DS3 interface, or both. The DMODE register bits or the DMODE inputs may be used to configure the DROP Bus interface. The DMODE inputs can be used to strap the device’s DROP Bus Mode when the DMODE bits are kept at “00b”. Setting the DMODE register bits to “00b” will enable the DMODE inputs to set the DROP mode. Setting the register bits to anything other than “00b” will set the DROP mode to the programmed setting.

DMODE[1:0]	Selected DROP Mode
01	Telecom Mode
10	DS3 Mode
11	Dual Mode

In the single Telecom mode, the DS3 blocks inside the device are held in reset and the DS3 DROP outputs will be forced low. In the single DS3 mode, the DROP Telecom blocks inside the device are held in reset and the Telecom DROP outputs will be forced low.

14.7 Bit Error Rate Monitor

The SPECTRA-622 provides two BERM blocks. One can be dedicated to monitoring the Signal Degrade (SD) error rates and the other dedicated to monitoring the Signal Fail (SF) error rates.

The Bit Error Rate Monitor (BERM) block counts and monitor line BIP errors over programmable periods of time (window size). At the associated thresholds, it declares an alarm or clears it if the alarm is already set. A different threshold and accumulation period must be used for declaring and clearing alarms regardless of whether the two operations are set to the same BER threshold. The following table list the recommended content of the BERM registers for different error rates (BER). Both BERMs in the TSB are equivalent and are programmed similarly. In a normal application, they will be set to monitor different BER's.

When the SF/SD CMODE bit is set to one, the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is set to zero, the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The table indicates the declare BER and evaluation period only.

The Saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

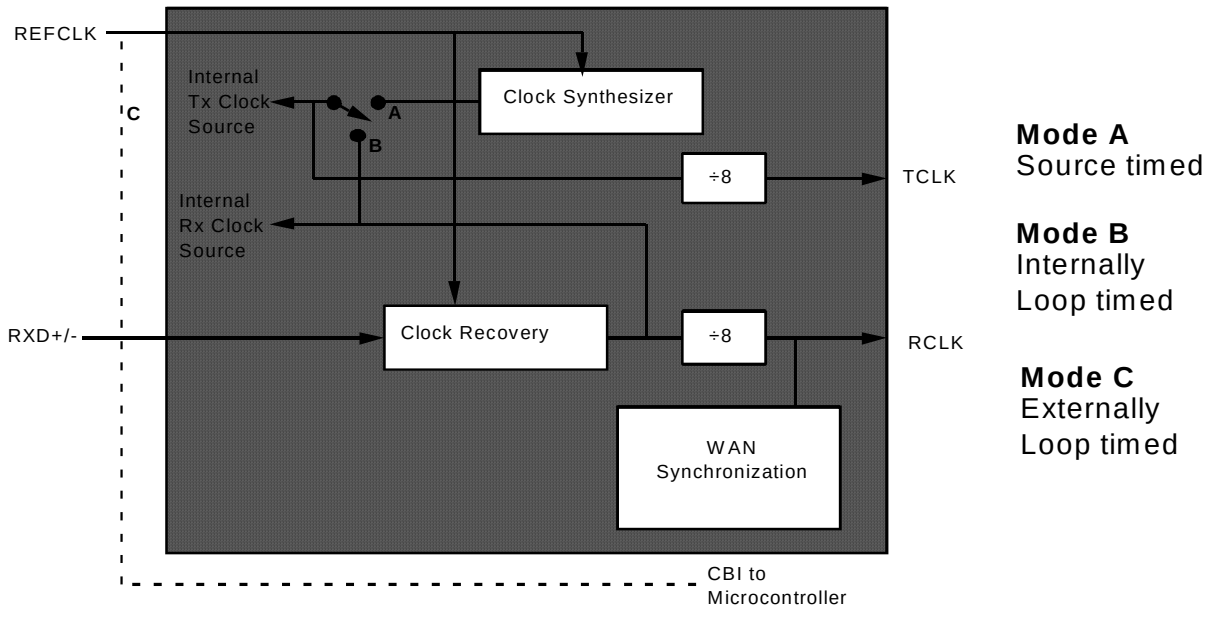
Table 24 -Recommended BERM settings

Declare BER	Evals Per Second	SF/SD SMODE	SF/SD CMODE	SF/SD SAP	SF/SD DTH	SF/SD CTH
10^{-3}	0.008	0	0	0x000008	0x956	0x1E9
10^{-4}	0.008	0	1	0x000008	0x1A5	0x03D
10^{-5}	0.025	0	1	0x000019	0x084	0x08E
10^{-6}	0.250	0	1	0x0000FA	0x085	0x08E
10^{-7}	2.500	0	1	0x0009C4	0x085	0x08E
10^{-8}	21.000	0	1	0x005208	0x06E	0x079
10^{-9}	167.000	0	1	0x028C58	0x056	0x062

14.8 Clocking Options

The SPECTRA-622 supports several clocking modes. Figure 20 is an abstraction of the clocking topology.

Figure 20 -Conceptual Clocking Structure



Mode A is provided for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a public UNI must conform to SONET Network Element (NE) requirements specified in Bellcore GR-253-CORE (1995 issue). These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and holdover. The 77.76 MHz clock source is typically a VCO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of 77.76 MHz to comply with the SONET/SDH network element free-run accuracy requirements. The SPECTRA-622 WANS block can be used to implement the system timing reference.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires an oscillator free-running at 77.76 MHz.

Mode A is selected by clearing the LOOPT bit of the Channel Control register. REFCLK is multiplied by 8 to become the 622.08 MHz transmit clock. REFCLK must be jitter free. The source REFCLK is also internally used as the clock recovery reference.

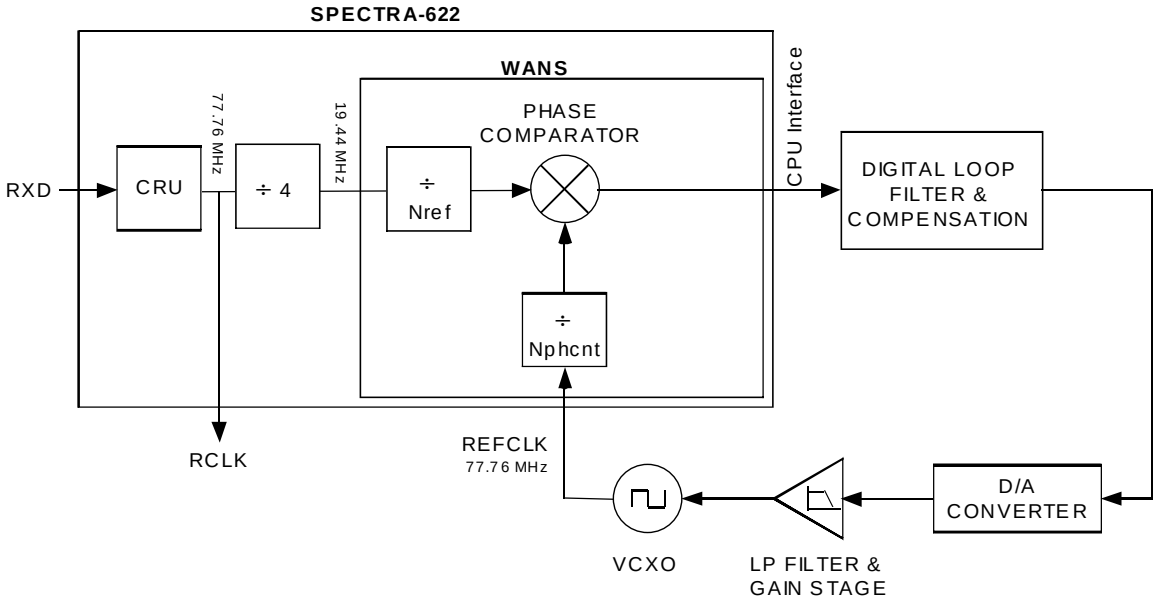
Mode B is provided for private UNIs and private NNIs that require synchronization to the recovered clock. Mode B is selected by setting the LOOPT bit of the Master Control register. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal condition, the transmit clock is synthesized from REFCLK.

Mode C is the external loop timing mode which make use of the WAN Synchronization block capabilities. This mode can be achieved when LOOPT is set to logic 0. The timing loop is achieved at the system level, through a microprocessor, an external VCXO and back into the REFCLK input. This mode allows an interface to meet Bellcore wander transfer and holdover stability requirements.

14.9 WAN Synchronization Parameters

The WANS implements a phase detector that can be used in the implementation of a digital PLL. Below, Figure 25, is a high level representation of a typical implementation of a high stability digital loop filter. In this circuit, the temperature and VCXO linearity compensation is performed digitally, although other techniques could be used.

Figure 25. Digital PLL Block Diagram



14.9.1 PLL Gain

The gain of the PLL is function of the Phase Detector sensitivity, the averaging process, the DLF transfer functions and other functions external to the WANS like the DAC and VCXO sensitivity, external compensation and buffering stages. The averaging process of the Phase Detector, by adding a fractional part to PHAWORD and shifting its integer part to the left, adds a gain the its transfer function. The value is equal to the number of averaging samples.

$$G(s) = \frac{K\text{pd} \times AF(s) \times LF(s) \times K\text{dac} \times K\text{vco}}{N}$$

where Kpd is the phase detector sensitivity
$AF(s)$ is the transfer function of the averaging process
$LF(s)$ is the transfer function of the DLF
Kdac is the DAC sensitivity
Kvco is the VCXO sensitivity

14.9.2 Phase Comparator

The Reference Period and the Phase Count Period registers define the division ration between the RCLK and VCOCLK. They need to be programmed so both periods are equal. The value programmed into the reference period and phase counter registers is one less than the actual count.

$$Tref = Trclk \times Nref = Tvcoclk \times Nphcnt$$

where Nref = REFPER + 1
Nphcnt = PHCNTPER + 1

The Phase Detector sensitivity is equal to:

$$Kpd = \frac{Nphcnt}{2\pi}$$

14.9.3 Phase Sample Averaging

The Averaging Period defines the number of Phase Count samples averaged together to create the Phase Word (PHAWORD). The number of averaging samples is expressed as a power of 2 with AVGPER. This period is equal to:

$$Tavg = Tref \times Navg = Tref \times 2^{AVGPER}$$

PHAWORD is a 31 bit wide word that includes an integer and fractional part. The fractional part is LSB aligned. Its width varies depending on the number of samples includes in the average with the number of bit equals to AVGPER value. The integer part is 16 bit wide. PHAWORD does not include a fractional part when AVGPER is equal to 0. When the fractional part of PHAWORD has less than 15 bits, the MSBs are padded with logic 0. The following gives an example for PHAWORD with an averaging period of 1024 (AVGPER = 10).

Bit	30 26	25 10	9 0
Value	0 0	PHAWORD Int	PHAWORD Frac

The PHAWORD sets the format for all downstream operations of the WANS, i.e. the fractional part is carried over to operations performed on PHAWORD.

14.9.4 Implementation Example

It was determine experimentally that using a frequency of 8kHz for acquiring Phase Sample and using 1024 samples for averaging provided a good compromise between PLL agility and stability. This will give the following programming parameters for the Phase comparator:

Tref = 1/8000 = 125uS

REFPER = (Tref/Trclk) – 1 = (125 * 10^-6/51.44 * 10 ^-9) –1 = 2429

PHCNTPER = (Tref/Tvcoclk) – 1 = (125 * 10^-6/12.86 * 10 ^-9) – 1 = 9719

AVGPER = 1024

14.10 Loopback Operation

The SPECTRA-622 supports five loopback functions: line loopback, system-side line loopback, DS3 line loopback, parallel diagnostic loopback and serial diagnostic loopback. The loopback modes are activated by the SLLE, PDLE and SDLE bits contained in the SPECTRA-622 Configuration register and the SLLBEN and DS3LLBEN bits in the SPECTRA-622 TPPS Configuration register.

The line loopback (SLLE=1) connects the high speed receive data and clock to the high speed transmit data and clock, and can be used for line side investigations (including clock recovery and clock synthesis). While in this mode, the entire receive path is operating normally.

The serial diagnostic loopback (SDLE=1) connects the high speed transmit data and clock to the high speed receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The parallel diagnostic loopback (PDLE=1) connects the byte wide transmit data and clock to the byte wide receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The system-side line loopback (SLLBEN=1) connects the STS-1 (STM-0/AU3) or equivalent receive stream from the Receive Telecom bus Aligner (RTAL) of the associated RPPS to the Transmit Telecom bus Aligner (TTAL) of the corresponding TPPS. This mode can be used for line side investigations (including clock recovery and clock synthesis) as well as path processing investigations. While in this mode, the entire receive path is operating normally.

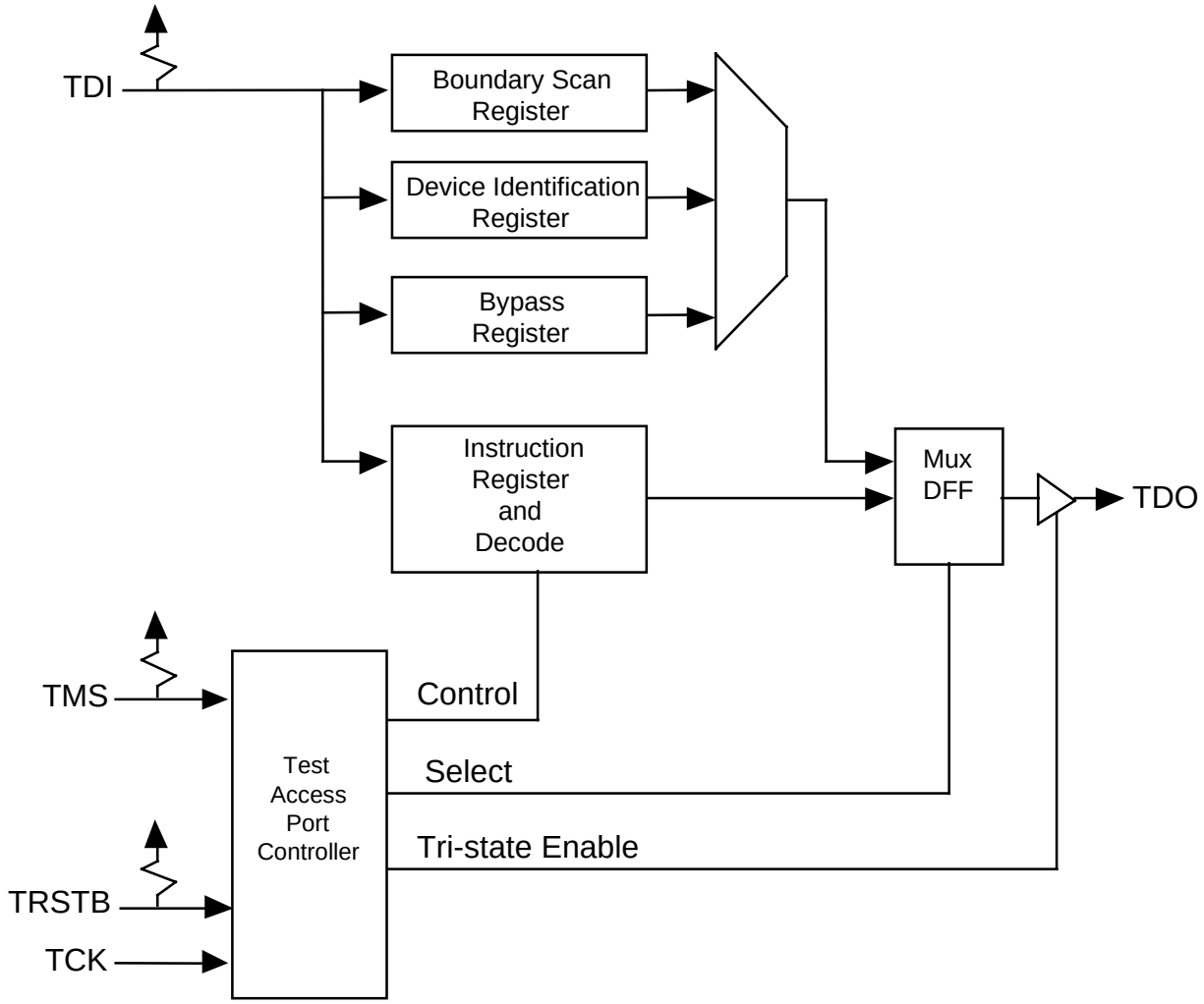
The SPECTRA-622 may be configured to support the system-side line loopback of up to twelve STS-1 (STM-0/AU3) or equivalent receive streams.

The DS3 line loopback (DS3LLBEN=1) connects the DS3 receive stream from the DS3 Mapper DROP side (D3MD) of the associated RPPS to the DS3 Mapper ADD side (D3MA) of the corresponding TPPS. The DS3ADDSEL bit in the SPECTRA-622 TPPS Path and DS3 Configuration register of the TPPS must also be set high. This mode can be used for line side investigations (including clock recovery and clock synthesis) as well as DS3 stream processing investigations. While in this mode, the entire receive (DS3) path is operating normally. The SPECTRA-622 may be configured to support the DS3 line loopback of up to twelve DS3 receive streams.

14.11 JTAG Support

The SPECTRA-622 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 26 -Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

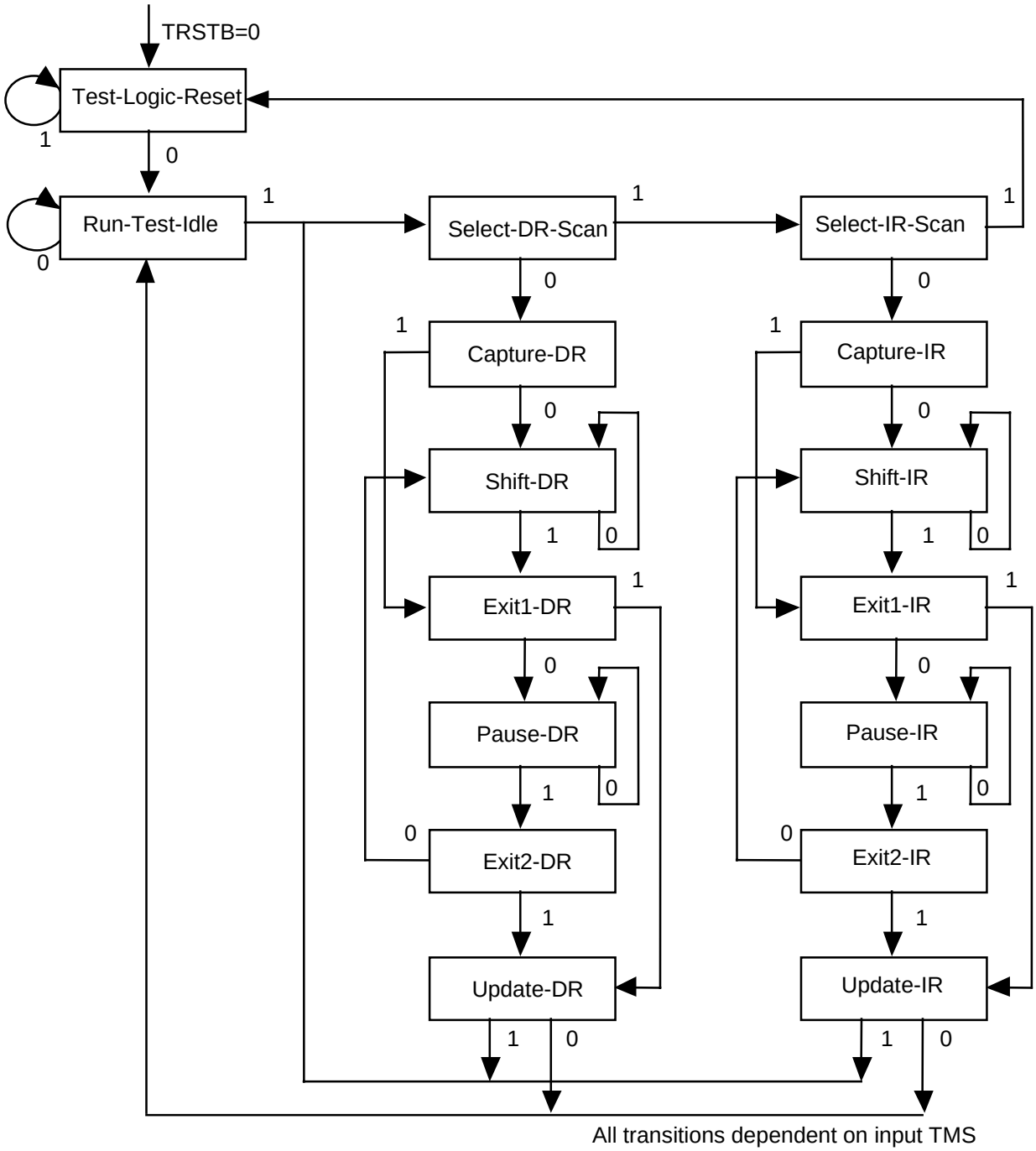
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

14.11.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 27 -TAP Controller Finite State Machine



14.11.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

14.11.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary

device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14.12 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

1. Use a single plane for both digital and analog grounds.

2. Provide separate +3.3 volt analog transmit, +3.3 volt analog receive, and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volts is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

4. High-frequency decoupling capacitors are recommended for the analog power pins as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into some reference circuitry. See the section on Power Supplies for more details.

5. The high speed serial streams (TXD+/-, RXD+/, and RRCLK+/-) must be routed with 50 ohm controlled impedance circuit board traces and must be

terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device. See the section on interfacing to ECL and PECL devices for more details.

14.13 Power Supplies

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. The recommended power supply sequencing follows:

1.) To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification.

2.) QAVD power must be supplied either after VDD or simultaneously with VDD to prevent current flow through the ESD protection devices which exist between QAVD and VDD power supplies. To prevent forward biasing the ESD protection diode between QAVD and VDD supplies, the differential voltage measured between these power supplies must be less than 0.5 volt.

This recommended differential voltage is to include peak to peak noise on the VDD power supply as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply.

3.) BIAS voltages (VBIAS and PBIAS) must be supplied either before VDD or simultaneously with VDD to prevent current flow through the ESD protection devices which exist between BIAS and VDD power supplies.

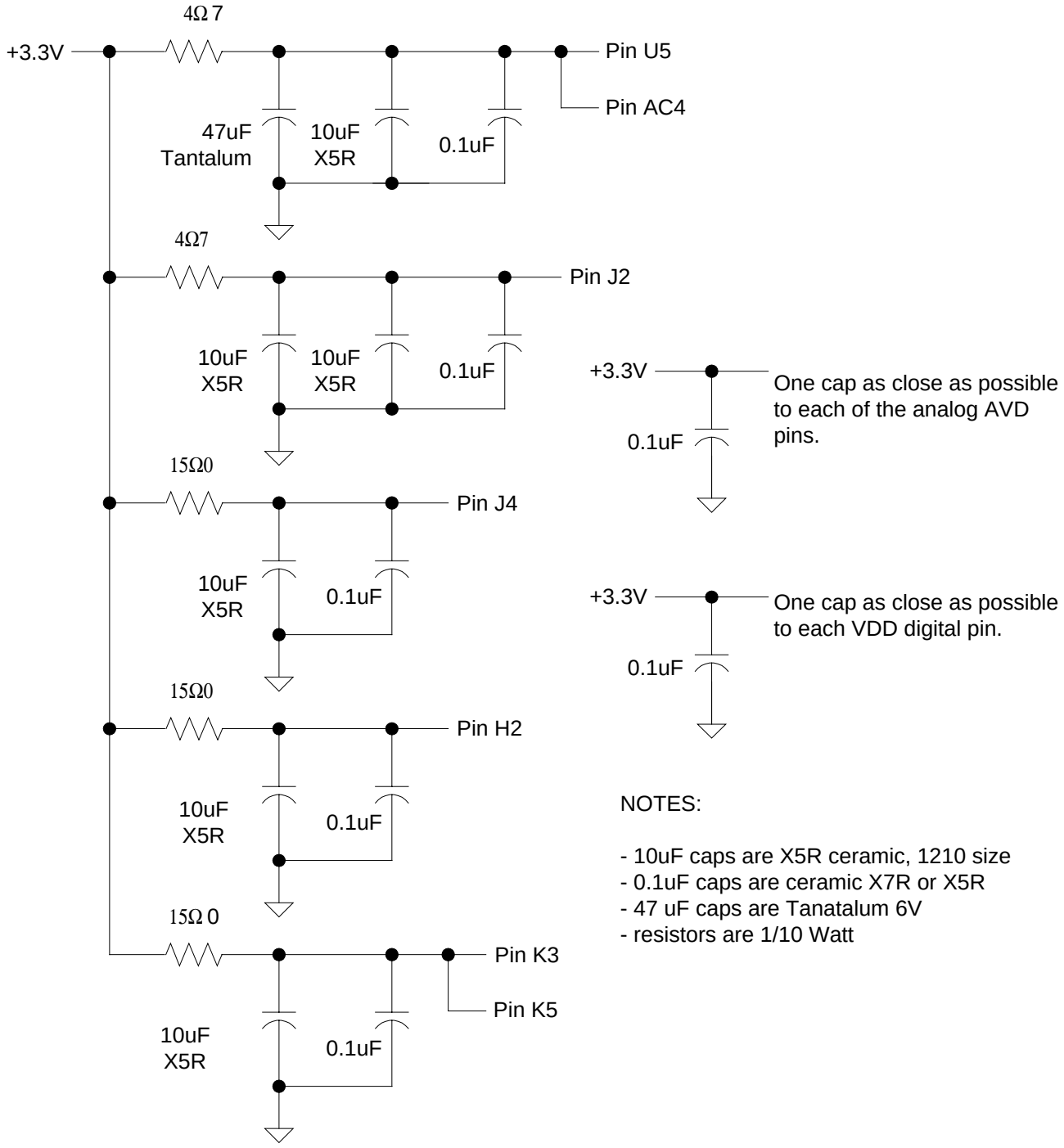
4.) Analog power supplies (AVD but not QAVD) must be either applied simultaneously with every QAVD and VDD, after all QAVD and VDD have been applied, or they must be current limited to the maximum latchup current specification. (100 mA). To prevent forward biasing the ESD protection diode between AVD supplies and QAVD the differential voltage measured between these power supplies must be less than 0.5 volt.

This recommended differential voltage is to include peak to peak noise on the QAVD and AVD power supplies as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by

using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. The relative power sequencing of the multiple AVD power supplies is not important.

5.) Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD / AVD discharge times will not damage the device.

Figure 28 -Analog Power Supply Filtering



NOTES:

- 10uF caps are X5R ceramic, 1210 size
- 0.1uF caps are ceramic X7R or X5R
- 47 uF caps are Tanatalum 6V
- resistors are 1/10 Watt

14.14 Interfacing to ECL or PECL Devices

Only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 29 and

Figure 30 illustrate the recommended configurations for both types of ECL voltage levels. The PECLV pin should be set appropriately for the selected configuration.

Figure 29 -Interfacing SPECTRA-622 PECL Pins to 3.3V Devices

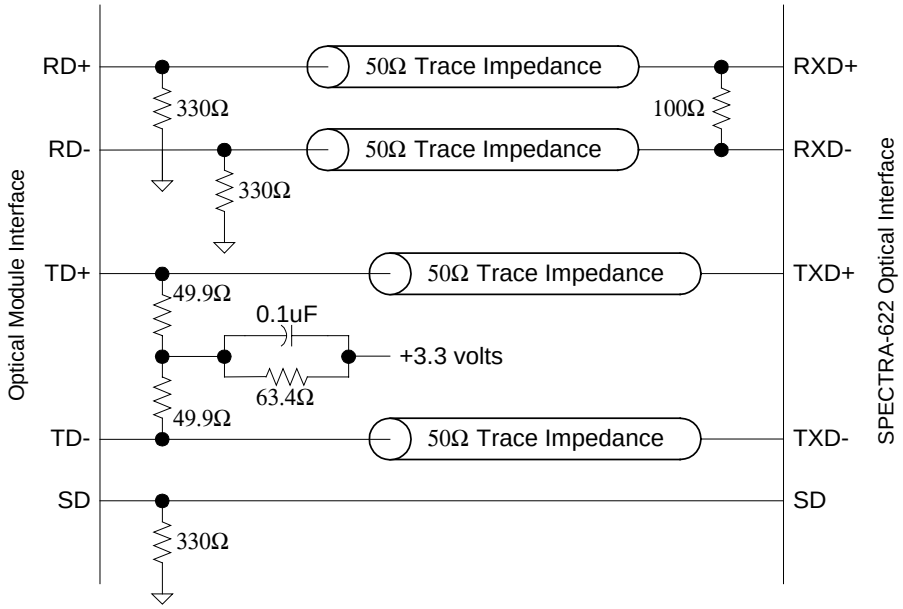
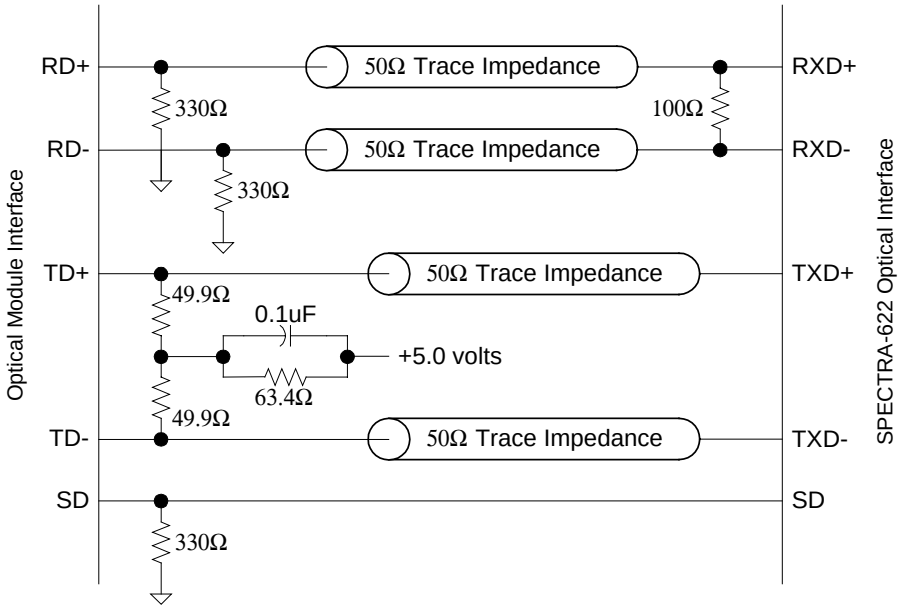


Figure 30 -Interfacing SPECTRA-622 PECL Pins to 5.0V Devices



When a PECL input is not being used, the positive differential input must be tied to analog power (AVD) and the negative differential input must be tied to analog ground (AVS). In all cases, the PECL inputs must be driven with a differential voltage (do not connect both pins to AVD or AVS).

When the PECL output is not being used, the external reference resistor TDREF1 may be tied to analog power (AVD) and TDREF0 may be tied to analog ground (AVS) to disable the PECL output. Both positive and negative differential outputs of the PECL output may be tied to analog ground (AVD).

Each PECL input and output has an associated ESD biasing pin PBIAS[3:0]. These biasing pins should be biased at 3.3 volts or 5.0 volts depending on the configuration used. Each bias pin should be high-frequency decoupled to prevent noise from coupling through the ESD structures and affecting the high-speed signals.

14.15 Clock Recovery

The Clock Synthesizer unit (CSU) in the Spectra-622 requires an external reference clock REFCLK to generate the 622 MHz transmit clock. The REFCLK input is a PECL input in order to reduce the amount of noise coupled into the CSU. In most cases, the reference clock must be generated and propagated using PECL logic in order for the CSU to meet SONET/SDH intrinsic jitter specifications.

In general, the reference clock REFCLK is supplied by a crystal oscillator with PECL outputs. The oscillator must have at least -115dBc/√Hz between 12 kHz and 5 MHz frequency offset in order for the CSU to meet SONET/SDH intrinsic jitter specifications. Do not use a TTL type crystal oscillator with a TTL to PECL converter as the TTL signal conversion will generate significant jitter on the reference clock.

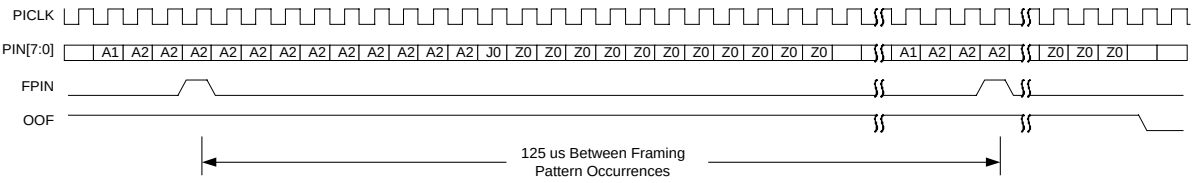
The Clock Recovery unit (CRU) in the Spectra-622 requires a 47nF non-polarized capacitor (ceramic ± 5% X7R or equivalent) between the C0 and C1 pins to control the amount of “peaking” in the jitter transfer curve. The capacitor should be located as close as possible to the C0 and C1 pins in order to prevent noise from coupling into CRU. It must be non-polarized as the capacitor may operate with a D.C. reverse-bias depending on process, voltage and temperature extremes.

15 FUNCTIONAL TIMING

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the SPECTRA-622 registers are set to their default states). It is also assumed that the STS (AU) grooming functions at the ADD and DROP buses using the Time-Slot Interchange feature are disabled.

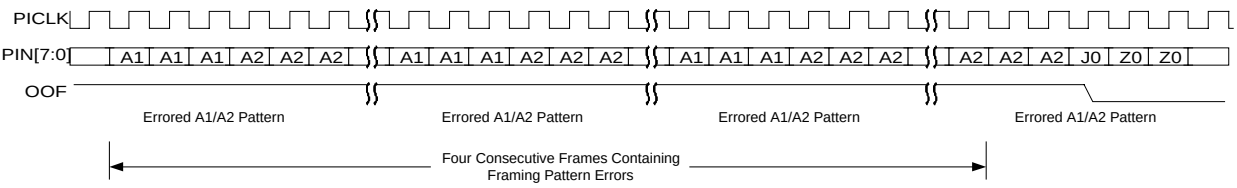
15.1 Parallel Line Interface

Figure 32 -In Frame Declaration Timing



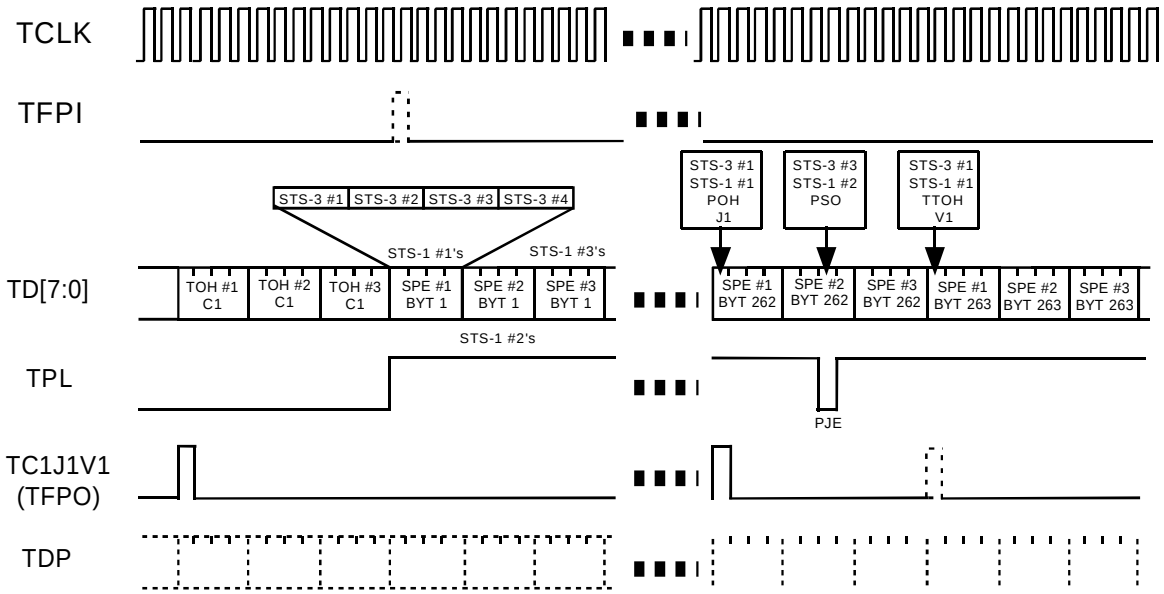
The In Frame Declaration Timing diagram above illustrates the declaration of the in-frame state by the SPECTRA-622 when processing a 77.76 Mbyte/s STS-12 (STM-4) stream on PIN[7:0]. An upstream serial-to-parallel converter indicates the location of the SONET frame using the FPIN input to mark the first SPE byte as illustrated in the timing diagram. The frame verification is initialized by a pulse on FPIN when the SPECTRA-622 is out of frame. The in-frame state is declared if the framing pattern is observed in the correct byte positions in the following frame, and in the intervening period (125 us) no additional pulse were present of FPIN. The SPECTRA-622 ignores pulses of FPIN while in frame. The algorithm results in a maximum average reframe time of 250 us in the absence of mimic framing patterns.

Figure 33 -Out of Frame Declaration Timing



The Out of Frame Declaration Timing diagram above illustrates the declaration of out of frame for an STS-12 (STM-4) stream using the parallel interface. The framing pattern is a 196-bit pattern that repeats once per frame. For the purposes of OOF declaration, the framing pattern may be modified using the ALGO2 bit in the RSOP Control register. Out of frame is declared when one or more errors are detected in this pattern for four consecutive frames as illustrated. In the presence of random data, out of frame will normally be declared within 500 us.

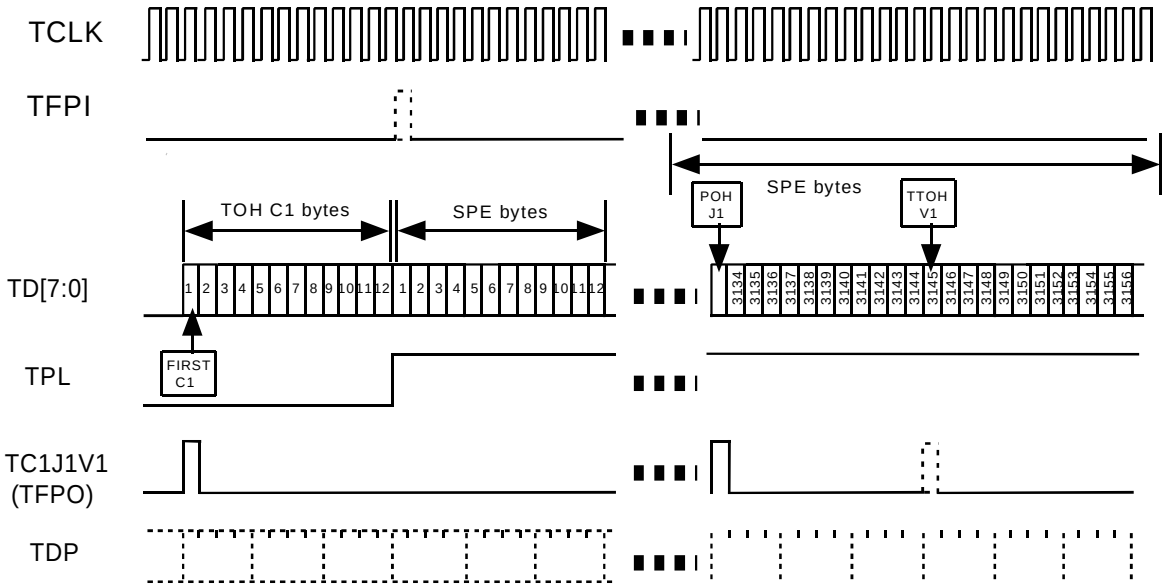
Figure 34 -STS-12 (STM-4/AU3) Transmit Telecom Bus Timing



The figure above shows the STS-12 (STM-4/AU3) Transmit Telecom bus timing. TCLK is a nominally 77.76 MHz clock. The frame pulse TFPI marks the first synchronous payload envelope byte in the STS-12 (STM-4/AU3) frame on TD[7:0]. This is also the first SPE byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream. It is not necessary for TFPI to be present at every frame. An internal counter fly-wheels based on the most recent TFPI received. Transport overhead and payload bytes are distinguished by the TPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #2. A stuff byte is place in the positive stuff opportunity byte position and TPL is set low to indicate that data is not available. The Transmit bus composite timing signal TC1J1V1 is set high when TPL is set low to mark the first C1 byte of the STS-12 (STM-4/AU3) frame. TC1J1V1 is set high when TPL is also set high to mark the J1 byte in each of the STS-1 (STM-0/AU3) streams. Optionally, TC1J1V1 is set high once every multiframe to mark the first frame of the Transmit bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport

frame and the synchronous payload envelope of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The Transmit bus parity output TDP reports the parity of TD[7:0] and optionally includes TPL and TC1J1V1.

Figure 35 -STS-12c (STM-4-4c) Transmit Telecom Bus Timing



The figure above shows the STS-12c (STM-4-4c) Transmit Telecom bus timing. TCLK is a nominally 77.76 MHz clock. In parallel mode, the frame pulse TFPI marks the first synchronous payload envelope byte on TD[7:0]. In serial mode, TFPI comes out about 10 ns to 25 ns before the first synchronous payload envelope byte. It is not necessary for TFPI to be present at every frame. An internal counter fly-wheels based on the most recent TFPI received. Transport overhead and payload bytes are distinguished by the TPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The Transmit bus composite timing signal TC1J1V1 is set high when TPL is set low to mark the first C1 byte. TC1J1V1 is set high when TPL is also set high to mark the J1 byte of the STS-12c (STM-4-4c) stream. Optionally, TC1J1V1 is set high once every multiframe to mark the “V1 byte” in the first frame of the Transmit bus tributary multiframe. The “V1 byte” corresponds to the 12-th byte after J1. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The Transmit bus parity output TDP reports the parity of TD[7:0] and optionally includes TPL and TC1J1V1.

15.2 Receive Transport Overhead Extraction

15.2.1 Receive Transport Overhead (RTOH) Functional Timing

Figure 36 -Receive Tranport Overhead Extraction

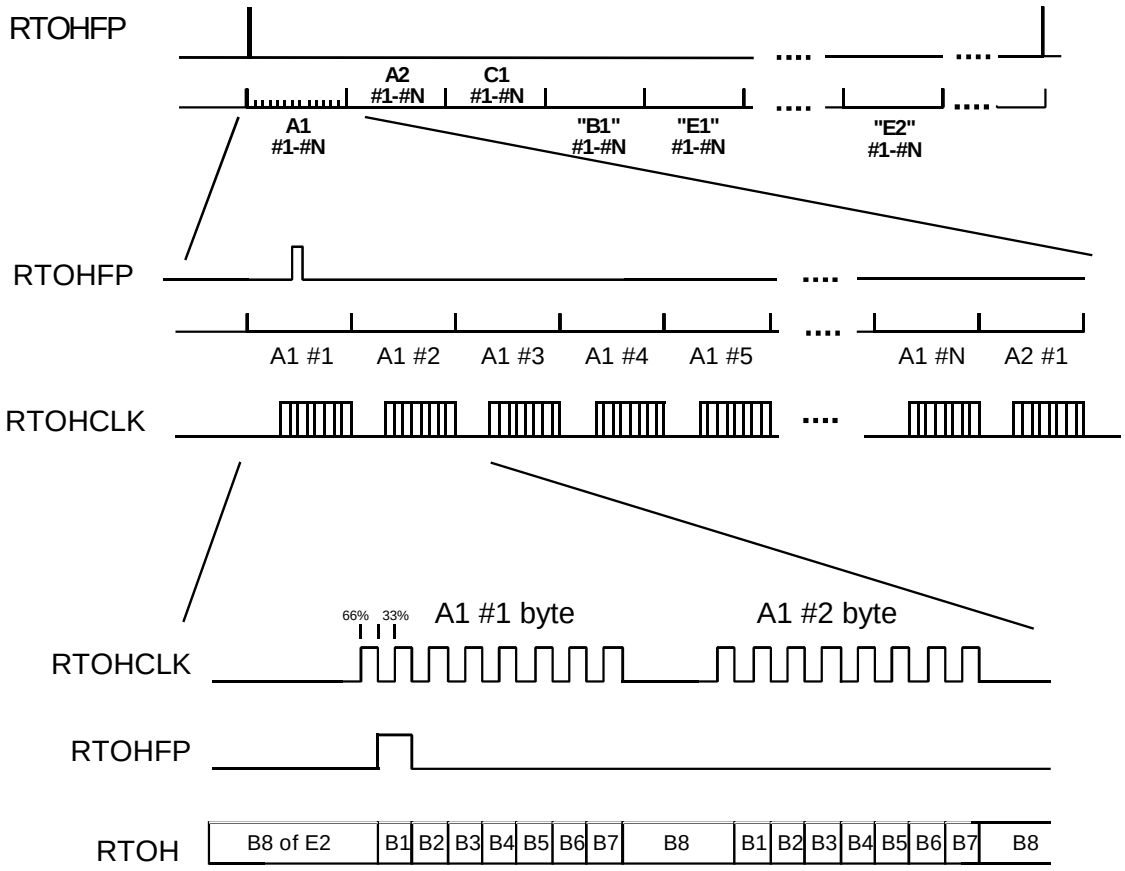


Figure 36 shows the Receive Transport Overhead (RTOH) output timing. RTOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz, 33% high duty cycle clock. 2592 bits (27x12 bytes) will be output on RTOH between the rising edges of RTOHFP. RTOHCLK will have a 33% high duty cycle and RTOHFP will be set high to identify the MSB (bit 1) of the STS-1 #1 A1 byte. The RTOHCLK begins bursting out data during RTOHFP high. The Overhead bytes of the each row are bursted out followed by a prolonged gapped period in the clock. The clock begins bursting out data once again when the next row's overhead has been received. In between each overhead byte, the clock gaps for one cycle.

RTOHCLK should be used to sample the RTOH and RTOHFP output signals. All outputs are aligned with the falling edge of RTOHCLK and should be sampled on the rising edge of RTOHCLK.

15.2.2 Receive Section and Line DCC Functional Timing

Figure 37 -RX Section/Line and Line DCC Timing (RX_GAPSEL=0)

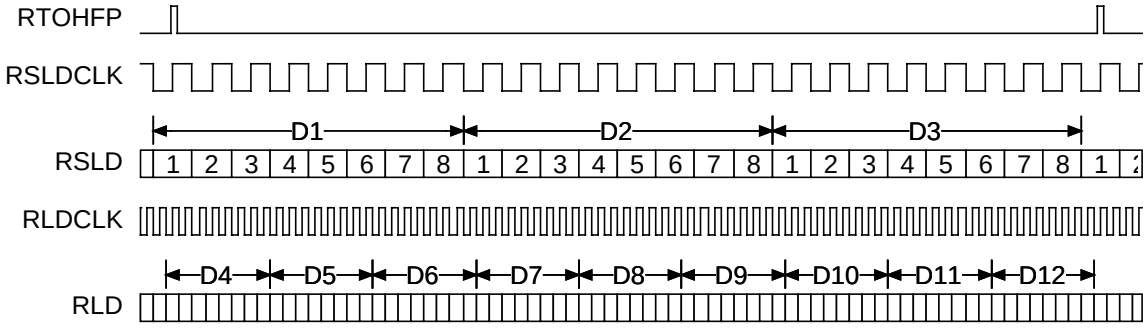
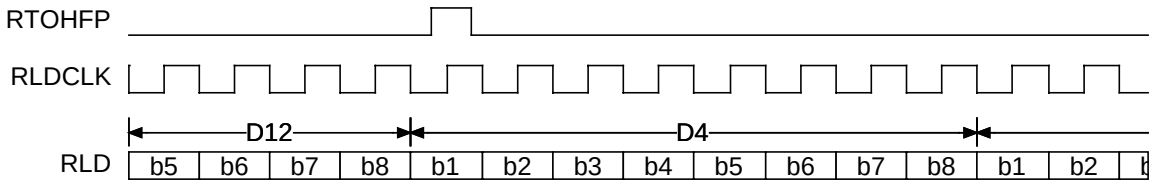


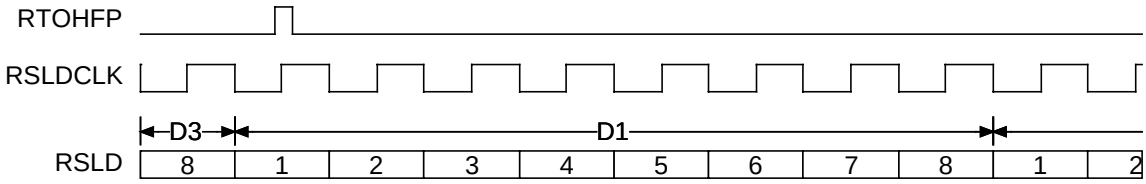
Figure 37 shows the receive section/line and line DCC output timings when RX_GAPSEL=0. The Section/Line (RSLD and RSLDCLK) functional timing is shown for the case where RSLD is carrying the section DCC bytes (D1-D3). In the case when carrying the line DCC bytes (D4-D12), the RSLD and RSLDCLK functional timing will be identical to that of RLD and RLDCLK. Both RLD and RSLD may be forced to output all ones. Enabling the LOS/LOF/LAIS or TIM alarms via the associated LINE_AISEN(2:0) or SECT_AISEN[2:0] register bits will force the RLD and RSLD outputs all ones when the alarms are asserted.

Figure 38 -RX Line DCC Timing (RX_GAPSEL=0)



The line data output (RLD) is aligned with the falling edge of the RLDCLK. The rising edge of RLDCLK should be used to sample the RLD data and RTOHFP. Sampling RTOHFP high identifies the MSB of the D4 byte available on the RSLD output. RLDCLK is a 576 kHz clock.

Figure 39 -RX Section DCC Timing (RX_GAPSEL=0)



The section/line data output (RSLD) is aligned with the falling edge of the RSLDCLK. The rising edge of RSLDCLK should be used to sample the RSLD data and RTOHFP. Sampling RTOHFP high identifies the MSB of the D1 or D4 byte available on the RLD output. When carrying the line DCC, RSLDCLK is a 576 kHz clock (see line DCCFigure Figure 39) and when carrying the section DCC, RSLDCLK is a 192 kHz clock (see section DCCFigure Figure 40).

Figure 40 -RX Section/Line and Line DCC Timing (RX_GAPSEL=1)

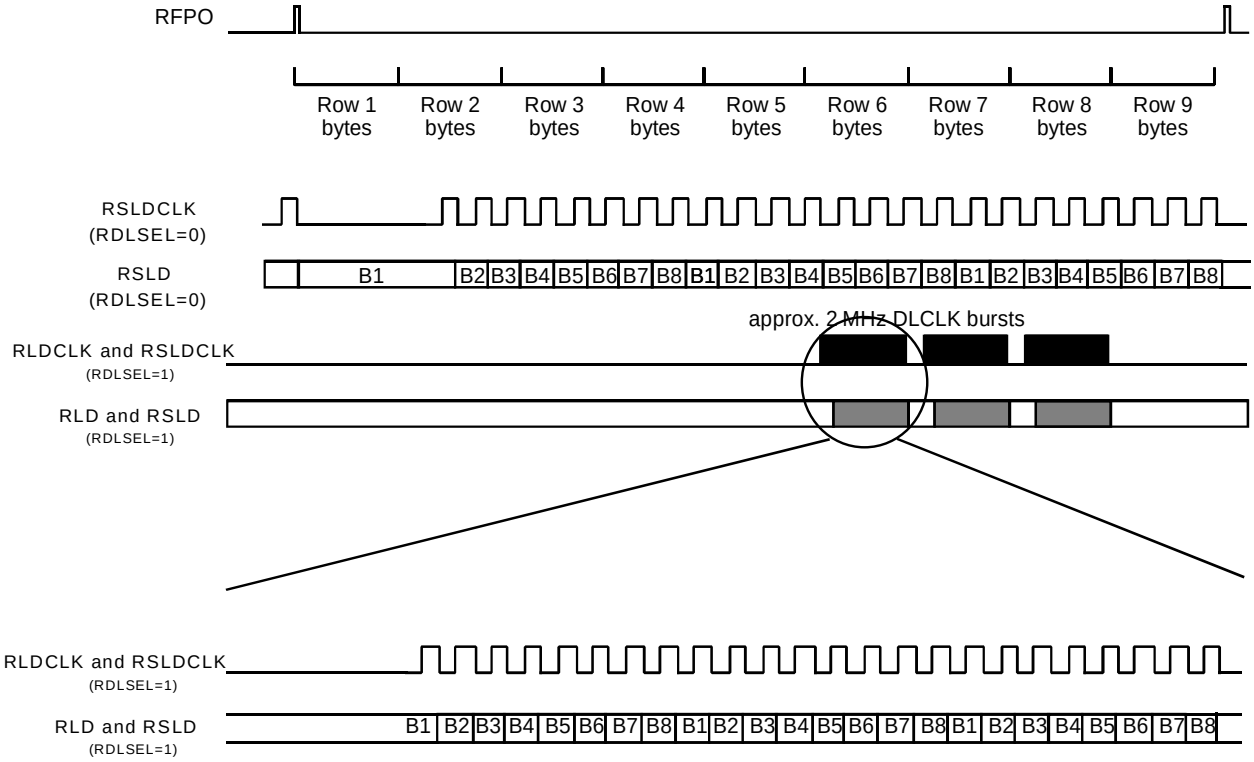


Figure 39 shows the receive section/line and line DCC output timings when RX_GAPSEL=1. The timing diagram shows the relationship between the RSLD/RLD serial data outputs and their associated clocks, RSLDCLK/RLDCLK when RX_GAPSEL=1. When register bit RSLDSEL is low, the section DCC (D1-D3) bytes are shifted out on the RSLD output. The RSLDCLK is a 216 KHz, 50% duty cycle clock gapped to produce a 192 KHz nominal rate. When register bit RSLDSEL is high, the line DCC (D4-D12) bytes are shifted out on the RSLD output. The RSLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate.. RSLD is always updated on the falling RSLDCLK edge.

The receive line DCC clock and data alignment timing diagram above shows the relationship between the RLD serial data output and its associated clock, RLDCLK. The line DCC, D4-D12, bytes are shifted out on the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock. RLD is updated on the falling RLDCLK edge. The RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate and RLD is used to shift out the line DCC (D4-D12) bytes. RLD is updated on the falling RSLDCLK edge.

A clock gap detector using a higher speed clock may be used. to identify the alignment of the RSLD and RLD data. The RFPO output may be used as an asynchronous reset. No specific timing relation between RFPO and the clock signals are implied by this diagram except to say that the RFPO pulse will occur during the gap.

15.2.3 Receive Order Wire and User Channel Functional Output Timing

Figure 41 -RX Order wire and User Channel Timing (RX_GAPSEL=0)

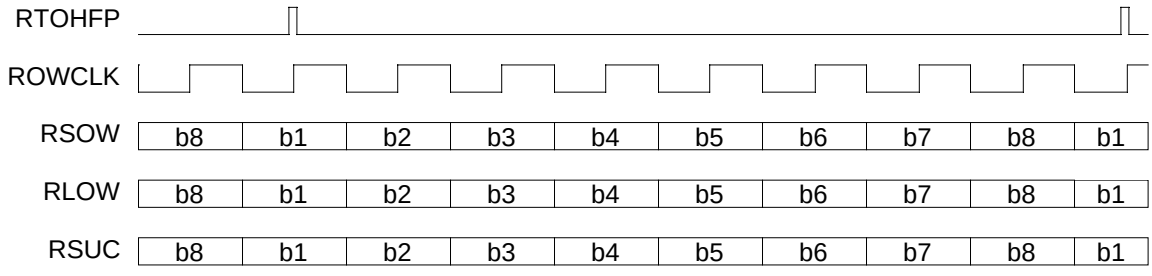


Figure 41 and Figure 42 shows the order wire and user channel output timings when RX_GAPSEL=0. The data outputs (RSOW, RLOW, RSUC) are aligned with the falling edge of the ROWCLK. The rising edge of ROWCLK should be used to

sample the data and RTOHFP. Sampling RTOHFP high identifies the MSB of the E1, E2, F1 bytes available on the RSOW, RLOW and RSUC outputs. ROWCLK is a 64 kHz clock.

Figure 42 -RSOW, RLOW and RSUC Alignment w.r.t. RTOHFP (RX_GAPSEL=0)

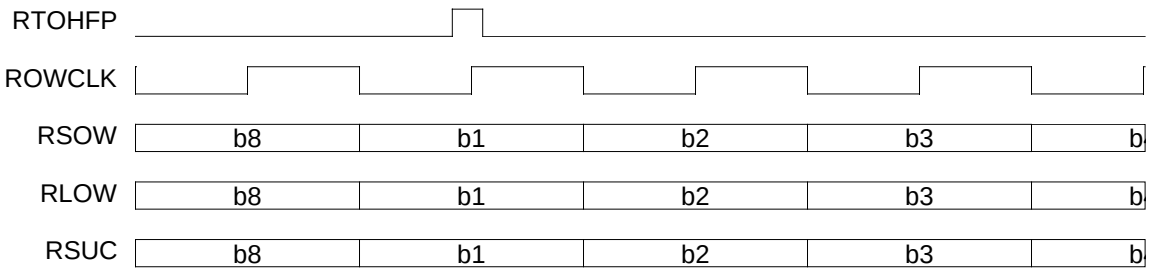


Figure 43 -RX Order wire and User Channel Timing (RX_GAPSEL=1)

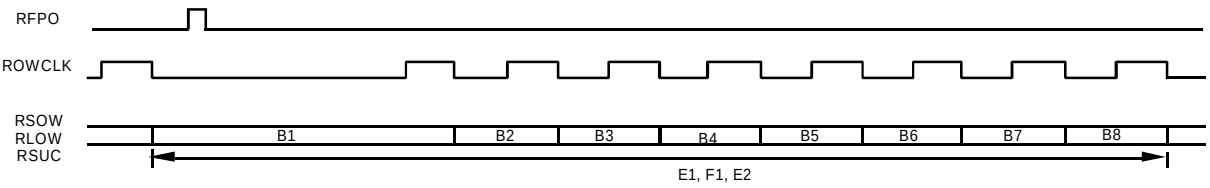


Figure 43 shows the order wire and user channel output timings when RX_GAPSEL=1. The data outputs (RSOW, RLOW, RSUC) are aligned with the falling edge of the ROWCLK. The rising edge of ROWCLK should be used to sample the data. ROWCLK is a 72 kHz, 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate clock.

A clock gap detector using a higher speed clock may be used. to identify the alignment of RSOW, RSUC and RLOW. The RFPO output may also be used as an asynchronous reset. No specific timing relation between RFPO and the clock signal are implied by this diagram except to say that the RFPO pulse will occur during the gap.

15.2.4 Receive Overhead (ROH) Functional Output Timings

Figure 44 -Receive Overhead Output Functional Timing (RX_GAPSEL=0)

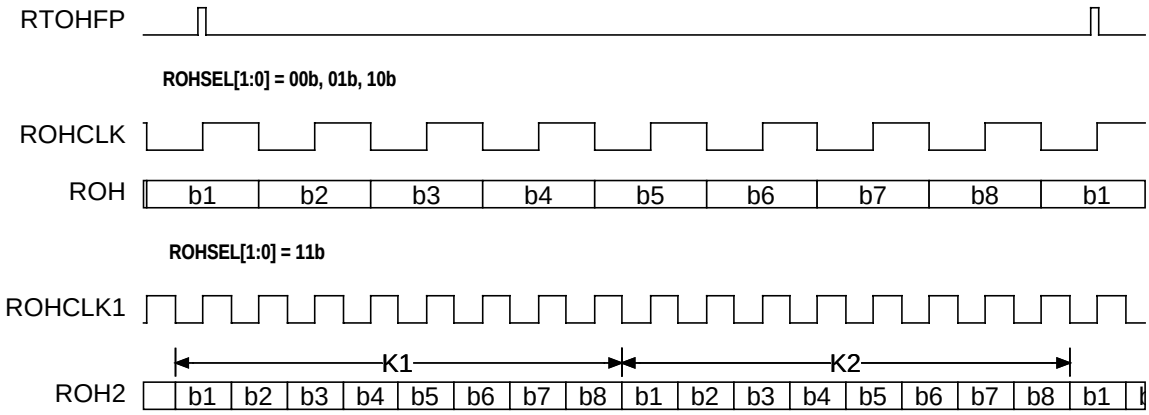


Figure 44 shows the receive overhead output functional timing when RX_GAPSEL=0. The data output (ROH) is aligned with the falling edge of the ROHCLK. Depending on the selected output mode via the ROHSEL[1:0] register bits, ROH will carry the 8 bit section or line or user channel bytes or the 16 bit K1/K2 APS bytes. The rising edge of ROHCLK should be used to sample the ROH data and RTOHFP. Sampling RTOHFP high identifies the MSB of the E1 or E2 or F1 byte or MSB of the K1 byte available on the ROH output. When outputting the order wire or user channel, ROHCLK is a 64 kHz clock. When outputting the APS bytes, ROHCLK is a 128 kHz clock.

Figure 45 -Receive Overhead Output Functional Timing (RX_GAPSEL=1)

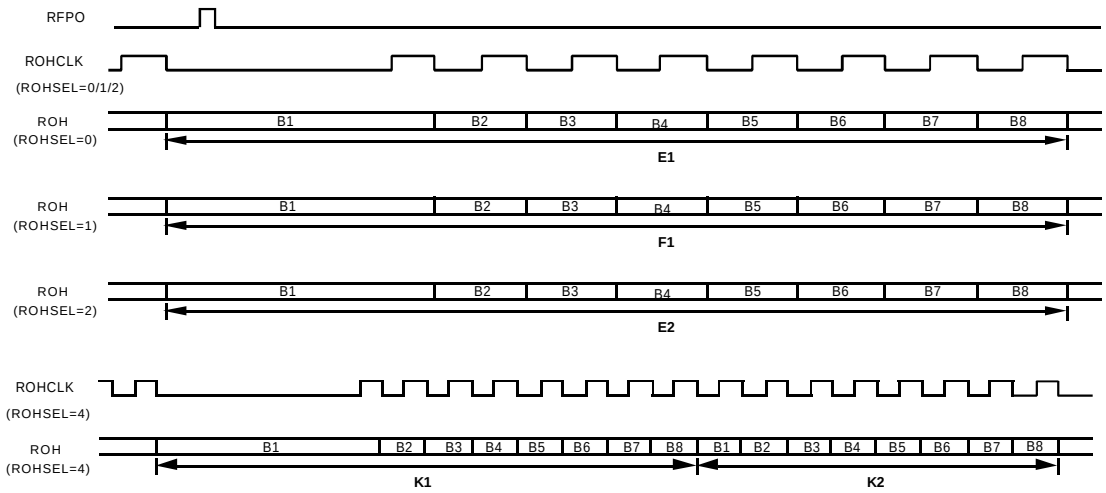


Figure 45 shows the receive overhead output functional timing when RX_GAPSEL=1. For ROHSEL={0,1,2}, ROHCLK will be a is a 72 kHz, 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate clock. The E1, F1 and E2 bytes may be selectively shifted out on the ROH.

For ROHSEL={3}, the ROHCLK will be a 144 KHz 50% duty cycle clock gapped to produce a 128 KHz nominal rate. The K1 and K2 bytes are shifted out on the ROH in the order as illustrated. All output data is updated on the falling edge of ROHCLK.

A clock gap detector using a higher speed clock may be used. to identify the alignment of ROH. The RFPO output may also be used as an asynchronous reset. No specific timing relation between RFPO and the clock signal are implied by this diagram except to say that the RFPO pulse will occur during the gap.

15.3 Transmit Transport Overhead Insertion

15.3.1 Transmit Transport Overhead (TTOH) Functional Timing

Figure 46 -Transmit Transport Overhead Insertion

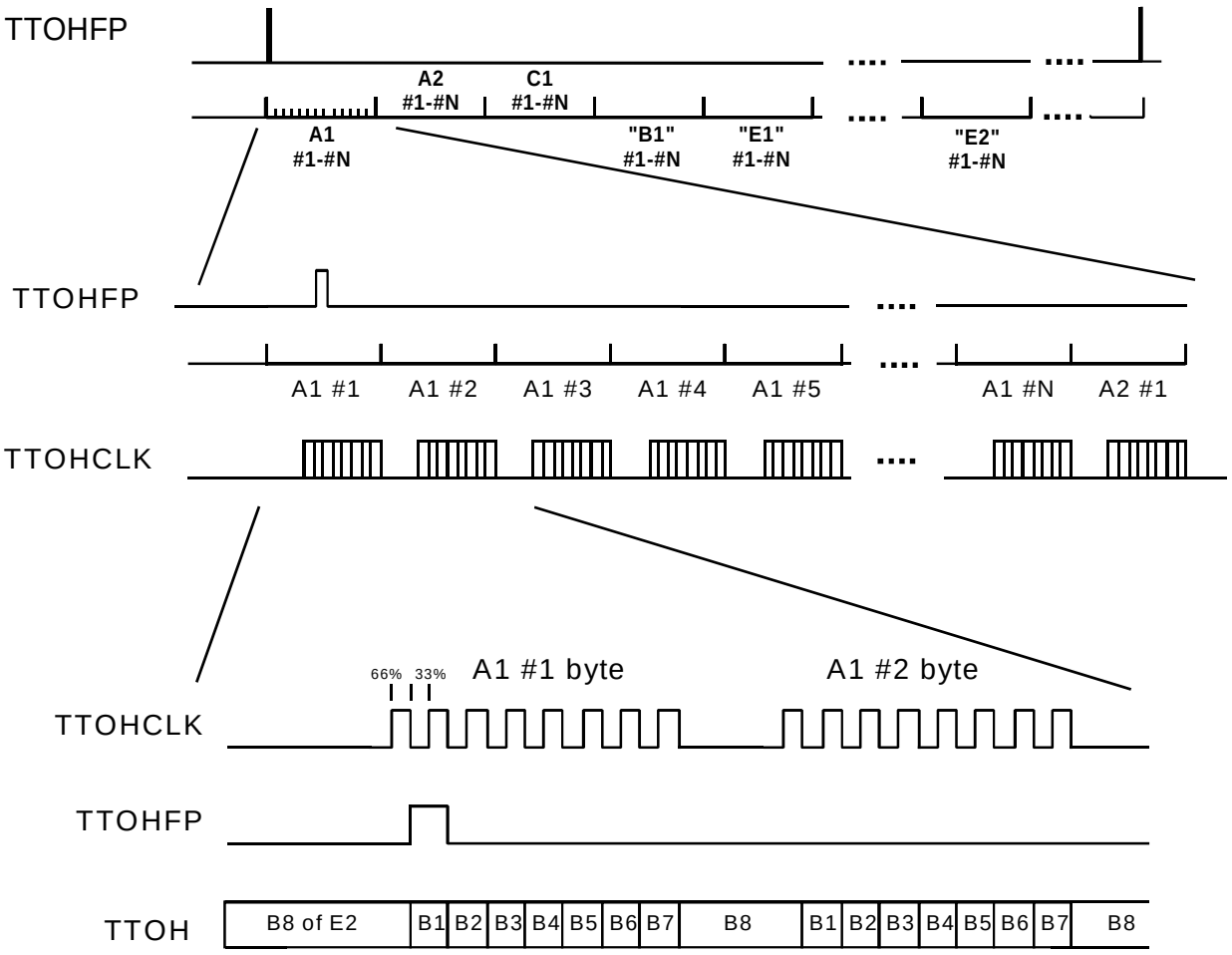


Figure 46 shows all the TTOH port signal functional timings. The TTOH ports (TTOH, TTOHCLK, TTOHFP and TTOHEN) are used to supply the SONET/SDH transport overhead bytes. The serial TTOH data stream supplies the 324 transport overhead bytes (108 section overhead and 216 line overhead bytes) in 125 us. The TTOHCLK output provides timing for the TTOH and TTOHEN inputs. TTOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock.

The TTOHCLK generates a burst of clock cycles after the TTOHFP. This burst is used to receive all overhead bytes needed for insertion into the 36 overhead bytes. The TTOHFP output is updated on the falling edge of TTOHCLK and is used to identify the positioning of the 1st A1 byte (STS-1 #1) most significant bit

on TTOH. External logic supplying the TTOH and TTOHEN must use the TTOHFP to locate when the MSB of the A1#1 byte should be present on TTOH.

The TTOC samples the TTOH and TTOHEN inputs on the rising edge of TTOHCLK. TTOHEN high during bit 1 of TOH byte on TTOH, validates the byte to be inserted into either the LPIN or PPIN data stream. In the second half of Figure 46, the first A1 byte will be inserted into the transmit stream since the TTOHEN is sampled high at the same time that bit 1 is sampled. The second A1 byte will not be inserted since the TTOHEN was not sampled high at the same time as bit 1of the second A1 byte.

An error insertion feature is provided for the H1, H2, B1, and B2 byte positions. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the transmit stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

Figure 46 also shows the functional timing for the TTOHREI input. The REI accumulator counts the number of high cycles on TTOHREI. The accumulated count is transferred to the holding register on the sampling of TTOHFP high. The sampling of TTOHFP high also resets the holding accumulation counter to zero or one, depending if the TTOHREI is sample high or low. The transferred count is then inserted into the M1 byte of the transmit data stream when the REI_EN register bit in the TTOC Control Register is set to is set to logic one.

15.3.2 Transmit Section and Line DCC Functional Timing

Figure 47 -TX Section/Line and Line DCC Timing (TX_GAPSEL=0)

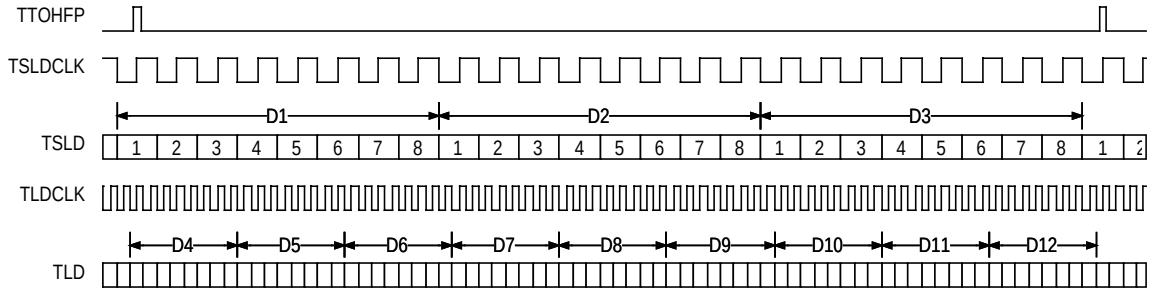


Figure 48 -TX Line DCC Output Timing (TX_GAPSEL=0)

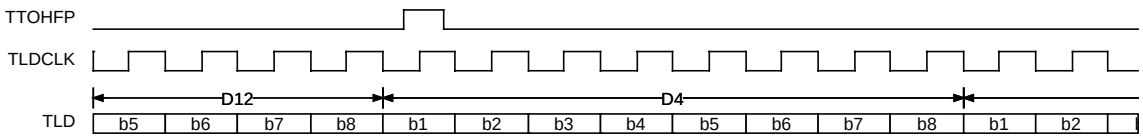


Figure 49 -TX Section DCC Output Timing (TX_GAPSEL=0)

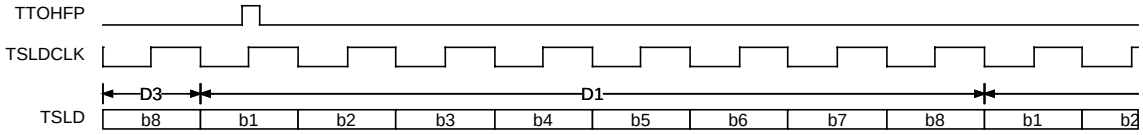


Figure 47, Figure 48 and Figure 49 show the functional timing for the section and line DCC ports when TX_GAPSEL=0. The TTOC block generates output clocks TSLDCLK and TLDCLK. TSLDCLK is programmable (TSLD_SEL) to provide timing for the section or line DCC over the TSLD serial input. When TSLD_SEL is a logic low, the TSLD serial input is set to carry the section DCC (D1 to D3) bytes. In this case TSLDCLK is a 192 kHz clock. When TSLD_SEL is a logic high, the TSLD serial input is set to carry the line DCC (D4 to D12) bytes. In this case TSLDCLK is a 576 kHz clock. The TSLD serial input is sampled on the rising edge of TSLDCLK. When TSLD_SEL register bit is programmed low and TSLD is used to carry the line DCC bytes, the section DCC bytes can be force to all ones or all zeros via the TSDVAL register bit. TTOH and TTOHEN has precedence over TSDVAL.

TLDCLK provides timing for the line DCC over the TLD serial input. The TLD serial input is carries the line DCC (D4 to D12) bytes and TLDCLK is a 576 kHz clock. The TLD serial input is sampled on the rising edge of TLDCLK.

The TTOHFP output is updated on the falling edge of TTOHCLK but the TSLDCLK and TLDCLK clocks are generated such that the rising edge of both clocks are able to sample the TTOHFP.Figure 48 and Figure 49 show this relation. TTOHFP is used to identify the positioning of the D1 or D4 bit 1 (MSB) on TSLD and TLD respectively. External logic supplying the TSLD and TLD must use the TTOHFP to locate when the MSB of D1 and D4 should be present on TSLD and TLD.

Figure 50 -TX Section/Line and Line DCC Timing (TX_GAPSEL=1)

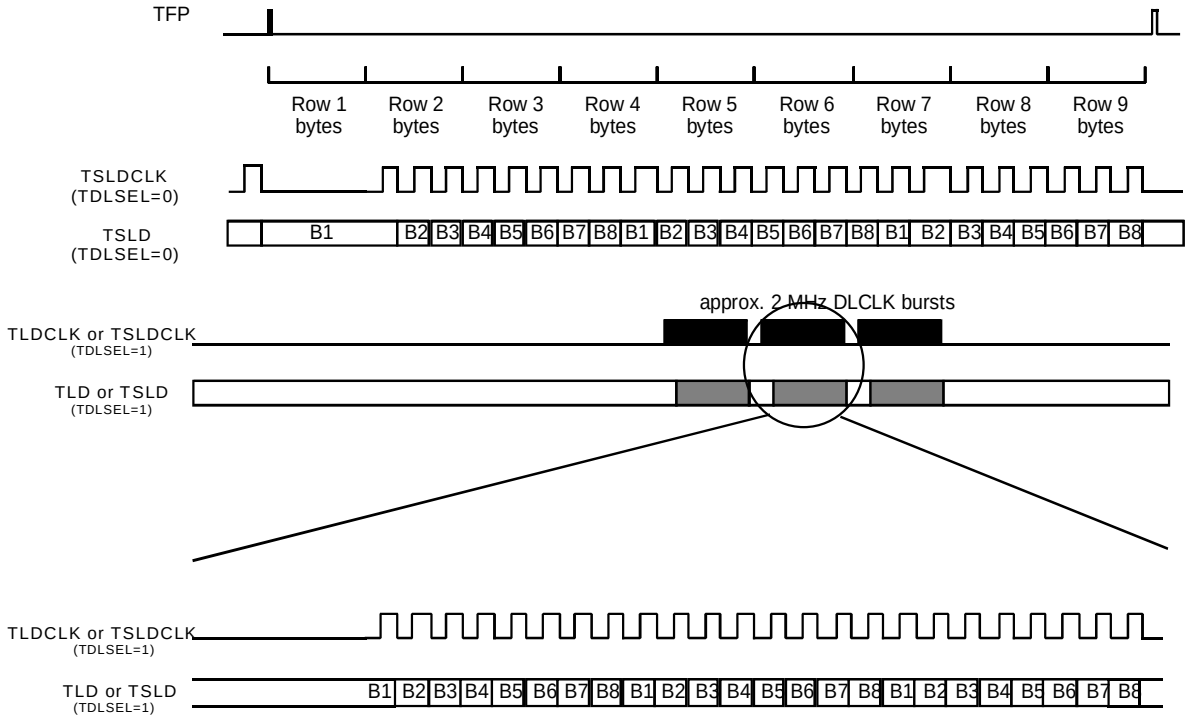


Figure 50 shows the timing relationship between the TSLD/TLD serial data inputs and their associated clocks, TSLDCLK/TLDCLK. When register bit TSLD_SEL is set low, TSLDCLK is a 216 KHz, 50% duty cycle clock gapped to produce a 192 KHz nominal rate that is aligned with TFP as shown in the timing diagram. The section DCC bytes, D1-D3 are sourced from the TSLD input. When register bit TSLD_SEL is set high, TSLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate. The line DCC bytes, D4-D12 are sourced from the TSLD input. All input data on TSLD is sampled on the rising edge of TSLDCLK.

Figure 50 also shows the transmit line DCC timing. The line DCC, D4-D12, bytes are shifted out on the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock. RLD is updated on the falling RLDCLK edge. The RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate and RLD is used to shift out the line DCC (D4-D12) bytes. RLD is updated on the falling RLDCLK edge.

A clock gap detector using a higher speed clock may be used. to identify the alignment of the TSLD and TLD data. The TFP output may be used as an asynchronous reset. No specific timing relation between TFP and the clock

signals are implied by this diagram except to say that the TFP pulse will occur during the gap.

15.3.3 Transmit Order Wire and User Channel Functional Timing

Figure 51 -Transmit Order Wire and User Channel Timing (TX_GAPSEL=0)

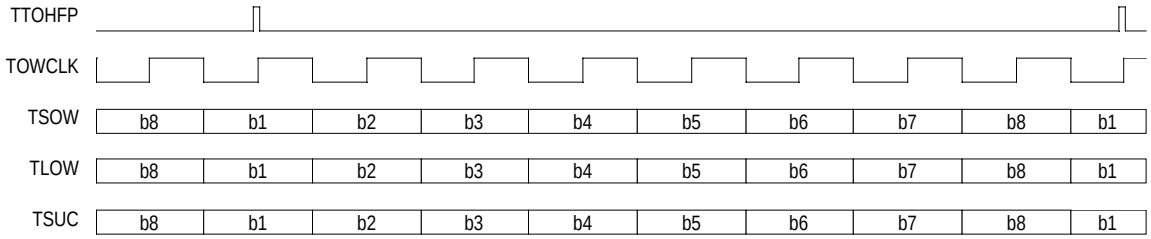


Figure 52 -TSOW, TLOW and TSUC Alignment w.r.t TTOHFP (TX_GAPSEL=0)

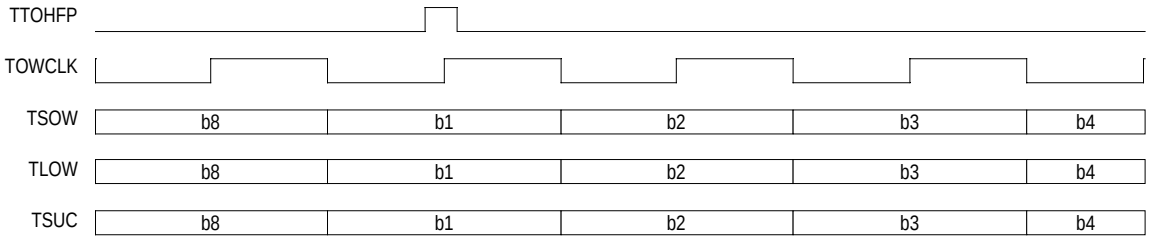


Figure 51 and Figure 52 shows the functional timing for the orderwire and user channel ports. The TTOC block generates an output clock TOWCLK that provides timing for the section orderwire (E1), section user channel (F1) and line orderwire (E2) bytes over the TSOW, TSUC and TLOW serial inputs respectively. TOWCLK is a 64 kHz clock and is used to sample the TSOW, TSUC and TLOW serial inputs on the rising edge.

The TTOHFP output is updated on the falling edge of TTOHCLK but the TOWCLK clock is generated such that the rising edge is able to sample the TTOHFP. Figure 52 show this relation. TTOHFP is used to identify the positioning of the E1, F1 and E2 bit 1 (MSB) on TSOW, TSUC and TLOW respectively.

External logic supplying the these inputs must use the TTOHFP to locate when the MSB of the bytes should be present on TSOW, TSUC and TLOW.

Figure 53 -Transmit Order Wire and User Channel Timing (TX_GAPSEL=1)

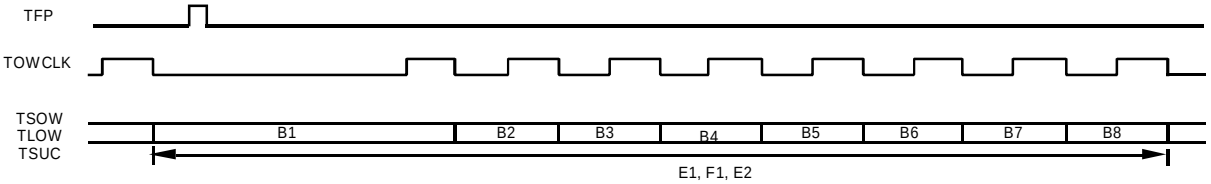


Figure 53 shows the transmit order wire and user channel timings when TX_GAPSEL=1. The data inputs (TSOW, TLOW, TSUC) are sampled on the rising edge of the TOWCLK. TOWCLK is a 72 kHz, 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate clock.

A clock gap detector using a higher speed clock may be used. to identify the alignment of TSOW, TSUC and TLOW. The TFP output may also be used as an asynchronous reset. No specific timing relation between TFP and the clock signal are implied by this diagram except to say that the TFP pulse will occur during the gap.

15.3.4 Transmit Overhead (TOH) Functional Timing

Figure 54 -Transmit Overhead Functional Timing (TX_GAPSEL=0)

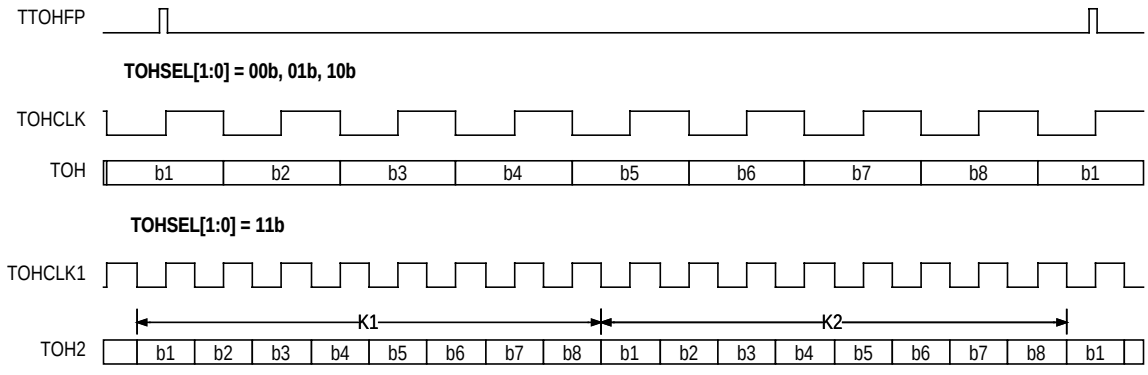


Figure 54 shows the functional timing for the transmit overhead ports when TX_GAP_SEL=0. The TTOC block generates the output clock TOHCLK. TOHCLK is programmable (TOH_SEL[1:0]) to provide timing for the section orderwire, section user channel, line orderwire or APS bytes over the TOH serial input. When TOH_SEL is programmed to select the orderwires or user channel

(TOH_SEL=00,01,10), the TOH serial input is set to carry the section orderwire (E1), section user channel (F1) or line orderwire (E2) bytes respectively. In this case TOHCLK is a 64 kHz clock. When TOH_SEL is programmed to select the line APS (K1/K2) (TOH_SEL=11), the TOH serial input is set to carry K1 and K2 bytes. In this case TOHCLK is a 128 kHz clock. The TOH serial input is sampled on the rising edge of TOHCLK.

The TTOHFP output is updated on the falling edge of TTOHCLK but the TOHCLK clock is generated such that the rising edge of the clock is able to sample the TTOHFP. TTOHFP is used to identify the positioning of the E1, F1, E2 or K1 bit 1 (MSB) on TOH. External logic supplying the TOH input must use the TTOHFP to locate when the MSB of E1, F1, E2 or K1 bytes should be present on TOH.

Figure 55 -Transmit Overhead Functional Timing (TX_GAPSEL=1)

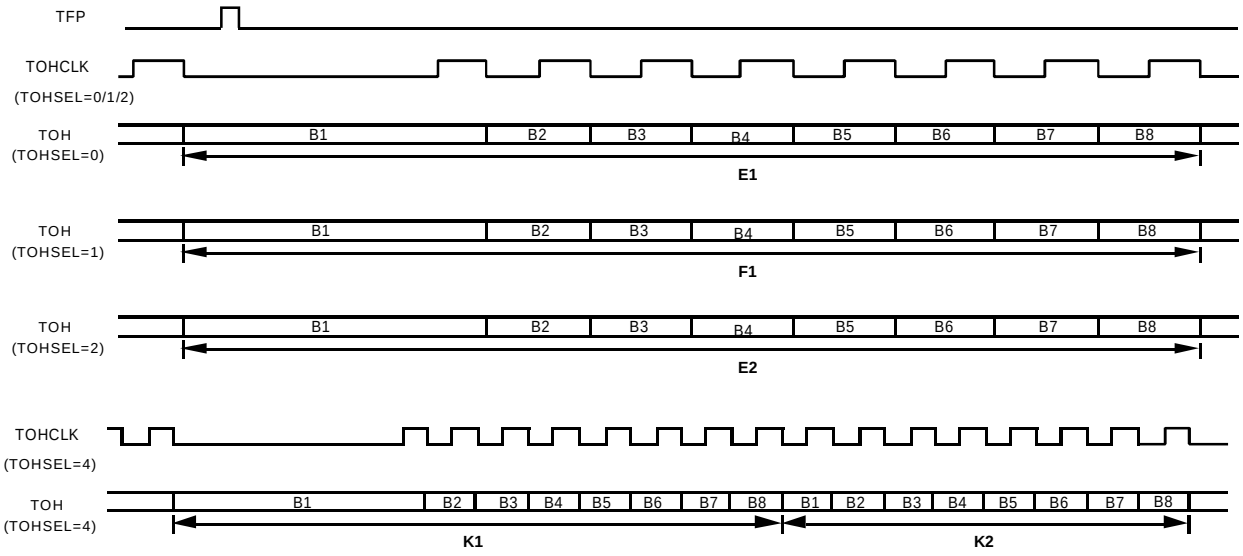


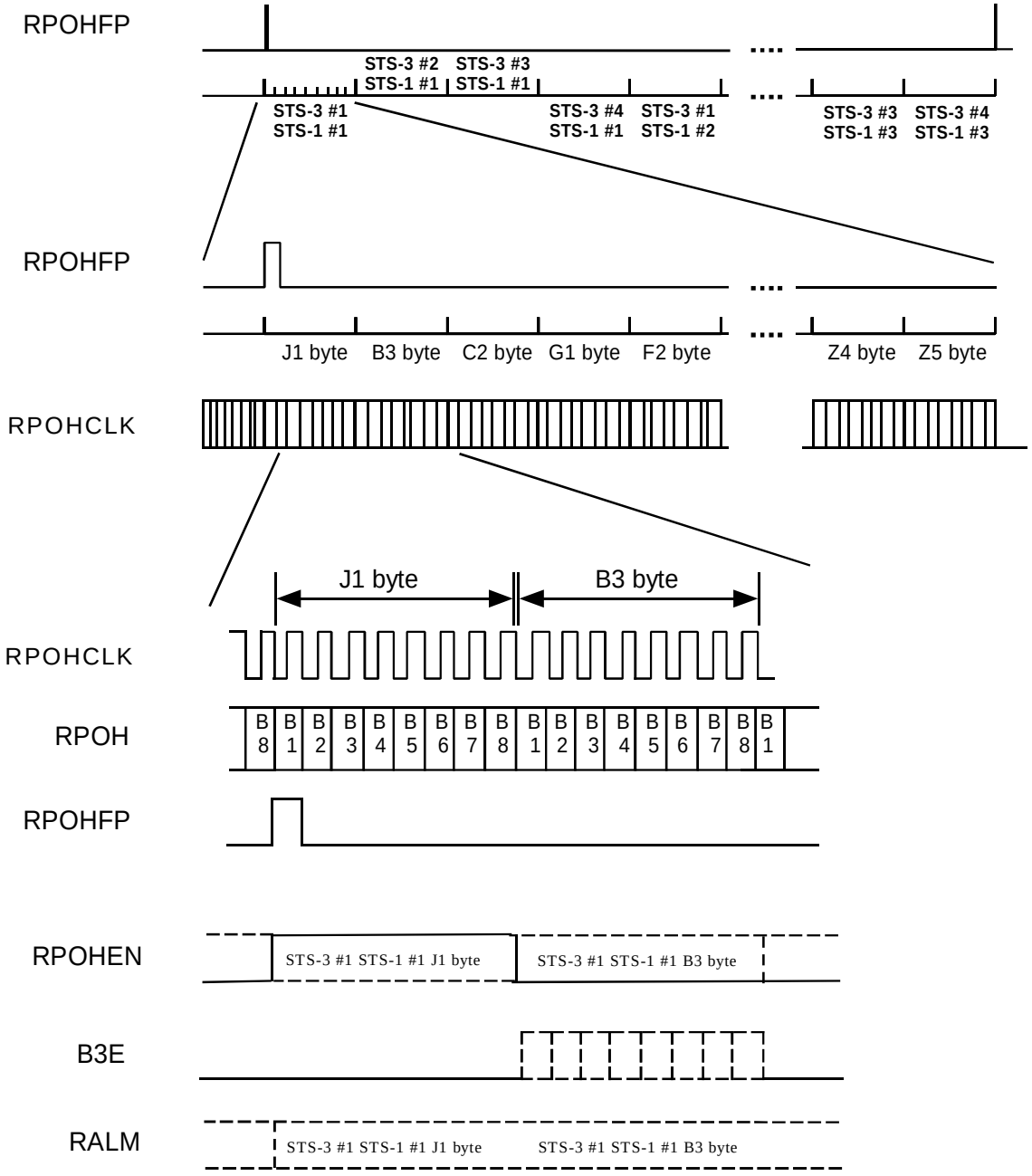
Figure 55 shows the transmit overhead output functional timing when TX_GAPSEL=1. For TOHSEL={0,1,2}, TOHCLK will be a is a 72 kHz, 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate clock. The E1, F1 and E2 bytes may be selectively shifted in on the TOH. The corresponding stream on the TSOW, TSUC or TLOW input is ignored.

For TOHSEL={3}, the TOHCLK will be a 144 KHz 50% duty cycle clock gapped to produce a 128 KHz nominal rate. The K1 and K2 bytes are shifted in on the TOH in the order as illustrated. All input data is sampled on the rising edge of ROHCLK.

A clock gap detector using a higher speed clock may be used. to identify the alignment of ROH. The RFPO output may also be used as an asynchronous reset. No specific timing relation between RFPO and the clock signal are implied by this diagram except to say that the RFPO pulse will occur during the gap.

15.4 Path Overhead Extraction and Insertion

Figure 56 - Receive Path Overhead Extraction/Alarm Timing



The figure above shows the receive path overhead extraction to a serial stream. RPOHCLK is a nominally 12.96 MHz clock and is substantially faster than the

actual arrival rate of the receive path overhead bytes. This allows the use of over-sampling to multiplex the path overhead data streams from the RPOP's onto a single RPOH output. The entire path overhead (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5 bytes) of each STS-1 (STM-0/AU3) in an STS-12 (STM-4/AU3) receive stream can be extracted, serialized and placed on RPOH over one or two RPOH frame periods. For each byte, the most significant bit (msb) is transmitted first. RPOHFP marks the most significant bit of the first J1 byte of the STS-12 (STM-4/AU3). This corresponds to the msb of the J1 byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream. The RPOHEN indicates the validity of the path overhead bytes extracted to the RPOH. If a new path overhead byte of a particular STS-1 (STM-0/AU3) stream is not available during the current time-slot then the RPOHEN is set low. In the above example, the J1 byte of the STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream is valid but the B3 byte is not yet available in the current RPOH frame.

The path overhead data streams of corresponding STS-1 (STM-0/AU3) or equivalent receive streams are arranged in the order of the Receive Path Processing Slice numbers (RPPS #1 to RPPS #12). RPPS #1 to #12 always process the SONET/SDH bytes (i.e. STS-1 (STM-0/AU3) streams) in the received order.. With this assignment, the path overhead data streams are driven on to RPOH in the hierarchical order of STS-3 #1 STS-1 #1, STS-3 #2 STS-1 #1, STS-3 #3 STS-1 #1 - #3) STS-3 #4 STS-1 #1 and etc.

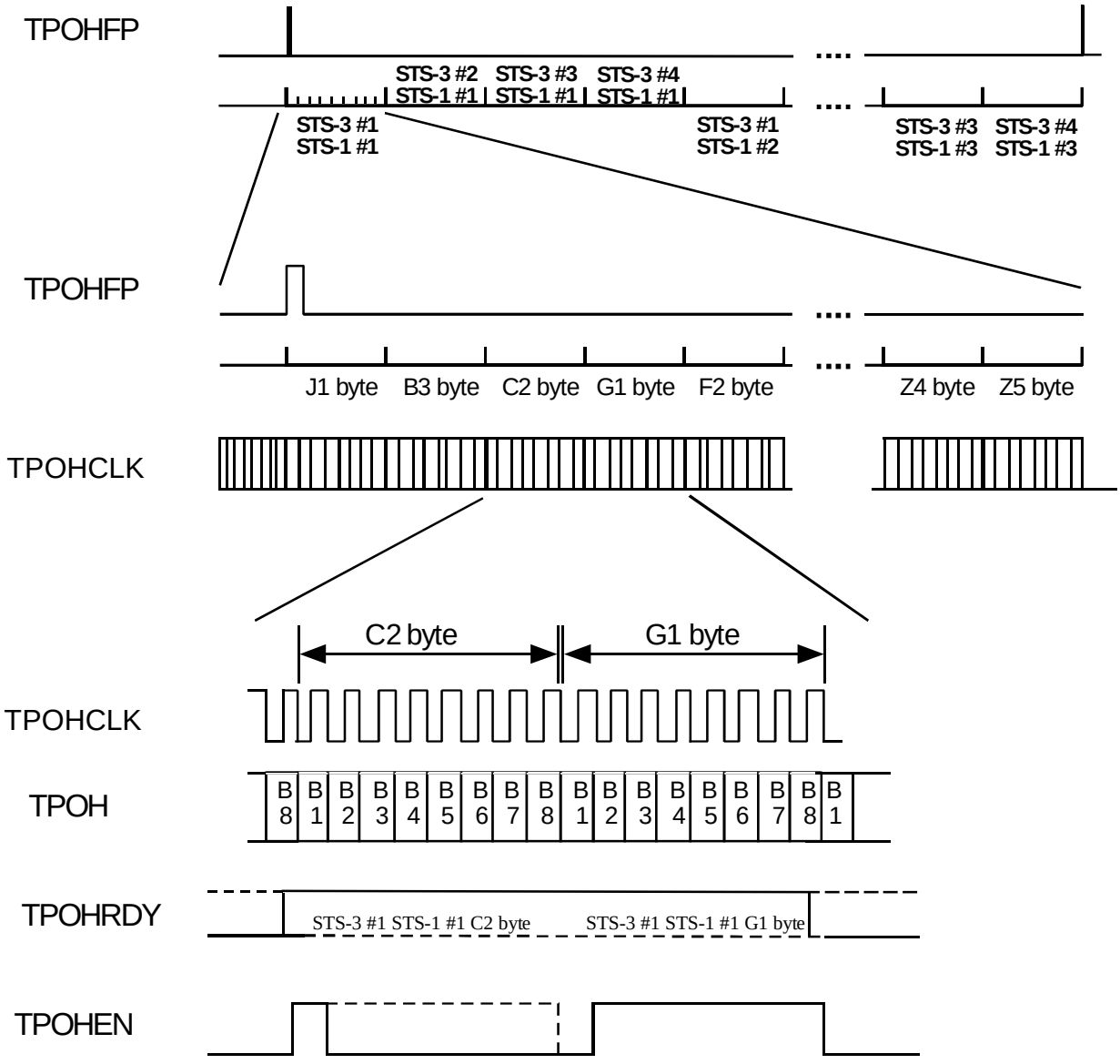
For an STS-3c (STM-1/AU4) in the STS-12 (STM-4/AU3/AU4) receive stream, only the path overhead time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 (processed by a master RPPS) carry valid path overhead bytes when RPOHEN is set high. During the path overhead time-slots of the equivalent STS-1 (STM-0/AU3) #2 and #3 processed by corresponding slave RPPS's, RPOHEN is always set low. For an STS-12c (STM-4-4c) receive stream, only the path overhead time-slots associated with the equivalent STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 (processed by the master RPPS #1) carry valid path overhead bytes when RPOHEN is set high. RPOHEN is always set low for the eleven remaining STS-1 (STM-0/AU3) equivalent streams processed by corresponding slave RPPS's.

B3E identifies the bits within the B3 bytes containing a parity error and it is only valid during the B3 byte time-slot of an STS-1 (STM-0/AU3) or equivalent stream when RPOHEN is set high.

RALM identifies an STS-1 (STM-0/AU3) or equivalent stream where one or more receive alarm conditions have been detected. The receive alarm conditions which enable an assertion during the corresponding RALM time-slot are controlled by the SPECTRA-622 RPPS RALM Output Control #1 and #2 registers. RALM for each STS-1 (STM-0/AU3) or equivalent stream is asserted during the entire

period (time-slot) when the corresponding path overhead bytes are serialized on RPOH regardless of the RPOHEN setting.

Figure 58 -Transmit Path Overhead Insertion Timing



The figure above shows the transmit path overhead insertion from a serial stream. TPOHCLK is a nominally 12.96 MHz clock and is substantially faster than the actual transmit rate of the path overhead bytes. This allows the use of

over-sampling to multiplex the path overhead data streams destined for the TPOP's on a single TPOH input. The entire path overhead, except B3 and H4, (J1, C2, G1, F2, Z3, Z4, Z5 bytes) of each STS-1 (STM-0/AU3) stream can be inserted into the STS-12 (STM-4/AU3) transmit stream via TPOH over one or two TPOH frame periods. In each byte, the most significant bit is transmitted first. TPOHFP marks the most significant bit (msb) of the first J1 byte of the STS-12 (STM-4/AU3) transmit stream. This corresponds to the msb of the J1 byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream. TPOHEN controls the insertion of data on TPOH on a byte basis. The data byte on TPOH is inserted in the path overhead of the corresponding STS-1 (STM-0/AU3) transmit stream if TPOHEN is set high and the TPOHRDY is also high when the msb of the data byte is sampled. TPOHEN assertions at the less significant bit positions are disregarded. TPOHEN is set high during (msb) bit 1 of the C2 byte and during bit 2 to bit 8 of the G1 byte with TPOHRDY set high for both bytes as shown in the above figure. For this example, the G1 byte will not be inserted but the C2 byte will be taken from TPOH. If TPOHRDY were low during the C2 byte insertion then the process should be repeated for the next C2 byte time-slot of the STS-1 (STM-0/AU3) stream.

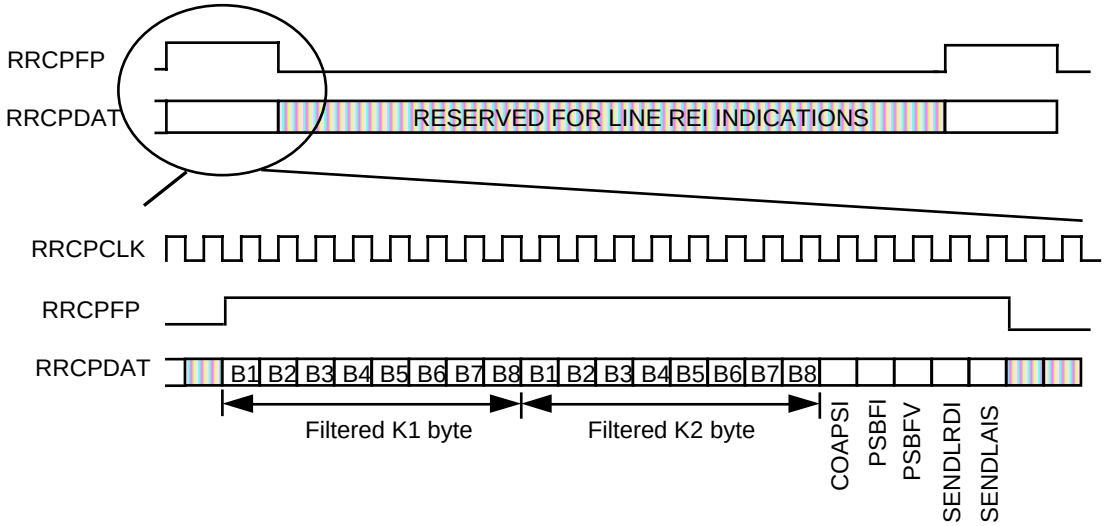
An error insertion feature is provided for the B3 and the H4 bytes. When TPOHEN and TPOHRDY are both high during the most significant bit of the B3 or H4 byte, the byte-wide error mask provided on TPOH during the B3 or H4 byte time-slot is XOR'ed to the corresponding transmit path BIP (B3) byte or tributary multiframe sequence (H4) byte.

The path overhead data streams of corresponding STS-1 (STM-0/AU3) or equivalent transmit streams are arranged in the order of the Transmit Path Processing Slice numbers (TPPS #1 to TPPS #12). TPPS #1 to #12 always process the SONET/SDH bytes (i.e. STS-1 (STM-0/AU3) streams) in the to be transmitted order.. With this assignment, the path overhead data streams are driven on to TPOH in the hierarchical order of STS-3 #1 STS-1 #1, STS-3 #2 STS-1 #1, STS-3 #3 STS-1 #1 STS-3 #4 STS-1 #1 and etc.

For an STS-3c (STM-1/AU4) in the STS-12 (STM-4/AU3/AU4) transmit stream, only the path overhead time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 processed by a master TPPS can be used. During the path overhead time-slots of the equivalent STS-1 (STM-0/AU3) #2 and #3 processed by corresponding slave TPPS's, TPOHEN must be set low. For an STS-12c (STM-4-4c) transmit stream, only the path overhead time-slots associated with the equivalent STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 processed by the master TPPS (TPPS #1) can be used. TPOHEN must be set low for the eleven remaining STS-1 (STM-0/AU3) equivalent streams processed by corresponding slaves TPPS's.

15.5 Mate SPECTRA-622 Interfaces

Figure 59 -Receive Ring Control Port



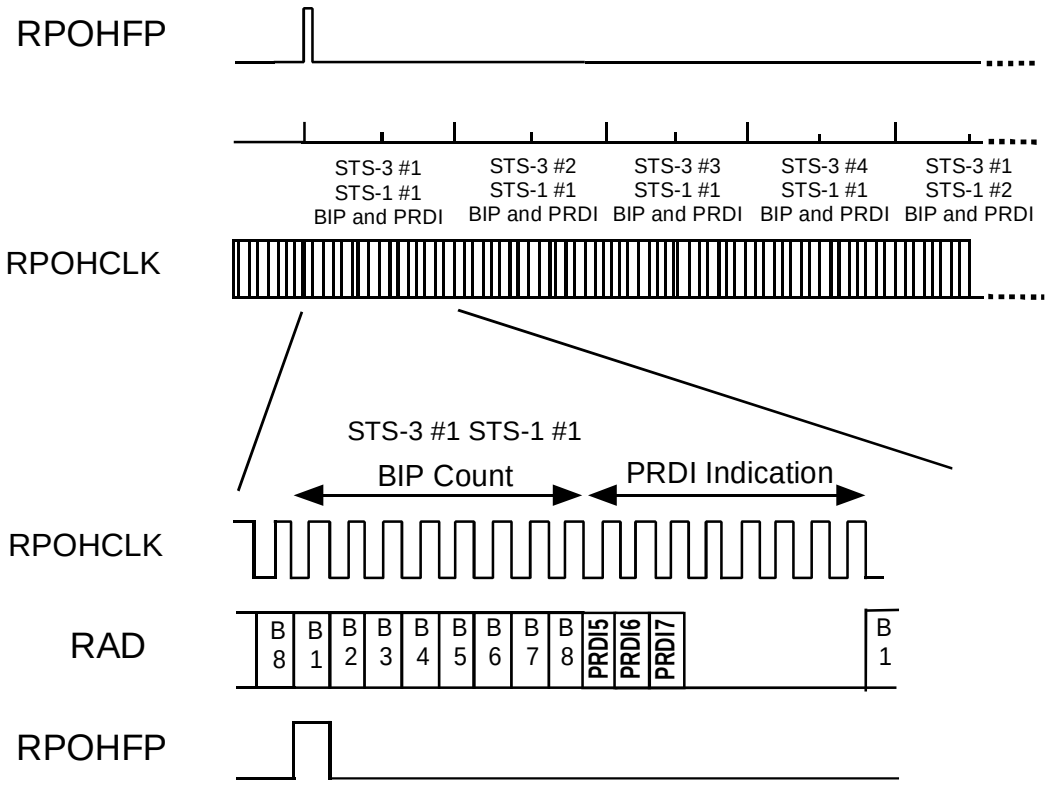
The Receive Ring Control Port timing diagram above illustrates the operation of the receive ring control port when the ring control ports are enabled (using the RCPEN bit in the SPECTRA-622 Ring Control register). The control port timing is provided by the RRCPCLK input. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK. RRCPFP is used to distinguish the bit positions carrying alarm status and maintenance signal control information (RRCPFP is high) from the bit positions carrying line REI indications (RRCPFP is low). RRCPFP is high for 21 bit positions once per 125 µs frame. Note, REI indications are enabled using the AUTOLREI bit in the SPECTRA-622 Ring Control register.

The first 16 bit positions contain the APS channel byte values after filtering (the K1 and K2 values have been identical for at least three consecutive frames, regardless of their values). The 17th bit position, COAPSI, is high for one frame when a new APS channel byte value (after filtering) is received. The 18th and 19th bit positions contain the current protection switch byte failure alarm status. PSBFI is high for one frame when a change in the protection switch byte failure alarm state is detected. PSBFV contains the real-time active high state value of the protection switch byte failure alarm. The 20th and 21st bit positions control the insertion of the line AIS and line RDI maintenance signals in a mate device. The SENDLRDI bit position is controlled by the logical OR of the section/line alarms as enabled by the SPECTRA-622 Line RDI Control register, or by the SLRDI bit in the SPECTRA-622 Ring Control Register. The SENDLAIS bit

position is controlled by the SLAIS bit in the SPECTRA-622 Ring Control Register.

While RRCPFP is low, RRCPDAT is high for one RRCPCLK cycle for each received REI indication.

Figure 60 - Receive Path Alarm Port Timing



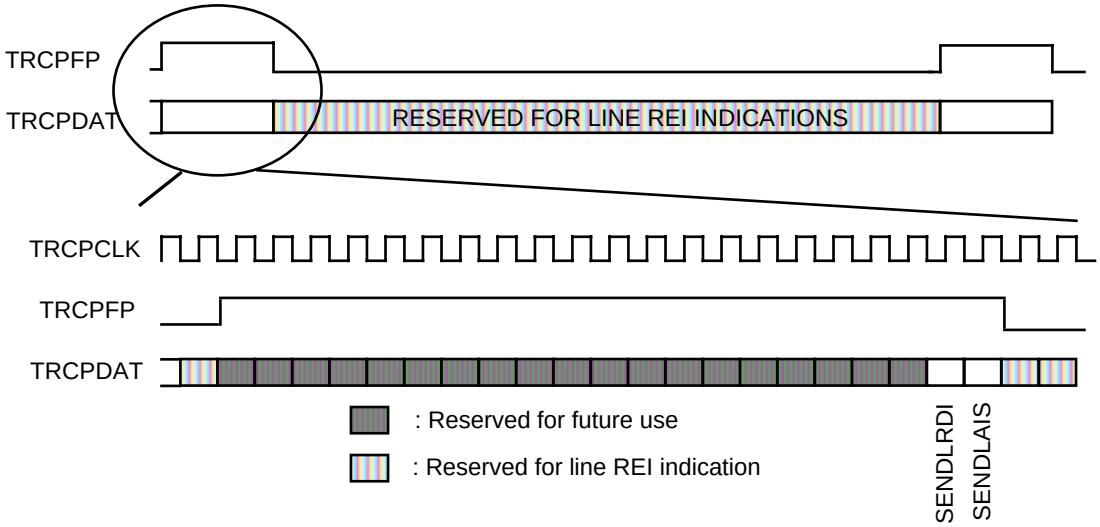
The figure above shows the format of the receive path alarm port. The path BIP-8 error counts and the PRDI codes from all STS-1 (STM-0/AU3) in an STS-12 (STM-4/AU3) receive stream are serialized in the receive alarm data output (RAD) and clocked out by RPOHCLK. Output data is updated on the falling edge of RPOHCLK. The eight BIP count bit positions for each STS-1 (STM-0/AU3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU3) stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The PRDI code bits are set when receive alarm conditions are asserted for the corresponding STS-1 (STM-0/AU3) stream. Note, BIP error indications are enabled using the AUTOPREI bit in the SPECTRA-622 RPPS Path REI/RDI Control #1 register. The PRDI5 indications are enabled

using bits in the SPECTRA-622 RPPS Path REI/RDI Control registers. The PRDI6 and PRDI7 bits are enabled using bits in the SPECTRA-622 RPPS Path Enhanced RDI Control registers.

Since the RPOHCLK is 12.96 MHz (66.6 us between RPOHFP), two BIP counts could be outputted within one frame period. So up to 16 BIP errors could be reported. On average only one BIP count is outputted per frame period (125 us).

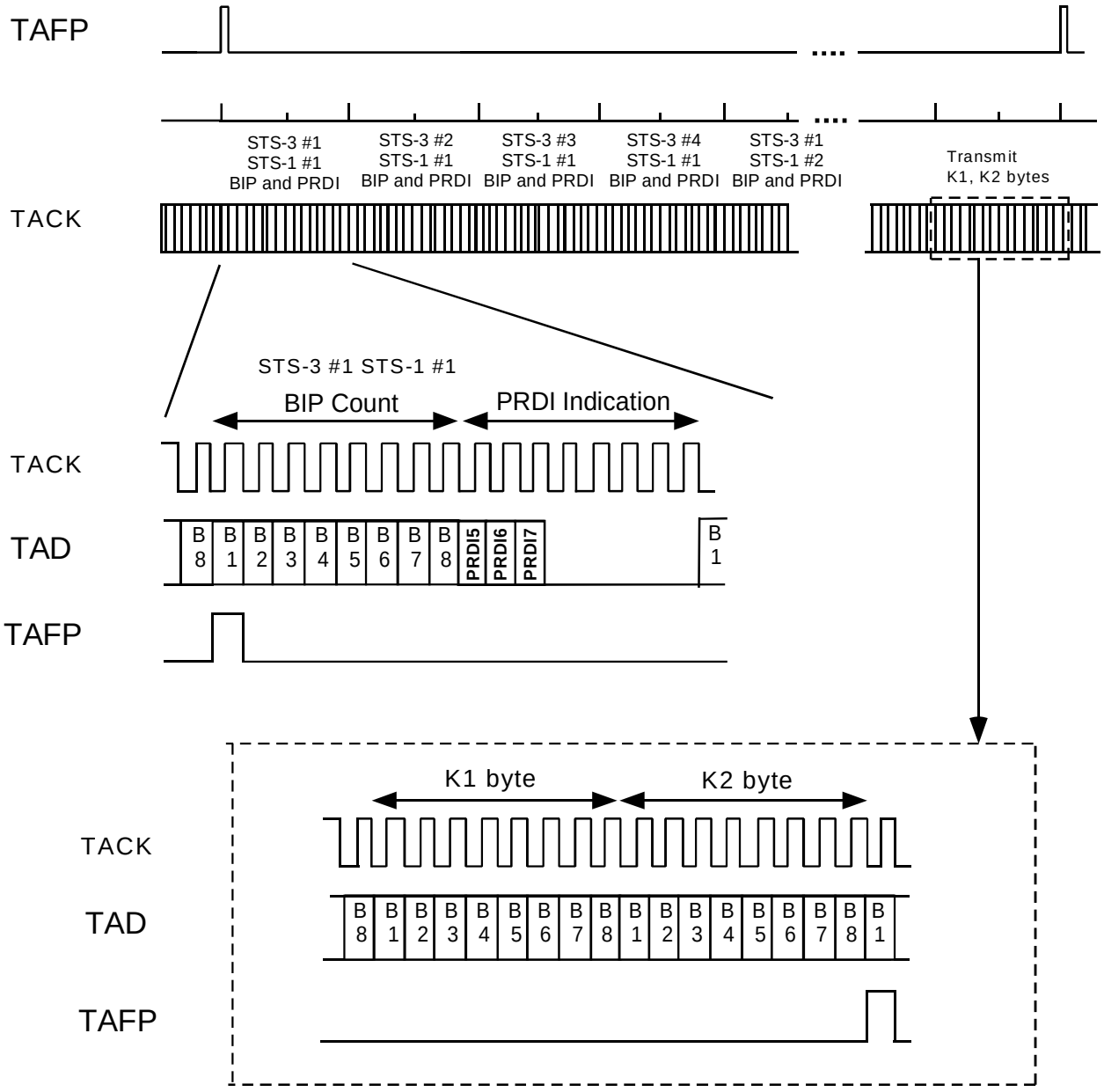
For an STS-3c (STM-1/AU4) in an STS-12 (STM-4/AU3/AU4) receive stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 carry valid information. The BIP Count and PRDI code time-slots of the equivalent STS-1 (STM-0/AU3) #2 and #3 should be ignored. For an STS-12c (STM-4-4c) receive stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 carry valid information. The BIP Count and PRDI code time-slots for the eleven remaining STS-1 (STM-0/AU3) equivalent streams should be ignored.

Figure 61 - Transmit Ring Control Port



The Transmit Ring Control Port timing diagram above illustrates the operation of the transmit ring control port when the ring control ports are enabled (using the RCPEN bit in the SPECTRA-622 Ring Control register). The control port timing is provided by the TRCPCLK input. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK. TRCPFP is used to distinguish the bit positions carrying maintenance signal control information (TRCPFP is high) from the bit positions carrying line REI indications (TRCPFP is low). TRCPFP is high for 21 bit positions once per frame 125 µs). Currently, only the last two bit positions are used. These bit positions control the insertion of line RDI and line AIS maintenance signals as illustrated. The remaining 19 bit positions are reserved for future feature enhancements.

Figure 62 - Transmit Alarm Port Timing



The figure above shows the format of the transmit path alarm port. The path BIP-8 error counts and PRDI codes for all STS-1 (STM-0/AU3) in an STS-12 (STM-4/AU3) transmit stream are serialized in the transmit alarm data input (TAD) and clocked in by TACK. The eight BIP count bit positions for each STS-1 (STM-0/AU3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU3) stream, all bit positions are set high. If there are fewer BIP

errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The PRDI code bits (PRDI5, PRDI6, PRDI7) are set accordingly when the corresponding STS-1 (STM-0/AU3) stream in the peer receive section inserts an RDI condition to be relayed back to the far end. The transmit APS channel, K1 and K2, bytes can also be sourced from TAD stream during the last two byte position in the input bit stream. Input data is sampled on the rising edge of TACK.

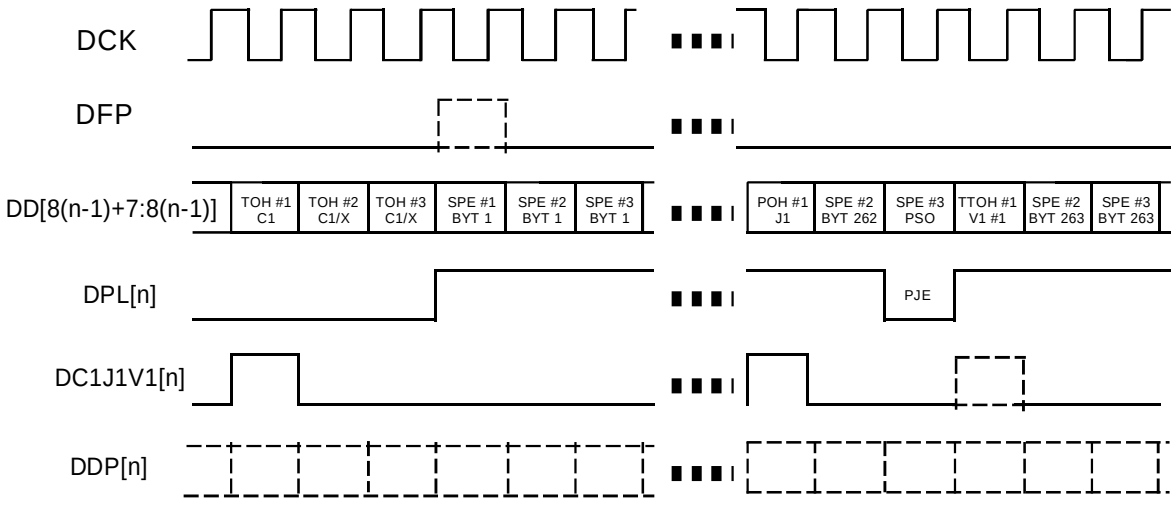
For an STS-3c (STM-1/AU4) in an STS-12 (STM-4/AU3/AU4) transmit stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 can be used. The TAD input must be set low during the BIP Count and PRDI code time-slots of the equivalent STS-1 (STM-0/AU3) #2 and #3. For an STS-12c (STM-4-4c) transmit stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 can be used. The TAD input must be set low during the BIP Count and PRDI code time-slots for the eleven remaining STS-1 (STM-0/AU3) equivalent streams.

The TAD port can revtrieve up to 15 BIP errors for each slice per frame. Given the timing of the RAD port, a mate SPECTRA-622 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames and the timing makes them appear within one frame period, the 16th count could be lost.

15.6 Telecom Bus System Side

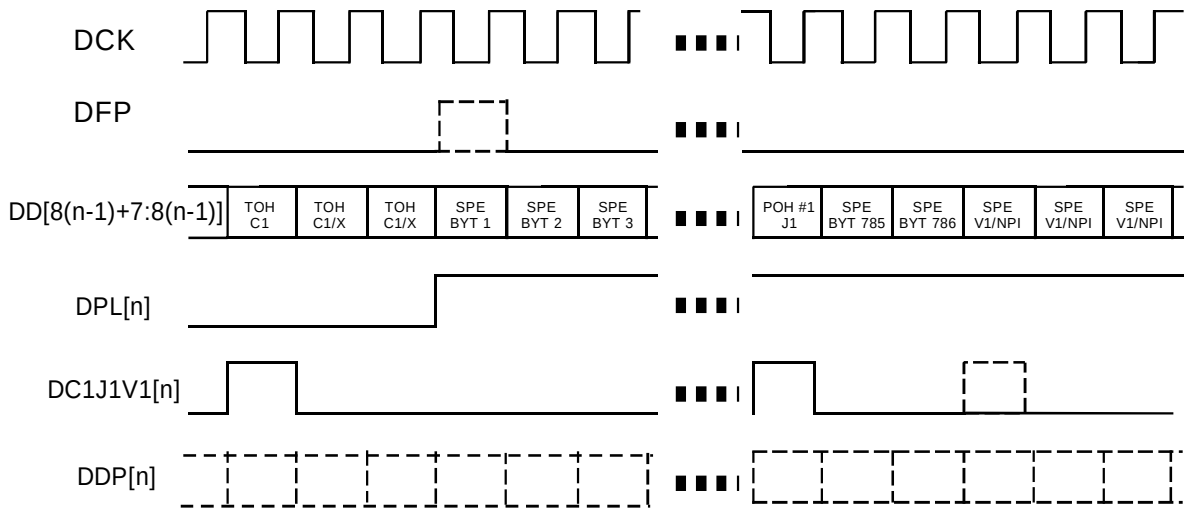
15.6.1 DROP Bus

Figure 63 - STS-3 (STM-1/AU3) 19.44 MHz Byte DROP Bus Timing



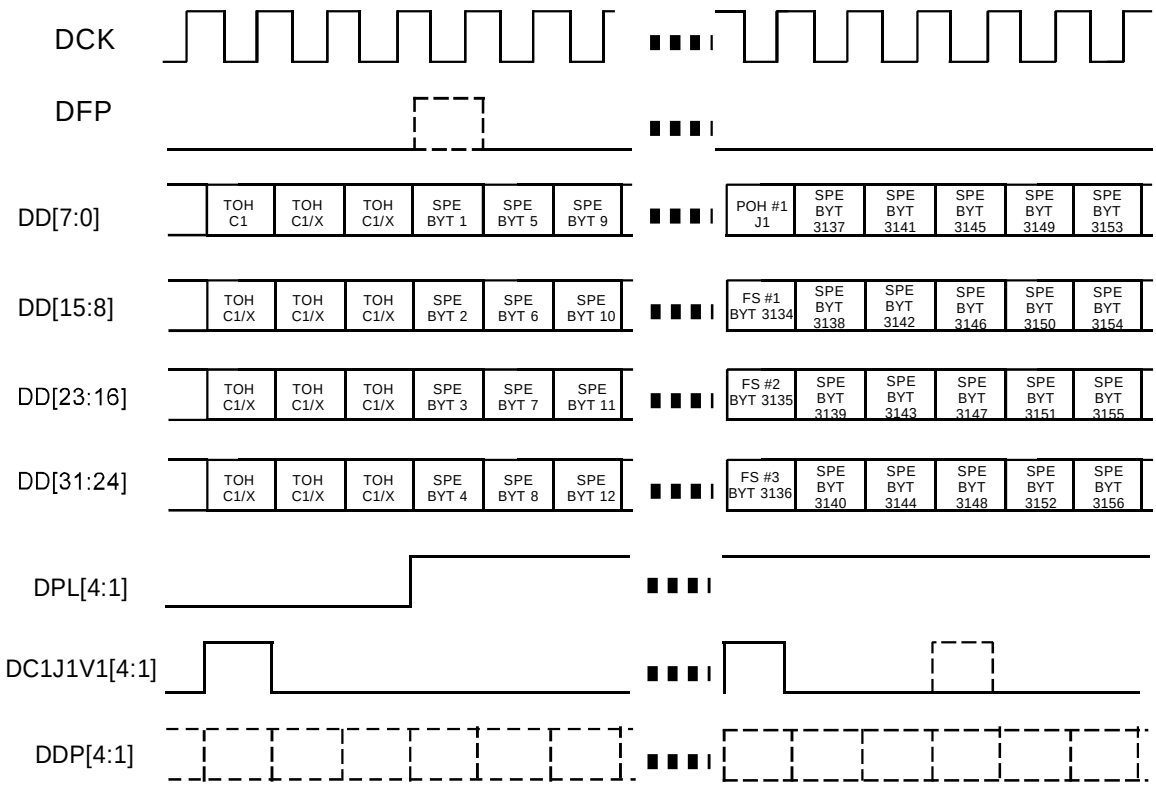
The figure above shows the STS-3 (STM-1/AU3) 19.44 MHz byte DROP bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom DROP buses. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-3 (STM-1/AU3) frame on DD[7:0] (DD[31:24], DD[23:16], DD[15:8]). It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] (DPL[4], DPL[3], DPL[2]) output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 (STM-0/AU3) #3. A stuff byte is place in the positive stuff opportunity byte position and DPL[1] (DPL[4:2]) is set low to indicate that data is not available. The DROP bus composite timing signal DC1J1V1[1] (DC1J1V1[4], DC1J1V1[3], DC1J1V1[2]) is set high when DPL[1] (DPL[4:2]) is set low to mark the C1 byte. DC1J1V1[1] (DC1J1V1[4:2]) is set high when DPL[1] (DPL[4:2]) is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU3) streams. Optionally, DC1J1V1[1] (DC1J1V1[4:2]) is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom DROP buses may be different. The DROP bus parity output DDP[1] (DDP[4], DDP[3], DDP[2]) reports the parity of DD[7:0] (DD[31:24], DD[23:16], DD[15:8]) and optionally includes DPL[1] (DPL[4:2]) and DC1J1V1[1] (DC1J1V1[4:2]).

Figure 64 - STS-3c (STM-1/AU4) 19.44 MHz Byte DROP Bus Timing



The figure above shows the STS-3c (STM-1/AU4) 19.44 MHz byte DROP bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom DROP buses. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte on DD[7:0] (DD[31:24], DD[23:16], DD[15:8]). It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] (DPL[4], DPL[3], DPL[2]) output which is set low to mark transport overhead bytes and set high to mark payload bytes. The DROP bus composite timing signal DC1J1V1[1] (DC1J1V1[4], DC1J1V1[3], DC1J1V1[2]) is set high when DPL[1] (DPL[4:2]) is set low to mark the C1 byte. DC1J1V1[1] (DC1J1V1[4:2]) is set high when DPL[1] (DPL[4:2]) is also set high to mark the J1 byte of the STS-3c (STM-1/AU4) stream. Optionally, DC1J1V1[1] (DC1J1V1[4:2]) is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe. When processing an STS-3c (STM-1/AU4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c (STM-1/AU4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom DROP buses may be different. The DROP bus parity output DDP[1] (DDP[4], DDP[3], DDP[2]) reports the parity of DD[7:0] (DD[31:24], DD[23:16], DD[15:8]) and optionally includes DPL[1] (DPL[4:2]) and DC1J1V1[1] (DC1J1V1[4:2]).

Figure 65 - STS-12c (STM-4-4c) 19.44 MHz Byte DROP Bus Timing

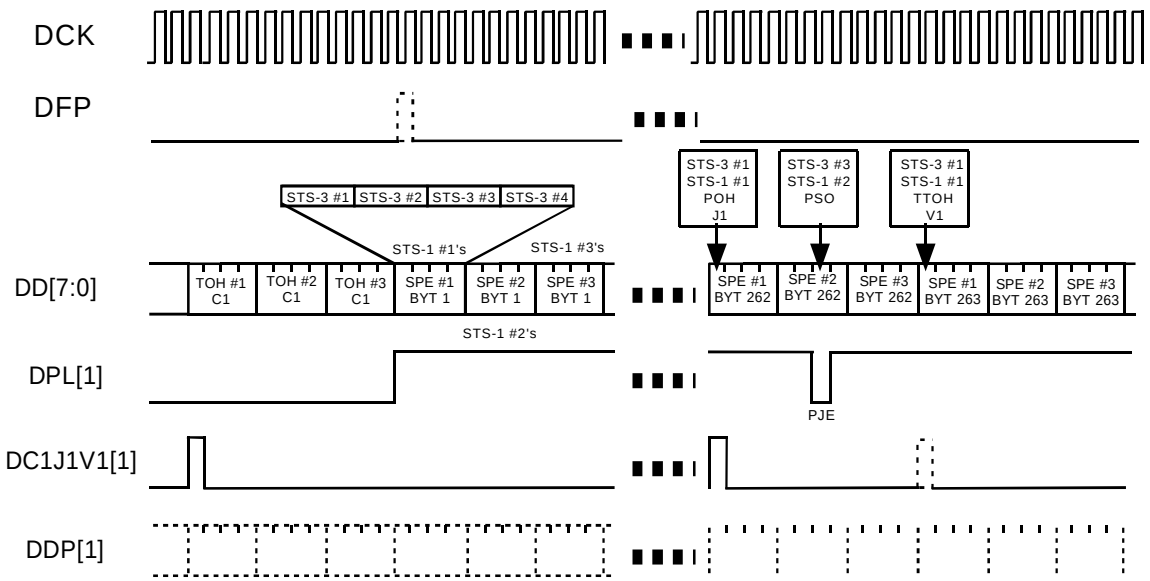


The figure above shows the STS-12c (STM-4-4c) 19.44 MHz byte DROP bus timing. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first, second, third and fourth synchronous payload envelope (SPE) bytes of the STS-12c (STM-4-4c) on DD[7:0], DD[15:8], DD[23:16] and DD[31:24] respectively. The SPE bytes are numbered according to the order of reception. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes on DD[7:0], DD[15:8], DD[23:16] and DD[31:24] are distinguished by the DPL[1]. DPL[2], DPL[3] and DPL[4] are set to the same value as DPL[1]. The DROP bus composite timing signal DC1J1V1[1] is set high when DPL[1] is set low to mark the first C1 byte. DC1J1V1[1] is set high when DPL[1] is also set high to mark the J1 byte of the STS-12c (STM-4-4c) stream. Optionally, DC1J1V1[1] is set high once every multiframe (four STS-12c (STM-4-4c) frames) to mark the third byte after the J1 byte on DD[7:0]. DC1J1V1[2], DC1J1V1[3] and DC1J1V1[4] will pulse to identify the C1 byte position but no J1 or V1 pulses will be present.7

The alignment of the transport frame and the synchronous payload envelope of the STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output

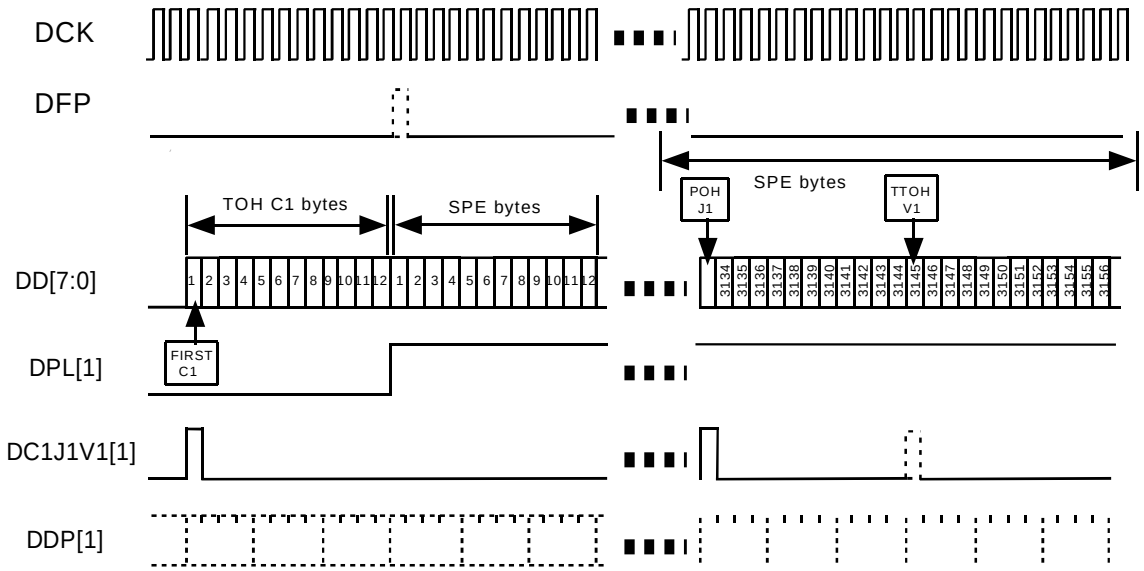
DDP[1] (DDP[2], DDP[3], DDP[4]) reports the parity of DD[7:0] (DD[15:8], DD[23:16], DD[31:24]) and optionally includes DPL[1] (DPL[2], DPL[3], DPL[4]) and DC1J1V1[1]] (DC1J1V1[2], DC1J1V1[3], DC1J1V1[4]).

Figure 66 - STS-12 (STM-4/AU3) 77.76 MHz Byte DROP Bus Timing



The figure above shows the STS-12 (STM-4/AU3) 77.76 MHz byte DROP bus timing. DCK is a 77.76 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-12 (STM-4/AU3) frame on DD[7:0]. This is also the first SPE byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #2. A stuff byte is place in the positive stuff opportunity byte position and DPL[1] is set low to indicate that data is not available. The DROP bus composite timing signal DC1J1V1[1] is set high when DPL[1] is set low to mark the first C1 byte of the STS-12 (STM-4/AU3) frame. DC1J1V1[1] is set high when DPL[1] is also set high to mark the J1 byte in each of the STS-1 (STM-0/AU3) streams. Optionally, DC1J1V1[1] is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP[1] reports the parity of DD[7:0] and optionally includes DPL[1] and DC1J1V1[1].

Figure 67 - STS-12c (STM-4-4c) 77.76 MHz Byte DROP Bus Timing

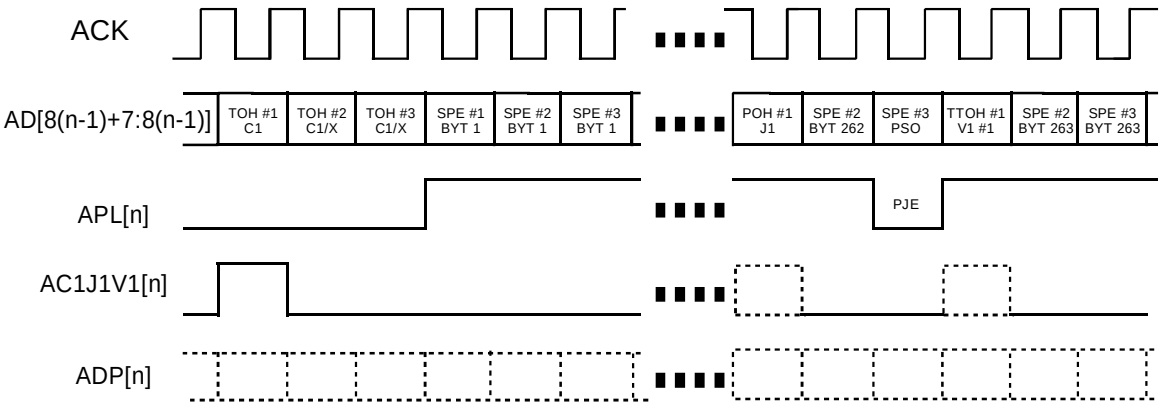


The figure above shows the STS-12c (STM-4-4c) 77.76 MHz byte DROP bus timing. DCK is a 77.76 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] output which is set low to mark transport overhead bytes and set high to mark payload bytes. The DROP bus composite timing signal DC1J1V1[1] is set high when DPL[1] is set low to mark the first C1 byte. DC1J1V1[1] is set high when DPL[1] is also set high to mark the J1 byte of the STS-12c (STM-4-4c) stream. Optionally, DC1J1V1[1] is set high once every multiframe to mark the “V1 byte” in the first frame of the DROP bus tributary multiframe. The “V1 byte” corresponds to the 12-th byte after J1. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP[1] reports the parity of DD[7:0] and optionally includes DPL[1] and DC1J1V1[1].

During a PAIS condition, jump in J1 location can occur on DC1J1V1.

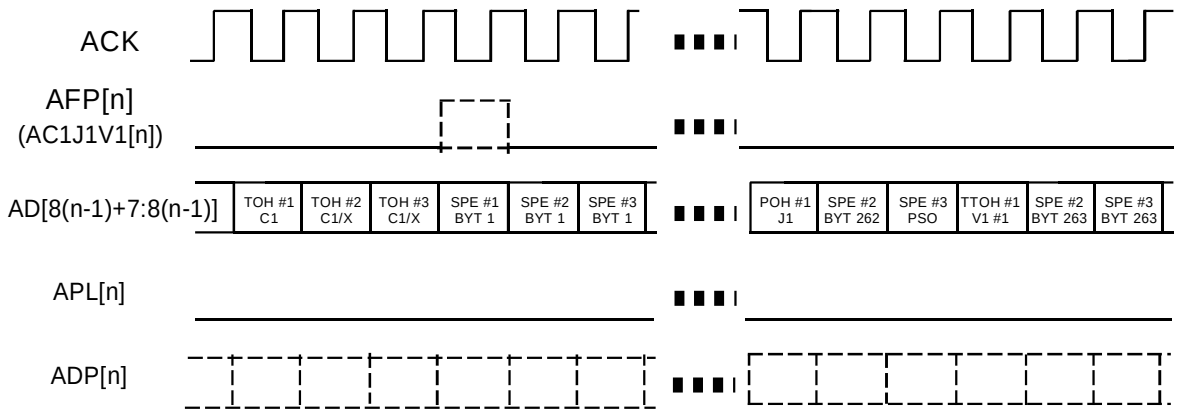
15.6.2 ADD Bus

Figure 68 - STS-3 (STM-1/AU3) 19.44 MHz Byte ADD Bus Timing



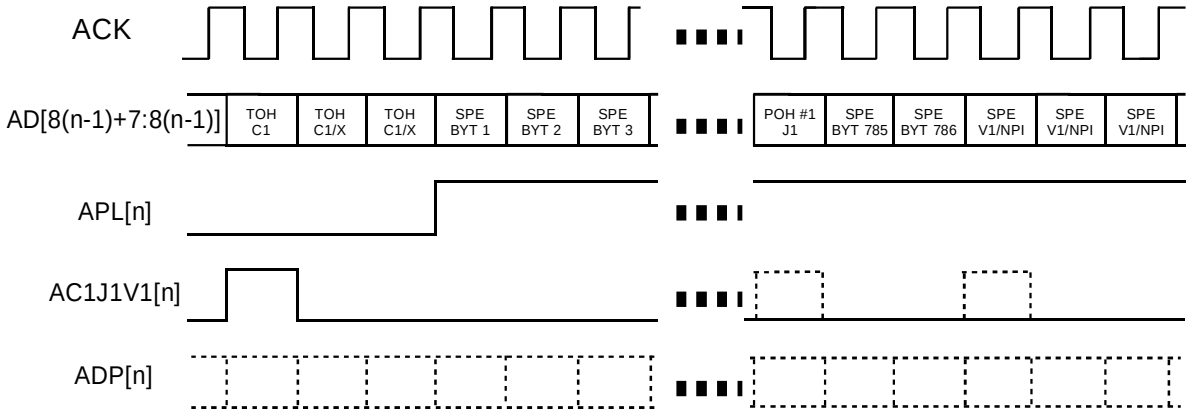
The figure above shows the STS-3 (STM-1/AU3) 19.44 MHz byte ADD bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom ADD buses. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] (APL[4], APL[3], APL[2]) input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). A positive justification event is shown for STS-1 (STM-0/AU3) #3. A stuff byte is place in the positive stuff opportunity byte and APL[1] (APL[4], APL[3], APL[2]) is set low to indicate that data is not available. The ADD bus composite timing signal AC1J1V1[1] (AC1J1V1[4], AC1J1V1[3], AC1J1V1[2]) is set high when APL[1] (APL[4:2]) is set low to mark the C1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high when APL[1] (APL[4:2]) is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU3) streams. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom ADD buses may be different. The ADD bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and optionally includes APL[1] (APL[4:2]) and AC1J1V1[1] (AC1J1V1[4:2]).

Figure 69 - STS-3 (STM-1/AU3) 19.44 MHz Byte ADD Bus (AFP) Timing



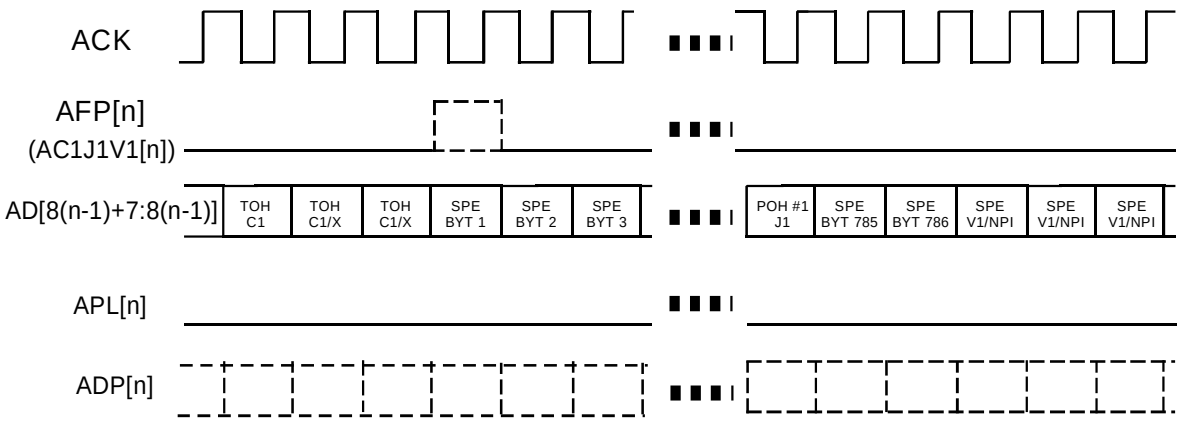
The figure above shows the STS-3 (STM-1/AU3) 19.44 MHz byte ADD bus (AFP) timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom ADD buses. ACK is a 19.44 MHz clock. The frame pulse AFP[1] (AFP[4], AFP[3], AFP[2]) marks the first synchronous payload envelope byte in the STS-3 (STM-1/AU3) frame on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]), all AFP[n] signals must be aligned. It is not necessary for AFP[n] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[n] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and the APL[1] (APL[4:2]) input signal must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the first frame of the ADD bus tributary multiframe in each STS-1 (STM-0/AU3) stream is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the synchronous payload envelope of STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom ADD buses may be different. The ADD bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]).

Figure 70 - STS-3c (STM-1/AU4) 19.44 MHz Byte ADD Bus Timing



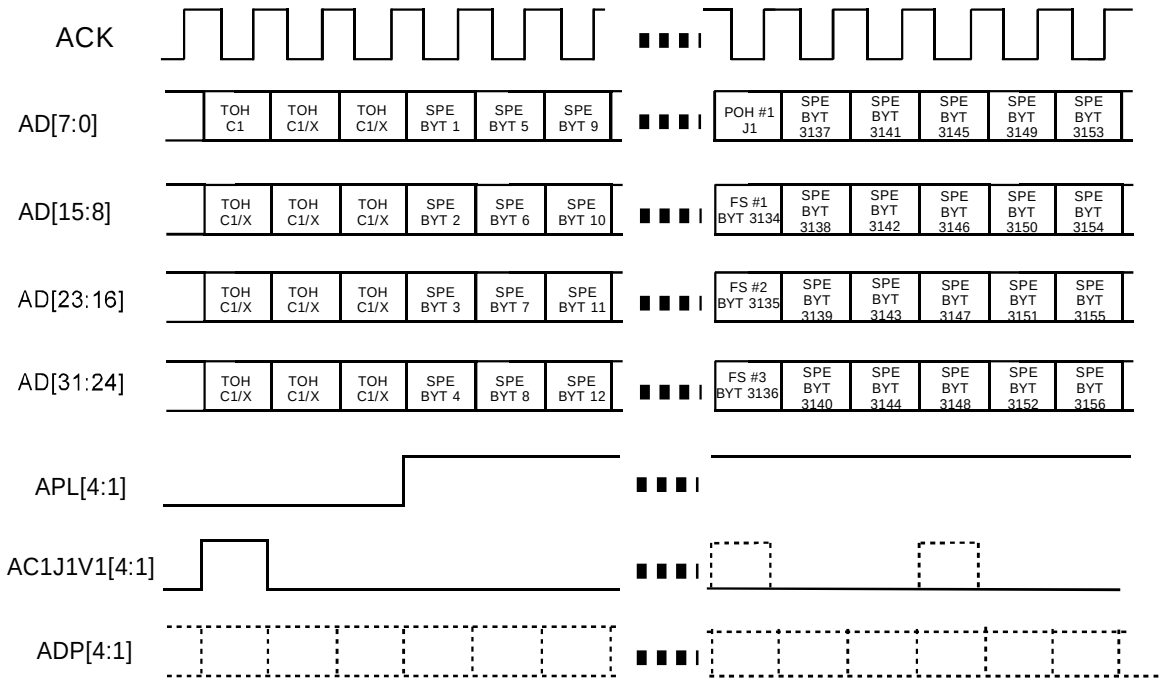
The figure above shows the STS-3c (STM-1/AU4) 19.44 MHz byte ADD bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom ADD buses. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] (APL[4], APL[3], APL[2]) input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). The ADD bus composite timing signal AC1J1V1[1] (AC1J1V1[4], AC1J1V1[3], AC1J1V1[2]) is set high when APL[1] (APL[4:2]) is set low to mark the C1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high when APL[1] (APL[4:2]) is also set high to mark the J1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe. When processing an STS-3c (STM-1/AU4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c (STM-1/AU4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom ADD buses may be different. The ADD bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and optionally includes APL[1] (APL[4:2]) and AC1J1V1[1] (AC1J1V1[4:2]).

Figure 71 - STS-3c (STM-1/AU4) 19.44 MHz Byte ADD Bus (AFP) Timing



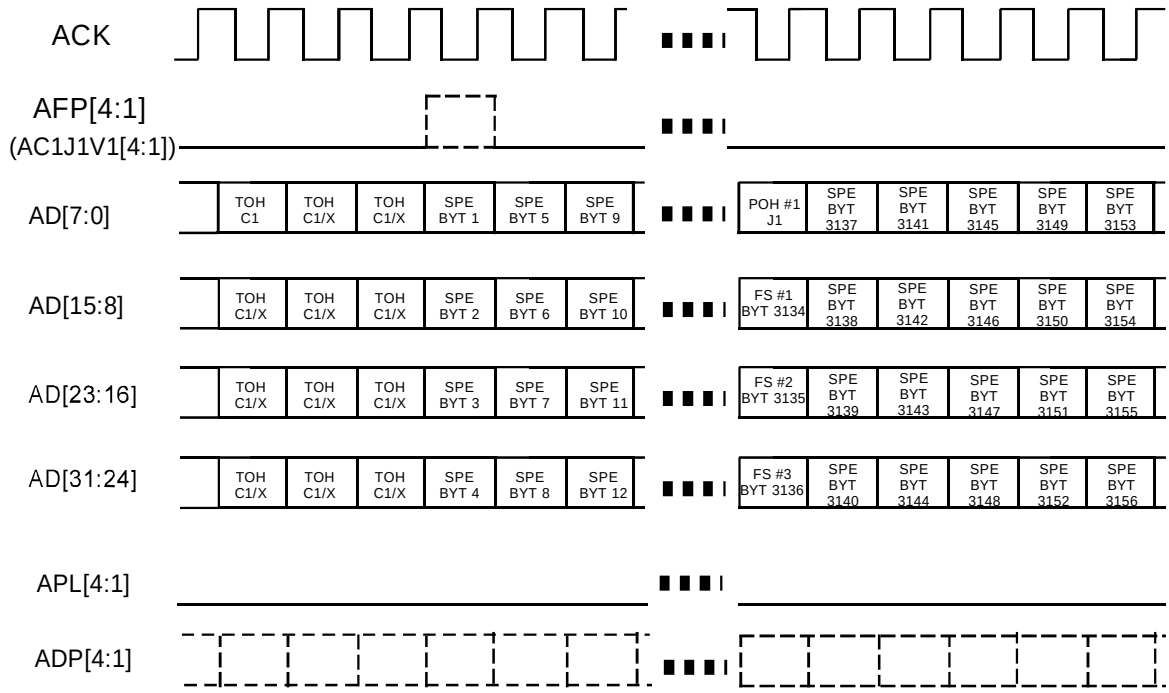
The figure above shows the STS-3c (STM-1/AU4) 19.44 MHz byte ADD bus (AFP) timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom ADD buses. ACK is a 19.44 MHz clock. The frame pulse AFP[1] (AFP[4], AFP[3], AFP[2]) marks the first synchronous payload envelope byte in the STS-3c (STM-1/AU4) frame on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]), all AFP[n] signals must be aligned. It is not necessary for AFP[n] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[n] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and the APL[1] (APL[4:2]) input signal must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the V1 byte in the first frame of the ADD bus tributary multiframe is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the synchronous payload envelope of STS-3c (STM-1/AU4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom ADD buses may be different. The ADD bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]).

Figure 72 - STS-12c (STM-4-4c) 19.44 MHz Byte ADD Bus Timing



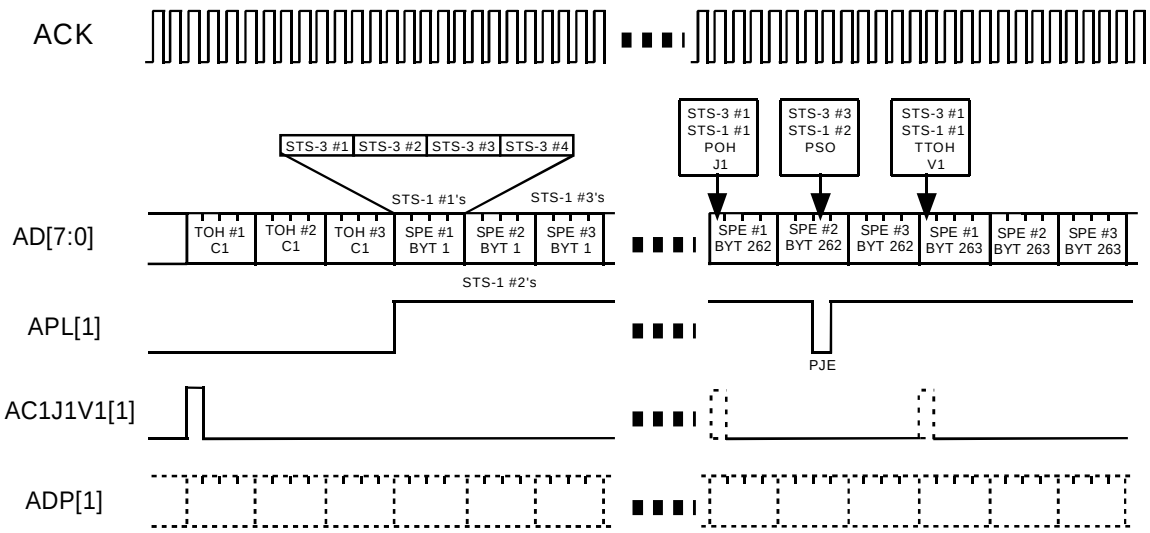
The figure above shows the STS-12c (STM-4-4c) 19.44 MHz byte ADD bus timing. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] (APL[2], APL[3], APL[4]) input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0] (AD[15:8], AD[23:16], AD[31:24]). The ADD bus composite timing signal AC1J1V1[1] (AC1J1V1[2], AC1J1V1[3], AC1J1V1[4]) is set high when APL[1] (APL[2], APL[3], APL[4]) is set low to mark the first (second, third, fourth) C1 byte. All four C1 indications on AC1J1V1[4:1] (i.e. transport frames) must be coincident and the SPE bytes of the STS-12c (STM-4-4c) stream must be presented to the four ADD buses in the order as depicted above. The SPE bytes shown in the figure are numbered according to the order of transmission. Optionally, AC1J1V1[1] is set high when APL[1] is also set high to mark the J1 byte of the STS-12c (STM-4-4c) stream on AD[7:0]. Optionally, AC1J1V1[1] is set high once every multiframe to mark the “V1 byte” of the first frame of the ADD bus tributary multiframe on AD[7:0]. The “V1 byte” corresponds to the third byte after J1 on AD[7:0]. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] (ADP[2], ADP[3], ADP[4]) carries the parity of AD[7:0] (AD[15:8], AD[23:16], AD[31:24]) and optionally includes APL[1] (APL[2], APL[3], APL[4]) and AC1J1V1[1] (AC1J1V1[2], AC1J1V1[3], AC1J1V1[4]).

Figure 73 -STS-12c (STM-4-4c) 19.44 MHz Byte ADD Bus (AFP) Timing



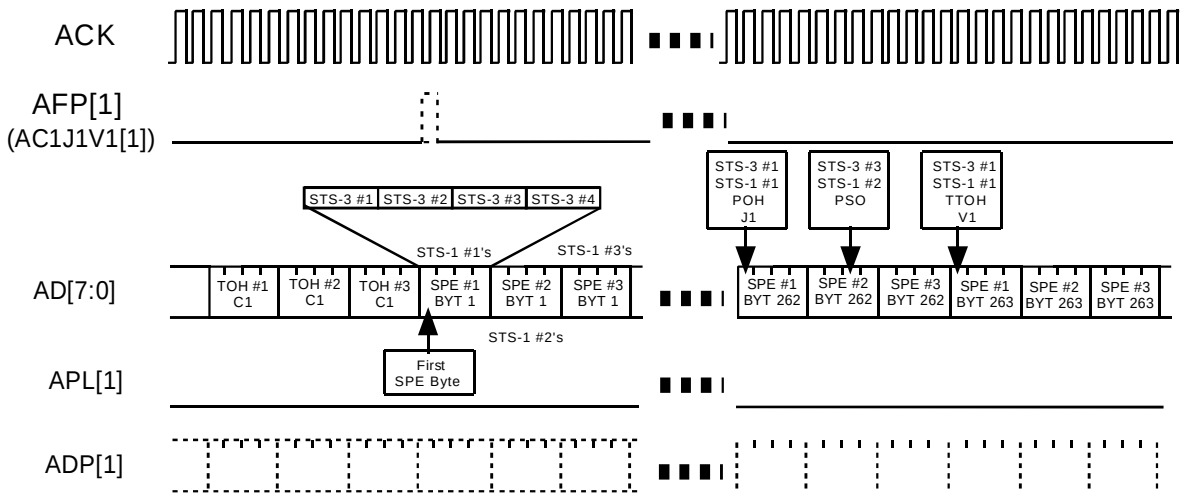
The figure above shows the STS-12c (STM-4-4c) 19.44 MHz byte ADD bus (AFP) timing. ACK is a 19.44 MHz clock. The frame pulse AFP[1] (AFP[2], AFP[3], AFP[4]) marks the first (second, third, fourth) synchronous payload envelope byte in the STS-12c (STM-4-4c) frame on AD[7:0] (AD[15:8], AD[23:16], AD[31:24]), all AFP[n] must be aligned. It is not necessary for AFP[n] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[n] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] and the APL[4:1] inputs must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. All four frame pulses on AFP[4:1] (i.e. transport frames) must be coincident and the SPE bytes of the STS-12c (STM-4-4c) stream must be presented to the four ADD buses in the order as depicted above. The SPE bytes shown in the figure are numbered according to the order of transmission. Optionally, the “V1 byte” in the first frame of the ADD bus tributary multiframe is determined by interpreting the H4 byte in the corresponding path overhead. The “V1 byte” corresponds to the third byte after J1 on AD[7:0]. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] (ADP[2], ADP[3], ADP[4]) carries the parity of AD[7:0] (AD[15:8], AD[23:16], AD[31:24]).

Figure 74 - STS-12 (STM-12/AU3) 77.76 MHz Byte ADD Bus Timing



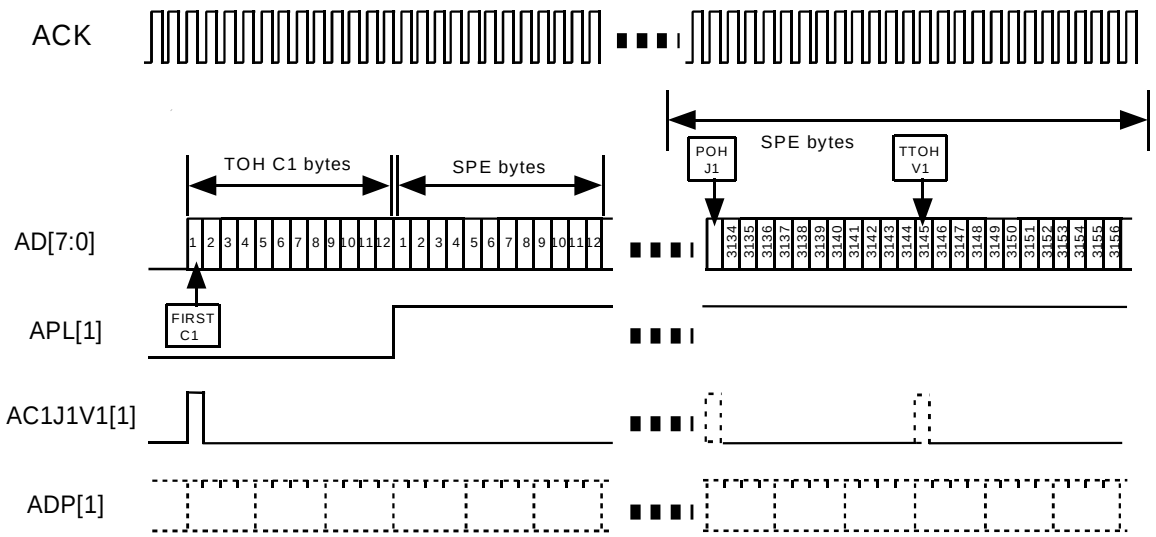
The figure above shows the STS-12 (STM-4/AU3) 77.76 MHz byte ADD bus timing. ACK is a 77.76 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0]. A positive justification event is shown for STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #2. A stuff byte is place in the positive stuff opportunity byte and APL[1] is set low to indicate that data is not available. The ADD bus composite timing signal AC1J1V1[1] is set high when APL[1] is set low to mark the first C1 byte. Optionally, AC1J1V1[1] is set high when APL[1] is also set high to mark the J1 byte in each of the STS-1 (STM-0/AU3) streams. Optionally, AC1J1V1[1] is set high once every multiframe to mark the V1 byte of first frame of the ADD bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-3 #1 STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] carries the parity of AD[7:0] and optionally includes APL[1] and AC1J1V1[1].

Figure 75 - STS-12 (STM-12/AU3) 77.76 MHz Byte ADD Bus (AFP) Timing



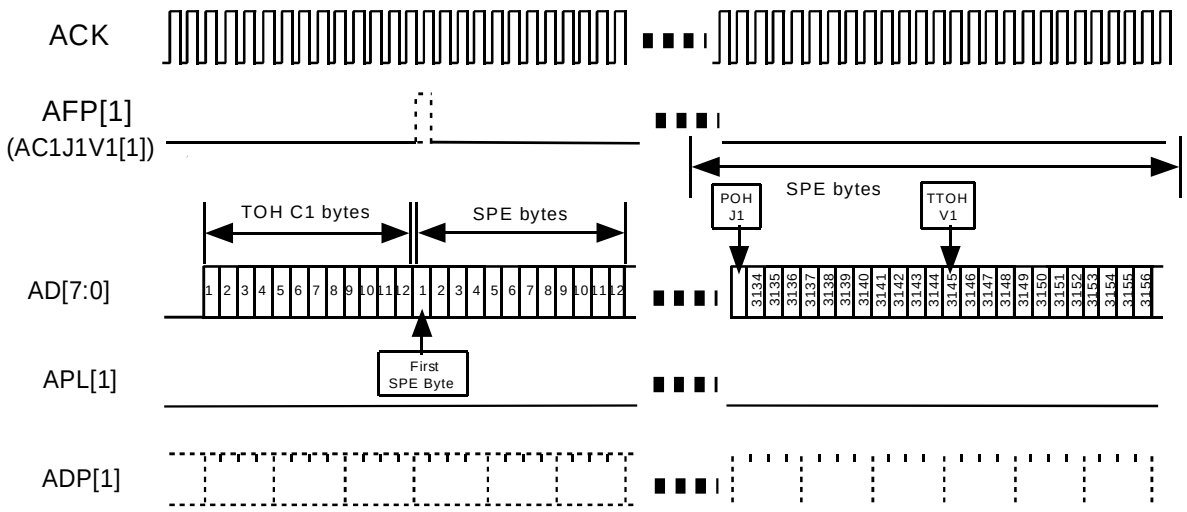
The figure above shows the STS-12 (STM-4/AU3) 77.76 MHz byte ADD bus (AFP) timing. ACK is a 77.76 MHz clock. The frame pulse AFP[1] marks the first synchronous payload envelope byte in the STS-12 (STM-4/AU3/AU4) frame on AD[7:0]. It is not necessary for AFP[1] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[1] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] for each STS-1 (STM-0/AU3) or equivalent stream and the APL[1] input must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the V1 byte in the first frame of the ADD bus tributary multiframe for each STS-1 (STM-0/AU3) or equivalent stream is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the synchronous payload envelope of STS-3 #1 STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] carries the parity of AD[7:0].

Figure 76 - STS-12c (STM-4-4c) 77.76 MHz Byte ADD Bus Timing



The figure above shows the STS-12c (STM-4-4c) 77.76 MHz byte ADD bus timing. ACK is a 77.76 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0]. The ADD bus composite timing signal AC1J1V1[1] is set high when APL[1] s set low to mark the first C1 byte. Optionally, AC1J1V1[1] is set high when APL[1] is also set high to mark the J1 byte. Optionally, AC1J1V1[1] is set high once every multiframe to mark the “V1 byte” of the first frame of the ADD bus tributary multiframe. The “V1 byte” corresponds to the 12-th byte after J1. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] carries the parity of AD[7:0] and optionally includes APL[1] and AC1J1V1[1].

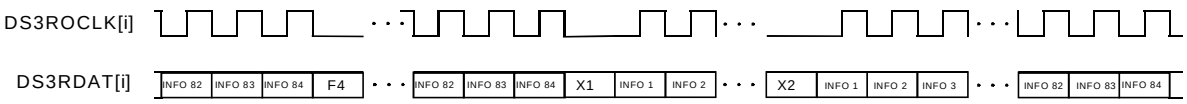
Figure 77 - STS-12c (STM-4-4c) 77.76 MHz Byte ADD Bus (AFP) Timing



The figure above shows the STS-12c (STM-4-4c) 77.76 MHz byte ADD bus (AFP) timing. ACK is a 77.76 MHz clock. The frame pulse AFP[1] marks the first synchronous payload envelope byte in the STS-12c (STM-4-4c) frame on AD[7:0]. It is not necessary for AFP[1] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[1] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] and the APL[1] input must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the “V1 byte” in the first frame of the ADD bus tributary multiframe is determined by interpreting the H4 byte in the corresponding path overhead. The “V1 byte” corresponds to the 12-th byte after J1. The alignment of the transport frame and the synchronous payload envelope of STS-12c (STM-4-4c) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP[1] carries the parity of AD[7:0].

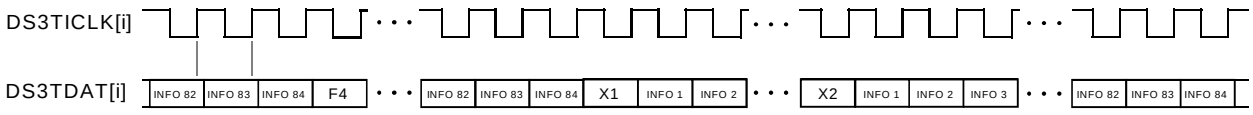
15.7 DS3 Mode System Side

Figure 78 - STS-1 (STM-0/AU3) DS3 DROP Interface Timing



The figure above shows the STS-1 (STM-0/AU3) DS3 DROP Interface timing. DS3ROCLK[i] is a gapped clock of serial bus #i where i = {1 .. 12}. Data bits on the DS3RDAT[i] bus are updated on the falling edge of DS3ROCLK[i]. The gapped clock is generated using an internal 51.84 MHz clock derived from the line clock or an external 44.928 MHz clock from the DS3RICLK input. The nominal frequency of DS3ROCLK[i] is 44.736 MHz. The line clock requires the REFCLK signal.

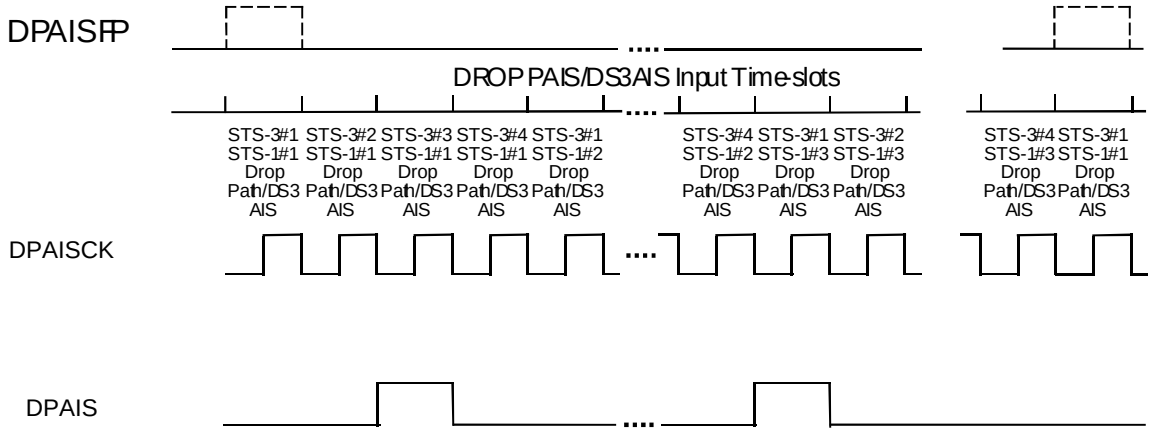
Figure 79 - STS-1 (STM-0/AU3) DS3 ADD Interface Timing



DS3TICLK[i] is a gapped clock used to fetch input data from a data source. The nominal frequency of DS3TICLK[i] is 44.736 MHz. Data bits on the DS3TDAT[i] bus are sampled on the rising edge of DS3TICLK[i].

15.8 System Side Path and DS3 AIS Control Port

Figure 80 - System DROP Side Path/DS3 AIS Control Port Timing

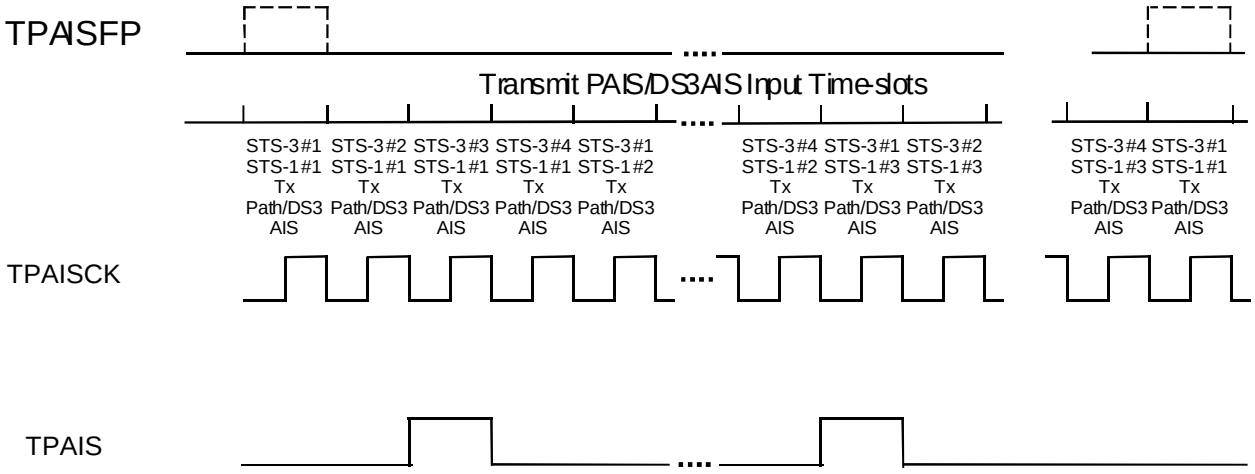


The figure above shows the System DROP Side Path/DS3 AIS Control Port timing. The frame pulse DPAISFP marks the first STS-1 (STM-0/AU3) or equivalent DROP bus path/DS3 AIS assertion control signal on the DPAIS input. It is not necessary for DPAISFP to be present at every frame. An internal counter fly-wheels based on the most recent DPAISFP received. The DPAISFP and DPAIS inputs are sampled on the rising edge of DPAISCK. When the DPAISFP alignment changes, the PAIS value sampled at the same time as the new DPAISFP will be according to the previous alignment. The subsequent DPAIS will be according to the new DPAISFP.

The path/DS3 AIS assertion control signals are multiplexed according to the hierarchical order of STS-1 #1 (STS-3 #1 - #4), STS-1 #2 (STS-3 #1 - #4) and STS-1 #3 (STS-3 #1 - #4) for the twelve STS-1 (STM-0/AU3) or equivalent receive streams. The above figure shows DROP bus path/DS3 AIS assertion for the STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #1 and STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #3 receive streams. The DPAIS must be set high during the above time-slots in consecutive DPAIS frames for continuous path/DS3 AIS assertion. Path/DS3 AIS assertion of a stream is removed when the corresponding DPAIS time-slot is set low.

The time-slot assignment on DPAIS is unrelated to the configuration of the STS (STM) groups in the receive streams. For a concatenated stream, only the time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 can be used. DPAIS must be set low during the time-slots for the remaining STS-1 (STM-0/AU3) equivalent streams in the concatenated stream.

Figure 81 - System ADD Side Path/DS3 AIS Control Port Timing



The figure above shows the System ADD Side Path/DS3 AIS Control Port timing. The frame pulse TPAISFP marks the first STS-1 (STM-0/AU3) or equivalent transmit stream path/DS3 AIS assertion control signal on the TPAIS input. It is not necessary for TPAISFP to be present at every frame. An internal counter fly-wheels based on the most recent TPAISFP received. The TPAISFP and TPAIS inputs are sampled on the rising edge of TPAISCK. When the TPAISFP alignment changes, the PAIS value sampled at the same time as the new TPAISFP will be according to the previous alignment. The subsequent TPAIS will be according to the new TPAISFP.

The path/DS3 AIS assertion control signals are multiplexed according to the hierarchical order of STS-1 #1 (STS-3 #1 - #4), STS-1 #2 (STS-3 #1 - #4) and STS-1 #3 (STS-3 #1 - #4) for the twelve STS-1 (STM-0/AU3) or equivalent transmit streams. The above figure shows transmit path/DS3 AIS assertion for the STS-3 (STM-1) #3 STS-1 (STM-0/AU3) #1 and STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #3 streams. The TPAIS must be set high during the above time-slots in consecutive TPAIS frames for continuous path/DS3 AIS assertion. Path/DS3 AIS assertion of a stream is removed when the corresponding TPAIS time-slot is set low. DS3 AIS is only transmitted for a particular STS-1 (STM-0/AU3) stream if it carries a DS3 data stream. DS3 stream transmission is enabled using the DS3ADDSEL bit in the SPECTRA-622 TPPS Path and DS3 Configuration register.

The time-slot assignment on TPAIS is unrelated to the configuration of the STS (STM) groups in the transmit stream. For a concatenated stream, only the time-slots associated with the equivalent STS-1 (STM-0/AU3) #1 can be used. TPAIS

must be set low during the time-slots for the remaining STS-1 (STM-0/AU3) equivalent streams in the concatenated stream.

16 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 25 -Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +4.6V
Bias Voltage (V_{BIAS})	(V_{DD} - .3) to +5.5V
Voltage on PECL or 5V tolerant pin	-0.3V to V_{BIAS}+0.3V
Voltage on any non 5V tolerant digital pin	-0.3V to V_{VDD}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

Note: The not 5V tolerante pins are: DC1JV1[4:1], DD[31:0], DDP[4:1], DPL[4:1], PGMRCLK, PGMTCLK, RCLK, TC1J1V1/TFPO, TCLK, TD[7:0], TDP, TPL. All other outputs and inputs are 5 volt tolerant.

17 D.C. CHARACTERISTICS

T_a = -40°C to +85°C, V_{DD} = 3.3V ± 5%, V_{DD} < BIAS < 5.5V
(Typical Conditions: T_a = 25°C, V_{DD} = 3.3V, V_{BIAS} = 5V)

Table 26 -D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	**Power Supply**	**3.14**	**3.3**	**3.47**	**Volts**	
BIAS	**5V Tolerant Bias**	**VDD**	**5.0**	**5.5**	**Volts**	
V_{IL}	**Input Low Voltage**	**0**	**1.2**	**0.8**	**Volts**	**Guaranteed Input Low voltage.**
V_{IH}	**Input High Voltage**	**2.0**			**Volts**	**Guaranteed Input High voltage.**
V_{OL}	**Output or Bi-directional Low Voltage**		**0.2**	**0.4**	**Volts**	**Guaranteed output Low voltage at VDD=3.13V and I_{OL}=maximum rated for pad.**
V_{OH}	**Output or Bi-directional High Voltage**	**2.4**	**2.6**		**Volts**	**Guaranteed output High voltage at VDD=3.13V and I_{OH}=maximum rated current for pad.**
V_{T+}	**Reset Input High Voltage**	**2.0**			**Volts**	**Applies to RSTB and TRSTB only.**
V_{T-}	**Reset Input Low Voltage**			**0.8**	**Volts**	**Applies to RSTB and TRSTB only.**
V_{TH}	**Reset Input Hysteresis Voltage**		**0.3**		**Volts**	**Applies to RSTB and TRSTB only.**
V_{PECLI-}	**Input PECL Low Differential Voltage**	VPECL - 1.810	VPECL - 1.700	VPECL - 1.470	**Volts**	**Applies to PECL inputs REFCLK+/-, RXD+/-, RRCLK+/- only.**

V_{PECLI+}	**Input PECL High Differential Voltage**	V_{PECL} - 1.165	V_{PECL} - 0.955	V_{PECL} -0.880	**Volts**	**Applies to PECL inputs REFCLK+/-, RXD+/-, RRCLK+/- only.**
$V_{PECLICM}$	**Input PECL Common Mode**	V_{PECL} - 1.490	V_{PECL} - 1.329	V_{PECL} - 1.180		
V_{PECLO-}	**Output PECL Low Differential Voltage**	V_{PECL} - 1.620	V_{PECL} - 1.705	V_{PECL} - 1.810	**Volts**	**Applies to PECL outputs TXD+/- only.**
V_{PECLO+}	**Output PECL High Differential Voltage**	V_{PECL} - 0.880	V_{PECL} - 0.955	V_{PECL} - 1.025	**Volts**	**Applies to PECL outputs TXD+/- only.**
I_{ILPU}	**Input Low Current**	**-100**	**-50**	**-4**	**µA**	**V_{IL} = GND. Notes 1 and 3.**
I_{IHPU}	**Input High Current**	**-10**	**0**	**+10**	**µA**	**V_{IH} = V_{DD}. Notes 1 and 3.**
I_{IL}	**Input Low Current**	**-10**	**0**	**+10**	**µA**	**V_{IL} = GND. Notes 2 and 3.**
I_{IH}	**Input High Current**	**-10**	**0**	**+10**	**µA**	**V_{IH} = V_{DD}. Notes 2 and 3.**
C_{IN}	**Input Capacitance**		**5**		**pF**	**t_A=25°C, f = 1 MHz**
C_{OUT}	**Output Capacitance**		**5**		**pF**	**t_A=25°C, f = 1 MHz**
C_{IO}	**Bi-directional Capacitance**		**5**		**pF**	**t_A=25°C, f = 1 MHz**
I_{DDOP1}	**Typical Serial Utilization in 80MHz. See Case1 in Note**		**860**	**940**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**
I_{DDOP2}	**Typical Paralle Utilization in 80MHZ. See Case2 in Note**		**860**	**940**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**

I_{DDOP3}	**Maxinum Utilization in 80MHz. See Case3 in Note**		**990**	**1140**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**
I_{DDOP4}	**Typical Serial Utilization in 20MHz . See Case4 in Note**		**920**	**990**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**
I_{DDOP5}	**Typical Parallel Utilization in 20MHz. See Case5 in Note**		**930**	**1000**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**
I_{DDOP6}	**Maxinum Utilization in 20MHz. See Case6 in Note**		**1060**	**1200**	**mA**	$I_{DDOP\ (max)}$,V_{DD} = 3.47V **$I_{DDOP\ (typical)}$,V_{DD} = 3.30V Outputs Unloaded**

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. List of the different configurations used for **I_{DDOP}** measurements

Case	Setup	Freq. (MHz)	ABC IDDQ Mode	ADD BUS		DROP BUS		Output Mode
				DS3	Telecom	DS3	Telecom	
1	**Typical Serial Utilization**	80	OFF	OFF	ON	OFF	ON	SERIAL
2	**Typical Parallel Utilization**	80	OFF	OFF	ON	OFF	ON	PARALLEL
3	**Maxinum Utilization**	80	OFF	OFF	ON	ON	ON	PARALLEL
4	**Typical Serial Utilization**	20	OFF	OFF	ON	OFF	ON	SERIAL

5	**Typical Parallel Utilization**	20	OFF	OFF	ON	OFF	ON	PARALLEL
6	**Maxinum Utilization**	20	OFF	OFF	ON	ON	ON	PARALLEL

18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_a = -40°C to +85°C, V_{DD} = 3.3V ± 5%)

Table 27 - Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tS_{RWB}	RWB to Read Set-up	10		ns
tH_{RWB}	RWB to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High		50	ns

Figure 82 - Microprocessor Interface Read Access Timing (Intel Mode)

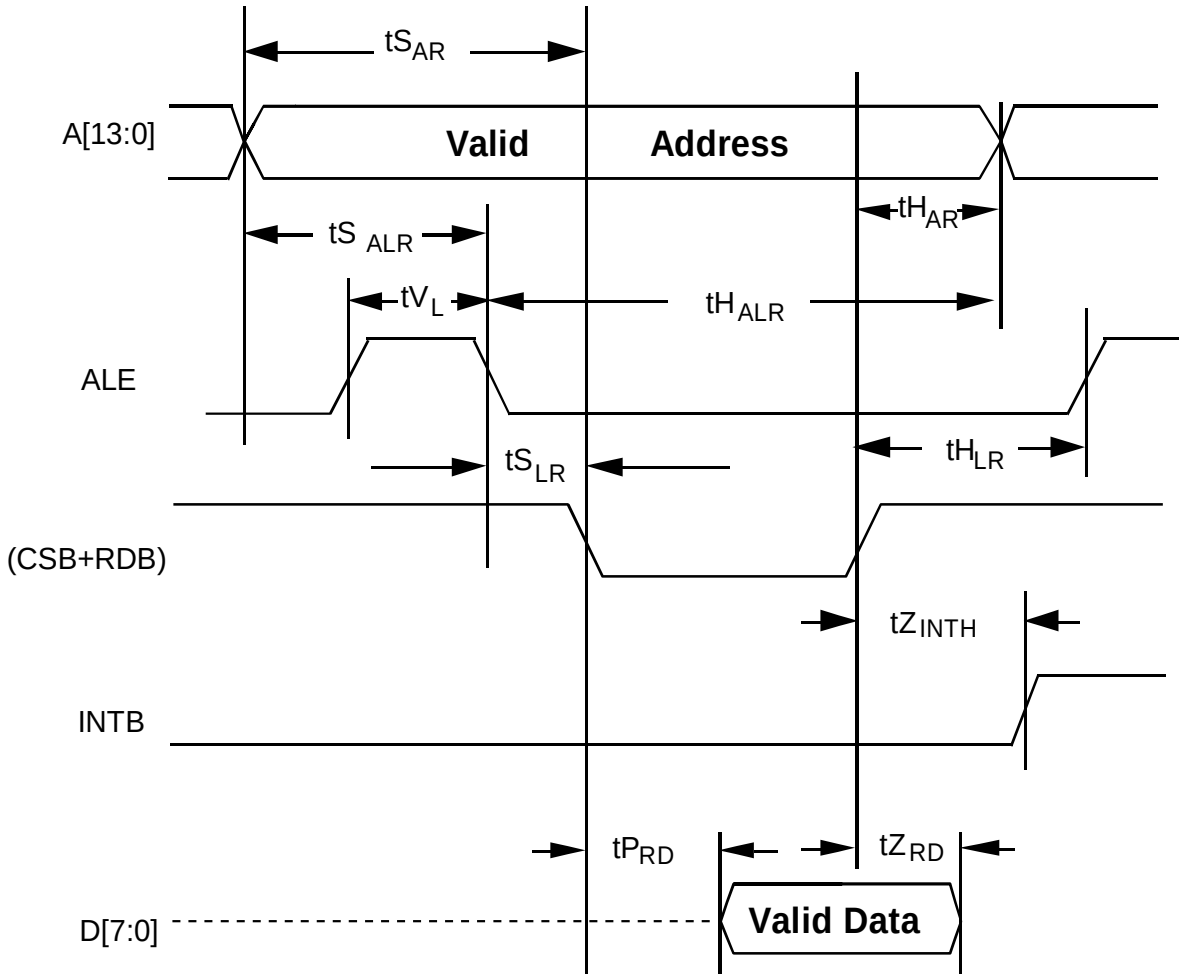
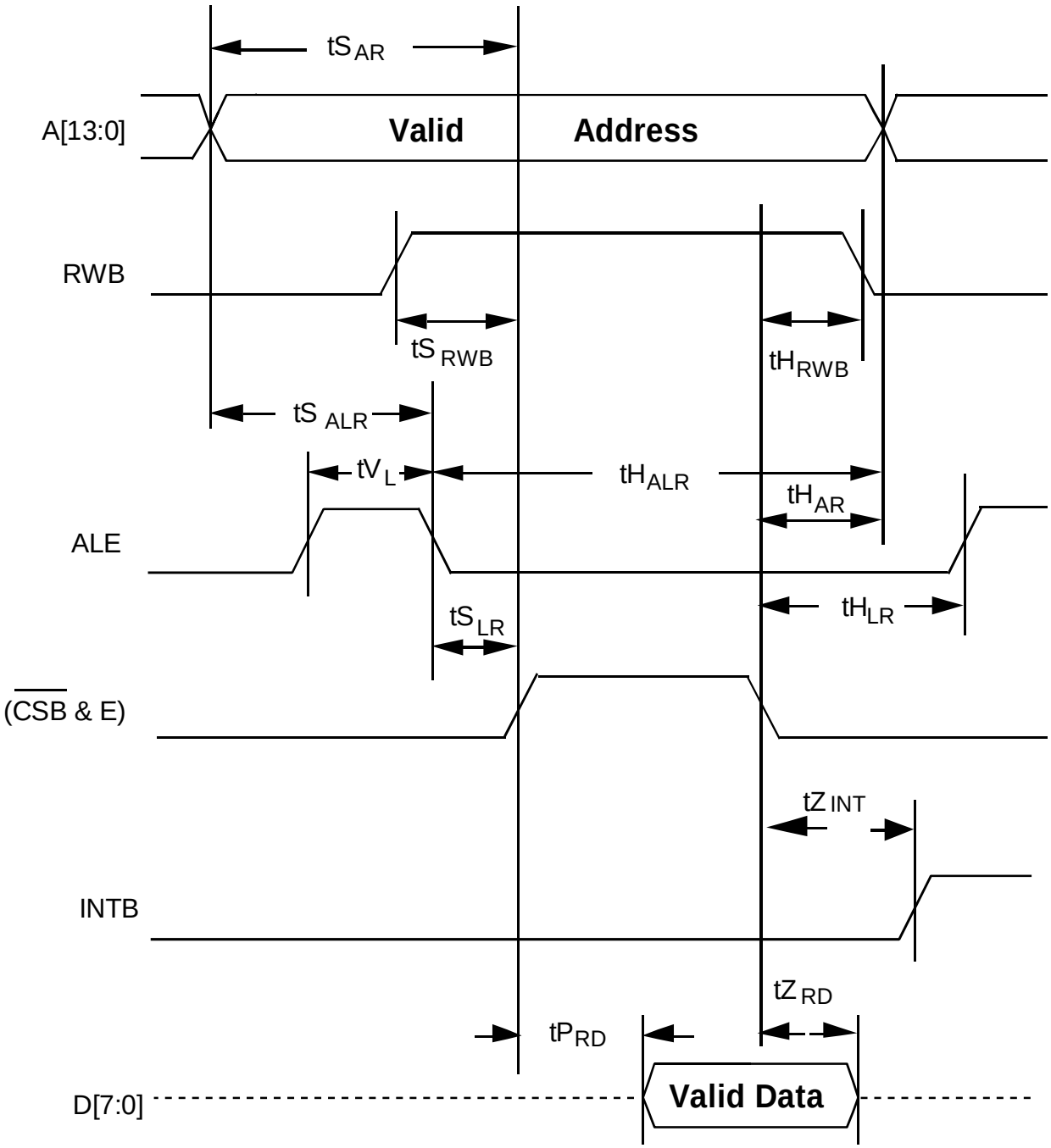


Figure 83 - Microprocessor Interface Read Access Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RWB signal and the inverted CSB signal.

5. Microprocessor Interface timing applies to normal mode register accesses only.

6. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

7. Parameter tH_{AR} and tS_{AR} are not applicable if address latching is used.

8. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

9. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 28 - Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tS_{RWB}	RWB to Write Set-up	10		ns
tH_{RWB}	RWB to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 84 - Microprocessor Interface Write Access Timing (Intel Mode)

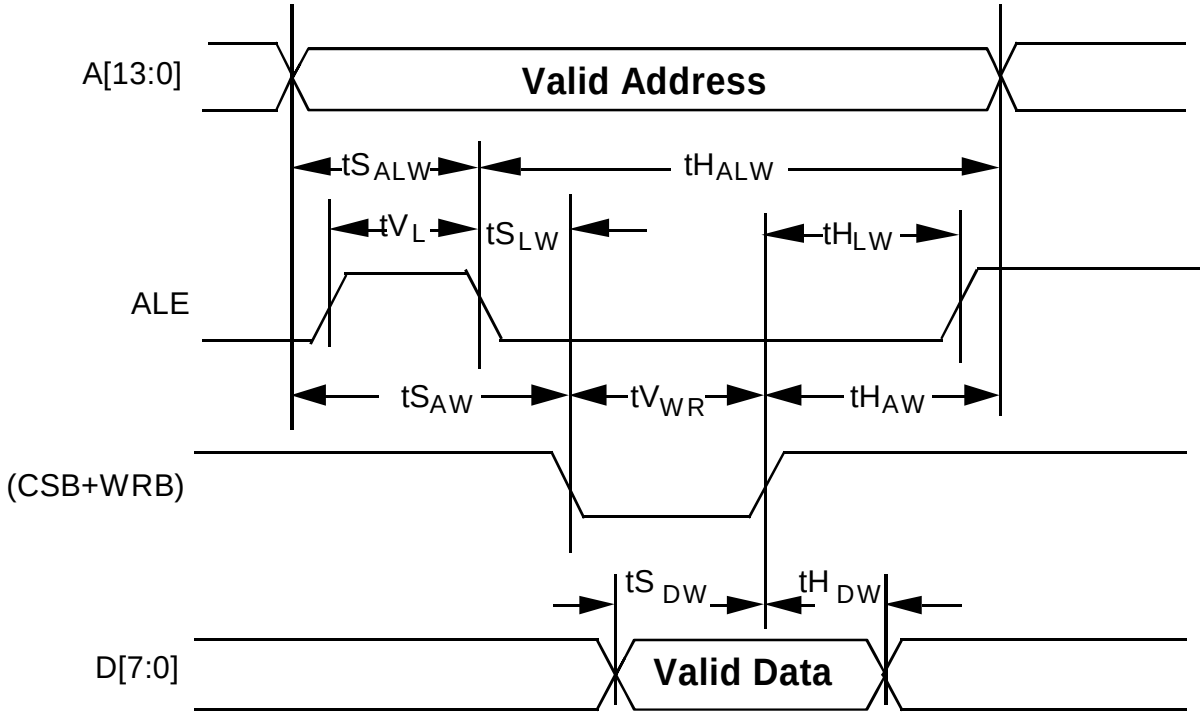
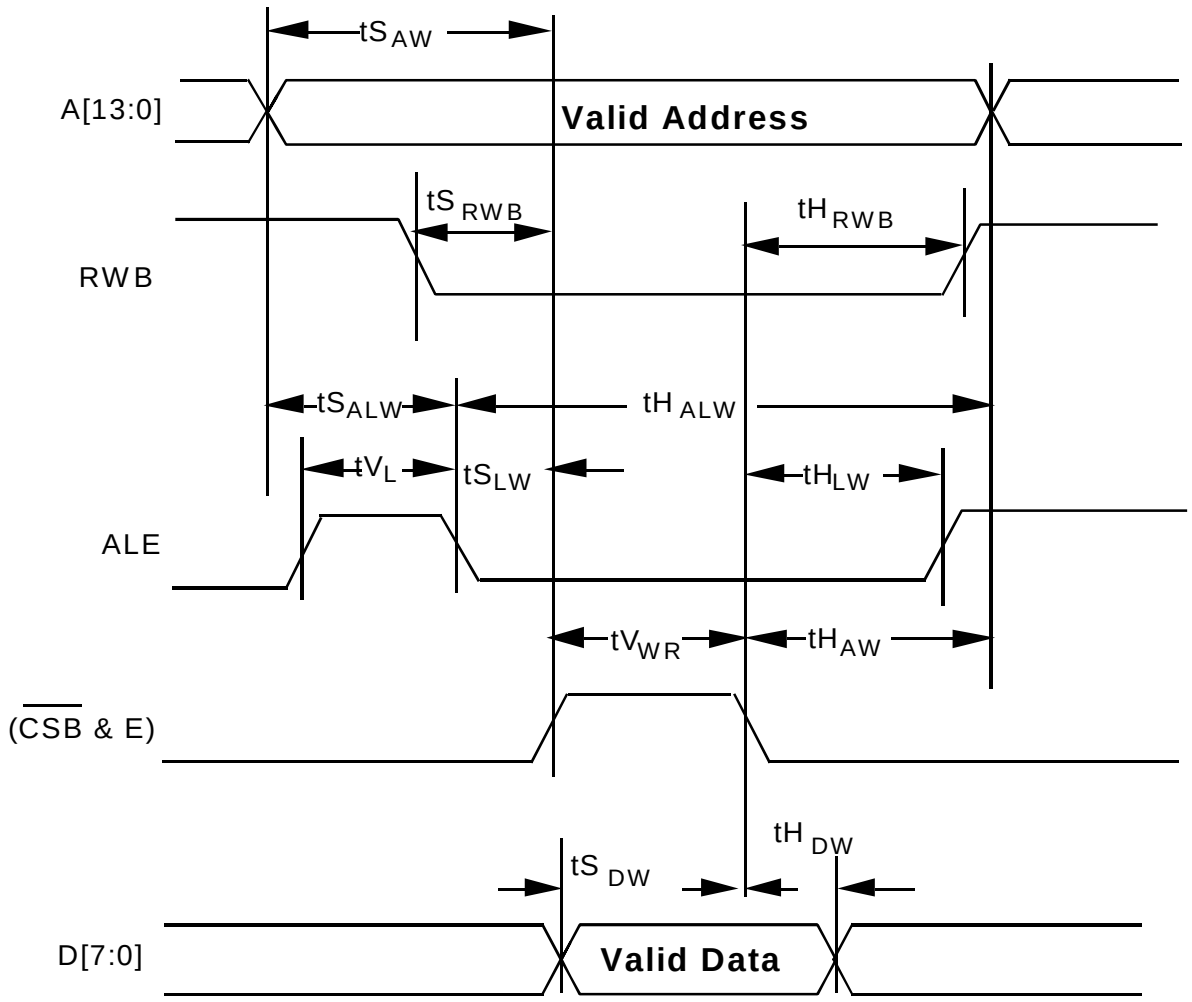


Figure 85 - Microprocessor Interface Write Access Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted RWB signal and the inverted CSB signal.

3. Microprocessor timing applies to normal mode register accesses only.

4. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

5. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

19 A.C. TIMING CHARACTERISTICS

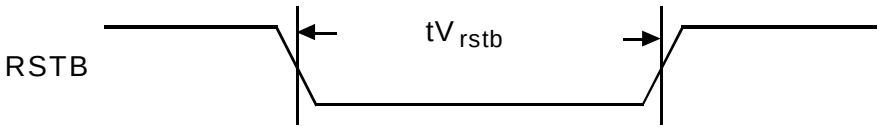
(T_a = -40°C to +85°C, V_{DD} = 3.3V ± 5%)

19.1 System Reset Timing

Table 29 -RSTB Timing

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 86 -RSTB Timing Diagram



19.2 Parallel Line Interface Timing

Table 30 -Transmit Parallel Line Interface Timing

Symbol	Description	Min	Max	Units
f_{TDCK}	TDCK Frequency (nominally 77.76 MHz)	60	80	MHz
D_{TDCK}	TDCK Duty Cycle	40	60	%
tP_{TCH}	TDCK High to TCLK High	2	6	ns
$D_{PGMTCLK}$	PGMTCLK Duty Cycle (PGMTCLK is nominally 77.76 MHz when the TCLKSEL bit in the SPECTRA-622 Clock Control register is set low. When the parallel line interface is enabled, PGMTCLK is a buffered version of TDCK. When the serial line interface is enabled, PGMTCLK is a divide by eight of the transmit line clock.) (PGMTCLK is nominally 19.44 MHz when the TCLKSEL bit is set high. When the parallel line interface is enabled, PGMTCLK is a divide by four of the TDCK. When the serial line interface is enabled, PGMTCLK is a divide by thirty-two of the transmit line clock.)	30	70	%
D_{TCLK}	TCLK Duty Cycle (TCLK is nominally 77.76 MHz. TCLK is a divide by eight of the transmit line clock when the serial line interface is selected. TCLK is a buffered version of TDCK when the parallel line interface is selected.)	30	70	%
tP_{TD}	TCLK High to TD[7:0] Valid	-0.5	3.5	ns
tP_{TPL}	TCLK High to TPL Valid	-0.5	3.5	ns
tP_{TC1}	TCLK High to TC1J1V1 Valid	-0.5	3.5	ns
tP_{TDP}	TCLK High to TDP Valid	-0.5	3.5	ns
tS_{TFPI}	TFPI setup time wrt TDCK (In Serial mode TFPI is timed w.r.t. TCLK)	3		ns
tH_{TFPI}	TFPI hold time wrt TDCK (In Serial mode TFPI is timed w.r.t. TCLK)	0.5		ns

Figure 87 -Transmit Parallel Line Interface Timing Diagram

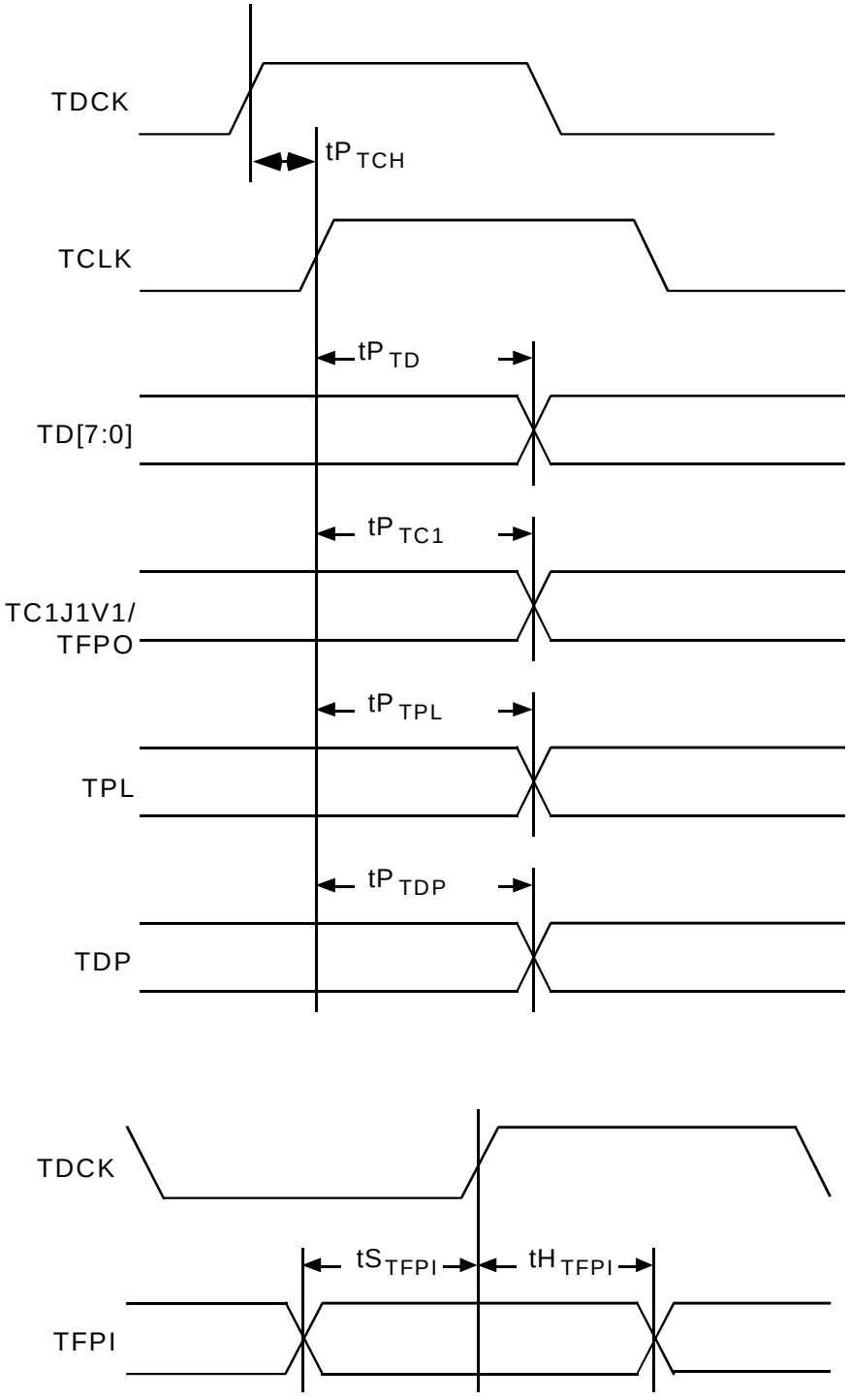
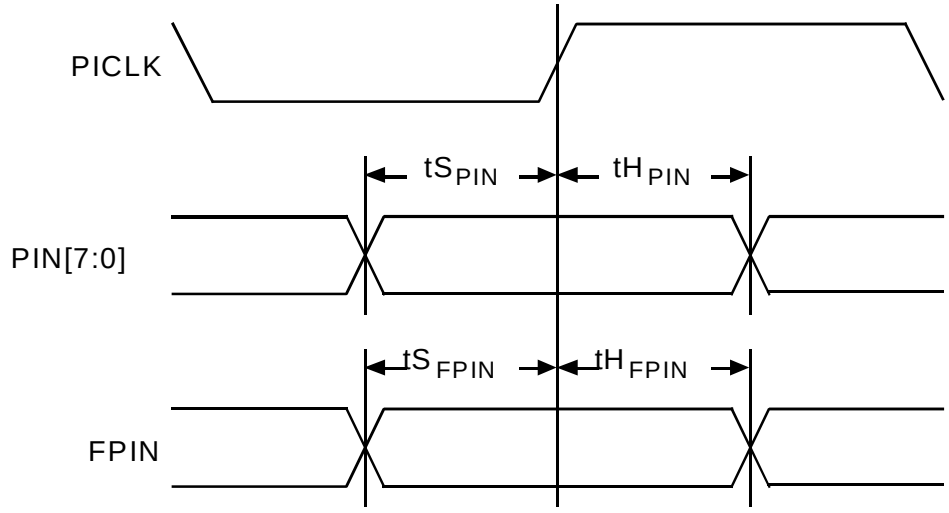


Table 31 -Receive Parallel Line Interface Timing

Symbol	Description	Min	Max	Units
f_{PICLK}	PICLK Frequency		77.76	MHz
D_{PICLK}	PICLK Duty Cycle	40	60	%
tS_{PIN}	PIN[7:0] Set-up time to PICLK	4.5		ns
tH_{PIN}	PIN[7:0] Hold time to PICLK	0		ns
tS_{FPIN}	FPIN Set-up time to PICLK	4.5		ns
tH_{FPIN}	FPIN Hold time to PICLK	0		ns

Figure 88 -Receive Parallel Line Interface Timing Diagram



19.3 Serial Line Interface Timing

Table 32 - Receive Line Side Interface Timing

Symbol	Description	Min	Typ	Max	Units
f_{RRCLK}	RRCLK Frequency		622.04		MHz
	RRCLK Frequency Tolerance†	-20		+20	ppm
D_{RRCLK}	RRCLK Duty Cycle	45		55	%
tS_{RXD}	RXD+/- Set-up time to RRCLK	200			ps
tH_{RXD}	RXD+/- Hold time to RRCLK	800			ps

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET/SDH free run accuracy specification.

Figure 89 - Receive Serial Line side timing

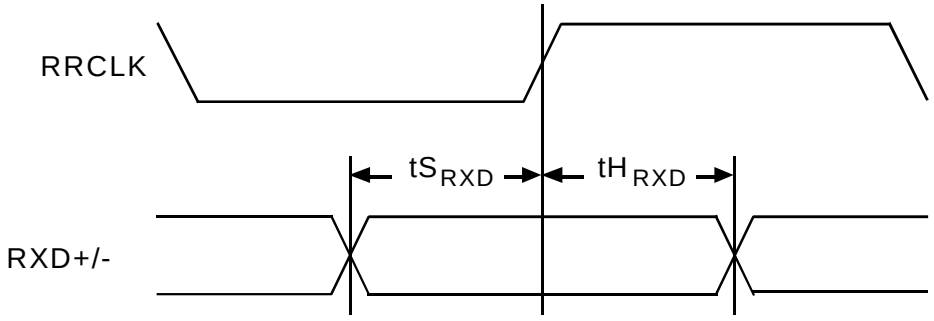


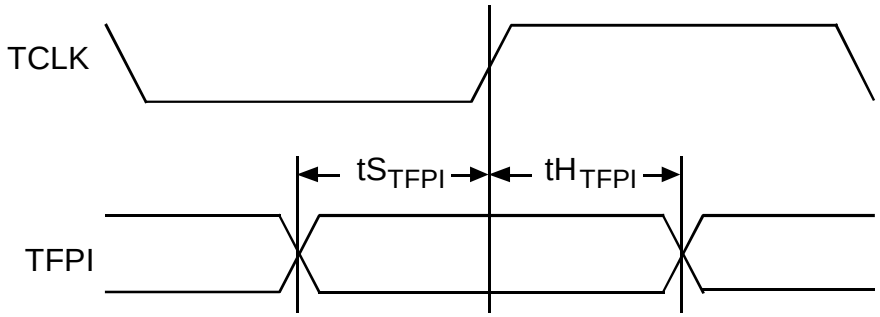
Table 33 - Receive Line Input Interface Timing

Symbol	Description	Min	Max	Units
f_{REFCLK}	REFCLK +/- Frequency		77.76	Mhz
D_{REFCLK}	REFCLK+/- Duty Cycle	45	55	%
	REFCLK+/- Frequency Tolerance†	-20	+20	ppm

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET/SDH free run accuracy specification.

Symbol	Description	Min	Max	Units
tS_{TFPI}	TFPI setup time wrt TCLK (In Parallel mode TFPI is timed w.r.t. TDCK)	5		ns
tH_{TFPI}	TFPI hold time wrt TCLK (In Parallel mode TFPI is timed w.r.t. TDCK)	0		ns

Figure 90 - Serial Transmit interface TFPI timing



19.4 Receive Timing

Table 34 - Receive Line Output Timing

Symbol	Description	Min	Max	Units
D_{RCLK}	RCLK Duty Cycle (RCLK is nominally 77.76 MHz. RCLK is a divide by eight of the receive line clock.)	30	70	%
$D_{PGMRCLK}$	PGMRCLK Duty Cycle (PGMRCLK is nominally 77.76 MHz when the RCLKSEL bit in the SPECTRA-622 Clock Control register is set low. PGMRCLK is a divide by eight of the receive line clock.) (PGMRCLK is nominally 19.44 MHz when the RCLKSEL bit is set high. PGMRCLK is a divide by thirty-two of the receive line clock.)	30	70	%
tP_{RFPO}	RCLK High to RFPO Valid Prop Delay	-1	5	ns
tP_{RLD}	RLDCLK Low to RLD Valid Prop Delay	-20	20	ns
tP_{RSLD}	RSLDCLK Low to RSLD Valid Prop Delay	-20	20	ns
tP_{ROW}	ROWCLK Low to RSOW, RSUC, RLOW Valid Prop Delay	-400	+400	ns
tP_{ROH}	ROHCLK Low to ROH Valid Prop Delay	-400	400	ns
tP_{RTOH}	RTOHCLK Low to RTOH and RTOHFP Valid Prop Delay	-5	10	ns

Figure 91 - Receive Line Output Timing

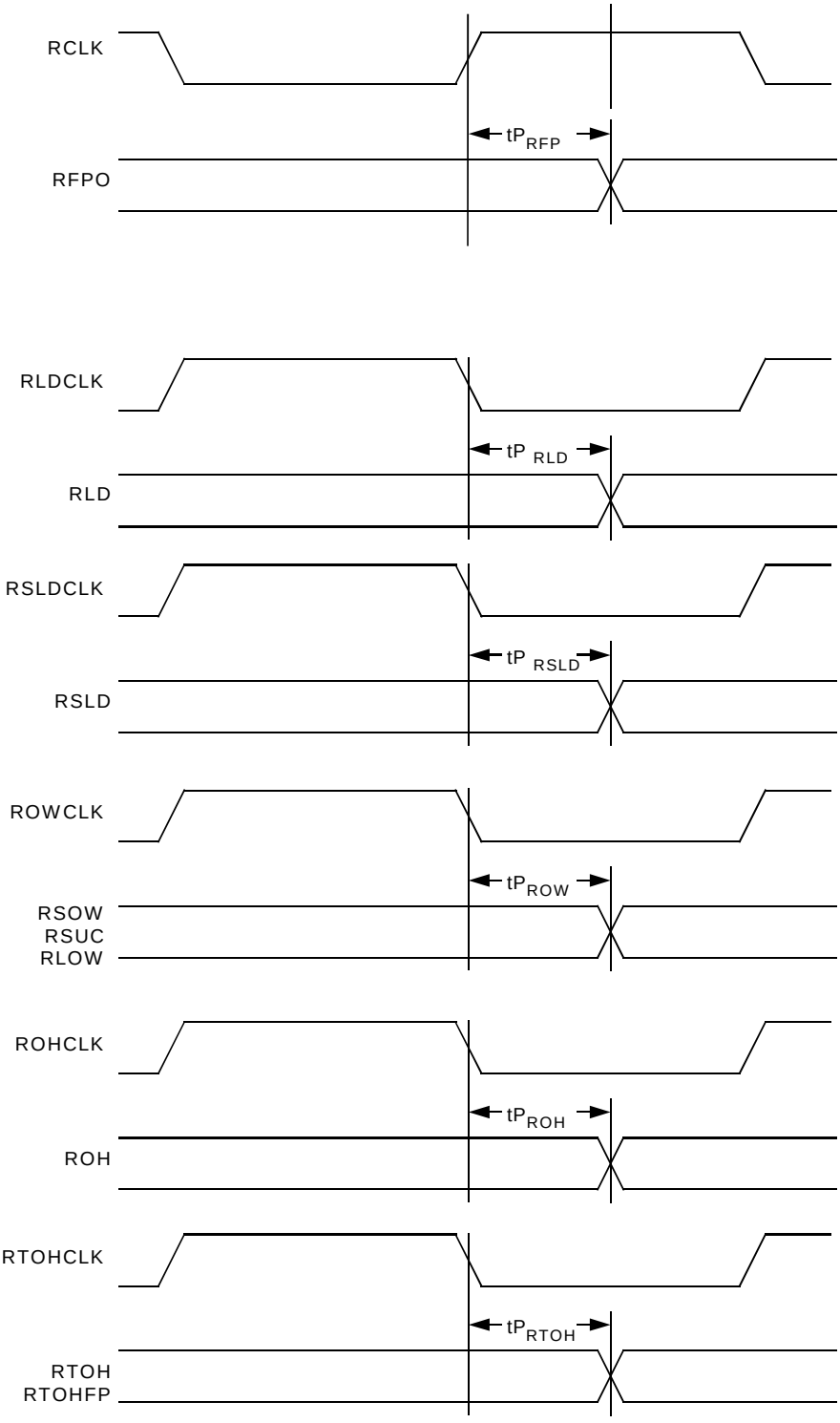


Table 35 - Receive Path Overhead and Alarm Port Output Timing

Symbol	Parameter	Min	Max	Units
$D_{RPOHCLK}$	RPOHCLK Duty Cycle (RPOHCLK is nominally a 12.92 Mhz clock)	45	55	%
tP_{RPOHFP}	RPOHCLK Low to RPOHFP Valid	-5	15	ns
tP_{RPOH}	RPOHCLK Low to RPOH Valid	-5	15	ns
tP_{RPOHEN}	RPOHCLK Low to RPOHEN Valid	-5	15	ns
tP_{B3E}	RPOHCLK Low to B3E Valid	-5	15	ns
tP_{RAD}	RPOHCLK Low to RAD Valid	-5	15	ns
tP_{RALM}	RPOHCLK Low to RALM Valid	-5	15	ns

Figure 92 - Receive Path Overhead and Alarm Port Output Timing

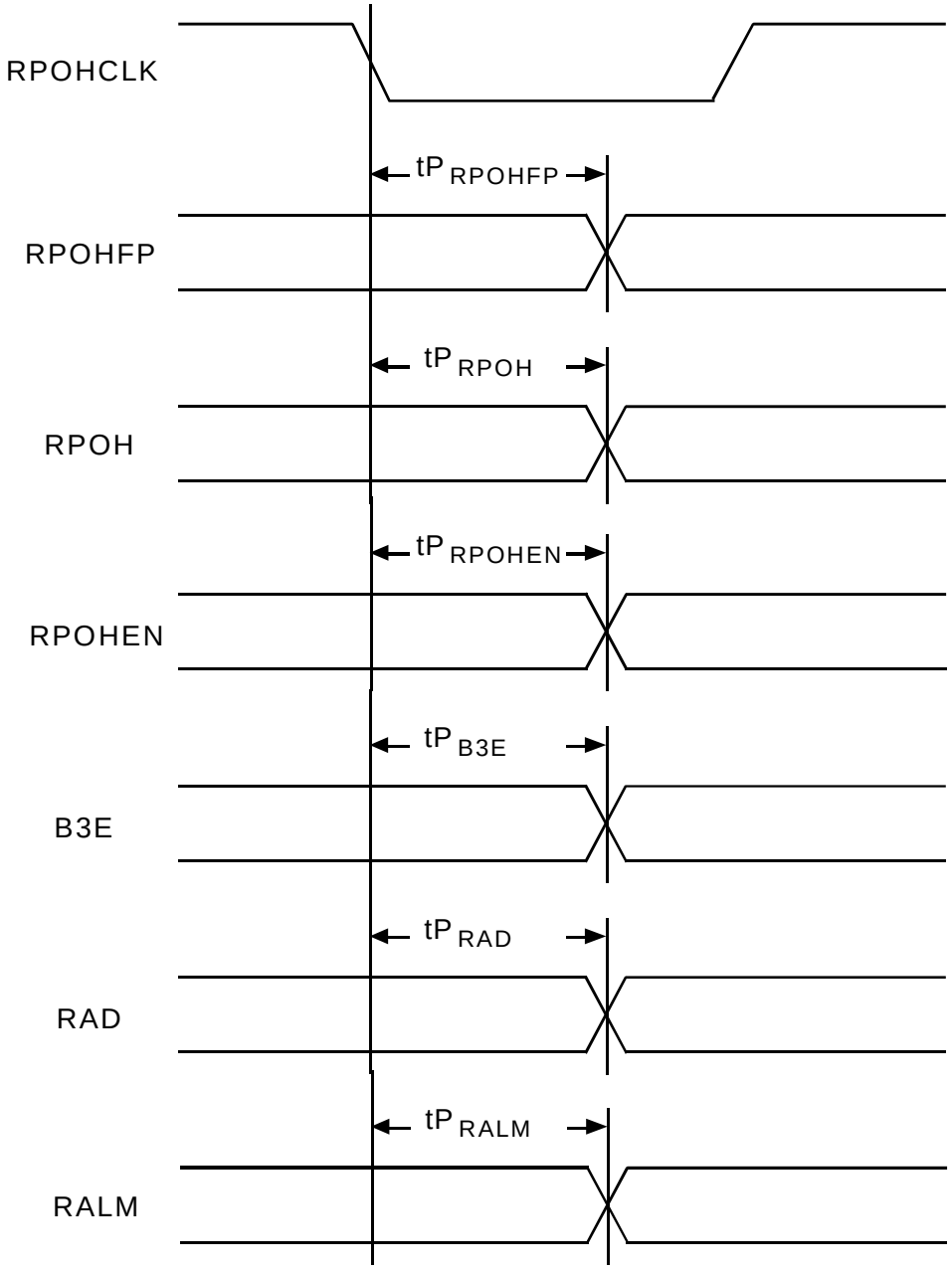
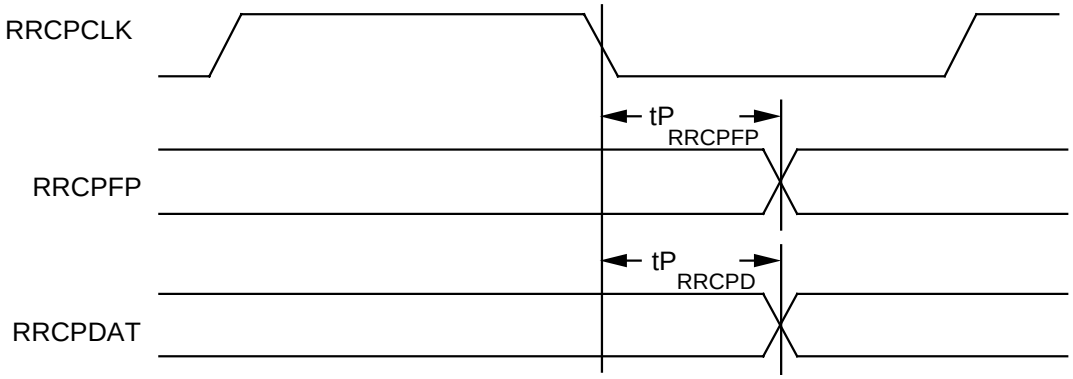


Table 36 - Receive Ring Control Port Output Timing

Symbol	Description	Min	Max	Units
tP_{RRCPFP}	RRCPCLK Low to RRCPFP Valid Prop Delay	-10	10	ns
tP_{RRCPD}	RRCPCLK Low to RRCPDAT Valid Prop Delay	-10	10	ns

Figure 93 - Ring Control Port Output Timing



DROP Bus Timing

Table 38 - Telecom DROP Bus Input Timing

Symbol	Parameter	Min	Max	Units
f_{DCK}	DCK Freq. (Nominally 19.44MHz)		20	MHz
f_{DCK}	DCK Freq. (Nominally 77.76 MHz) (DCK must not be gapped)	60	80	MHz
D_{DCK}	DCK Duty Cycle	40	60	%
tS_{DFP}	DFP Set-up Time	3		ns
tH_{DFP}	DFP Hold Time	0		ns

Figure 95 - Telecom DROP Bus Input Timing

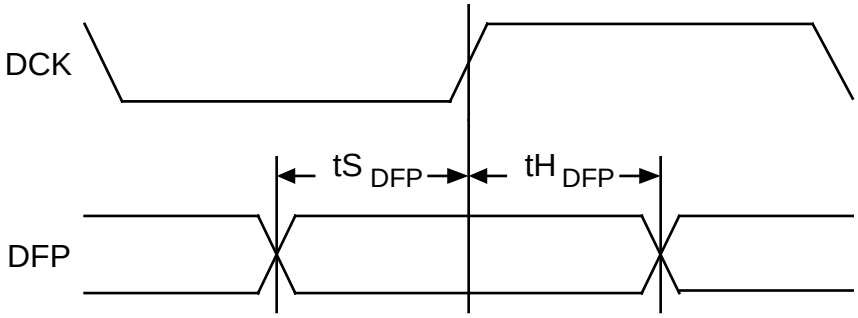


Table 39 - Telecom DROP Bus Output Timing at 77.76 Mhz DCK

Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0] Valid	1	6.5	ns
tP_{DC1}	DCK High to DC1J1V1[1] Valid	1	6.5	ns
tP_{DPL}	DCK High to DPL[1] Valid	1	6.5	ns
tP_{DDP}	DCK High to DDP[1] Valid	1	6.5	ns

Table 40- Telecom DROP Bus Output Timing at 19.44 Mhz DCK

Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0], DD[15:8], DD[23:16], DD[31:24] Valid	4	15	ns
tP_{DC1}	DCK High to DC1J1V1[4:1] Valid	4	15	ns
tP_{DPL}	DCK High to DPL[4:1] Valid	4	15	ns
tP_{DDP}	DCK High to DDP[4:1] Valid	4	15	ns

Figure 96 - Telecom DROP Bus Output Timing

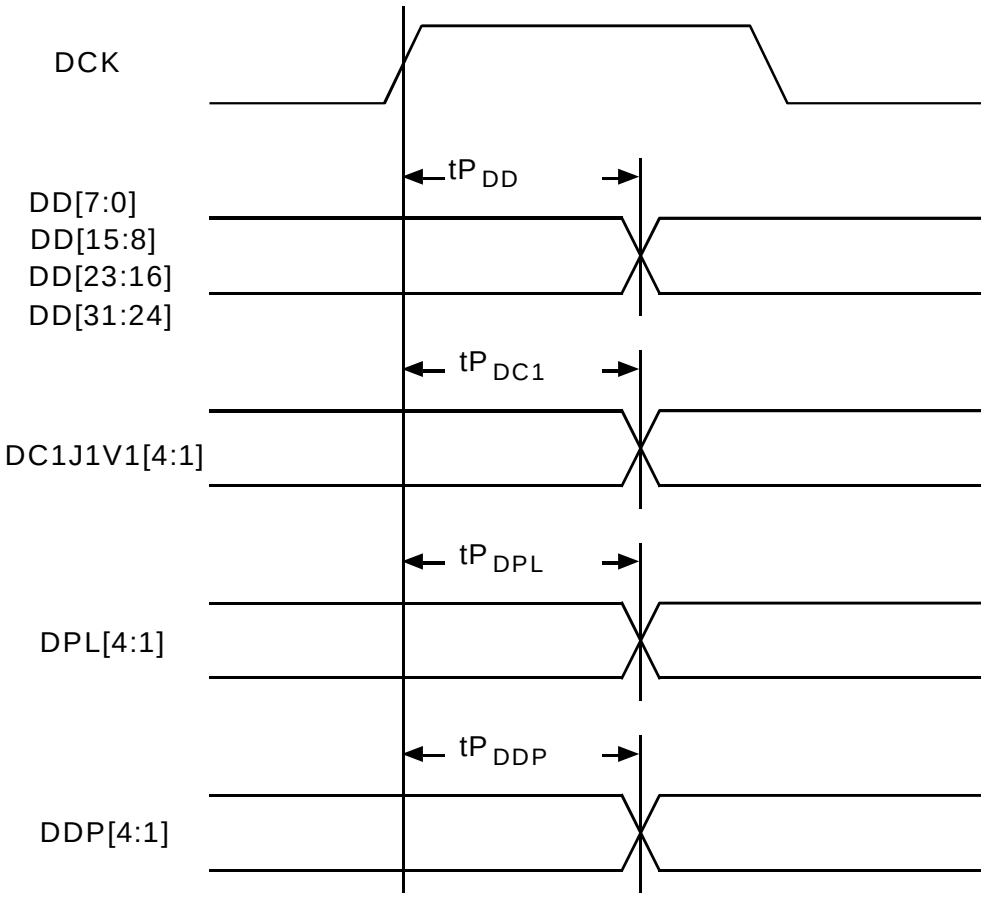


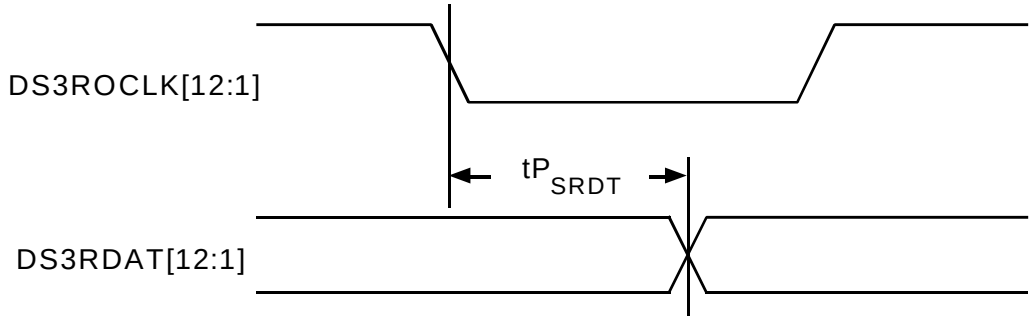
Table 41 - DS3 DROP Interface Input Timing

Symbol	Parameter	Min	Max	Units
$f_{DS3RICLK}$	DS3RICLK Freq. When used, the DS3RICLK input must be connected to a clock reference source which has a frequency of 44.928 MHz.	-100	+100	ppm
$D_{DS3RICLK}$	DS3RICLK Duty Cycle	40	60	%

Table 42 - DS3 DROP Interface Output Timing

Symbol	Parameter	Min	Max	Units
$f_{DS3ROCLK}$	DS3ROCLK[12:1] DS3ROCLK is nominally 44.736 MHz. DS3ROCLK is generated by gapping DS3RICLK when the DS3_SEL52 bit in the SPECTRA-622 RPPS Path and DS3 Configuration register is set low. DS3ROCLK is generated by gapping an internal 51.84 MHz clock when the DS3_SEL52 bit is set high.	-	-	MHz
$D_{DS3ROCLK}$	DS3ROCLK[12:1] Duty Cycle (for consecutive transitions of the gapped clock)	40	60	%
tP_{SRDT}	DS3ROCLK[12:1] Low to DS3RDAT[12:1] Valid	-2	6	ns

Figure 97 - DS3 DROP Interface Output Timing



19.6 Path AIS Input Timing

Table 43 - System DROP-side Path Alarm Input Timing

Symbol	Parameter	Min	Max	Units
$f_{DPAISCK}$	DPAISCK Freq.		20	MHz
$D_{DPAISCK}$	DPAISCK Duty Cycle	40	60	
tS_{DPS}	DPAIS Set-up Time	5		ns
tH_{DPS}	DPAIS Hold Time	5		ns
tS_{DPFP}	DPAISFP Set-up Time	5		ns
tH_{DPFP}	DPAISFP Hold Time	5		ns

Figure 98 - System DROP-side Path Alarm Input Timing

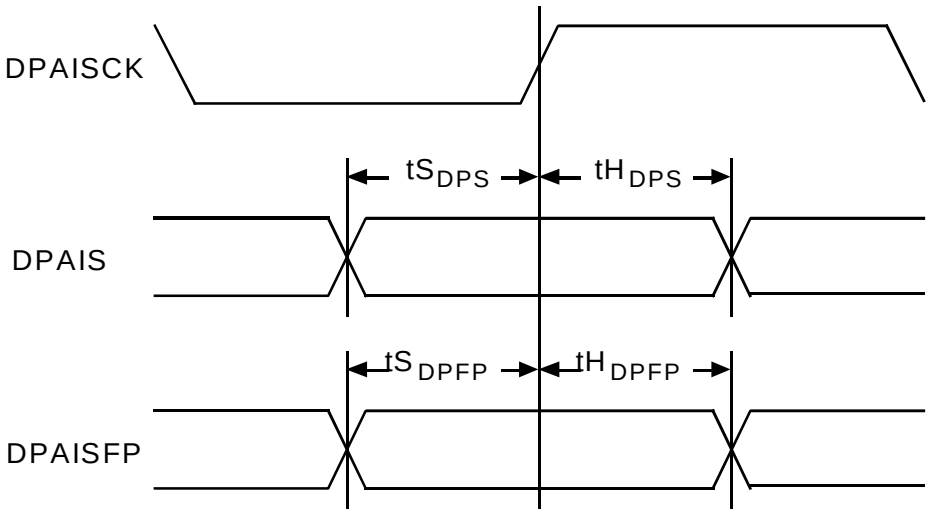
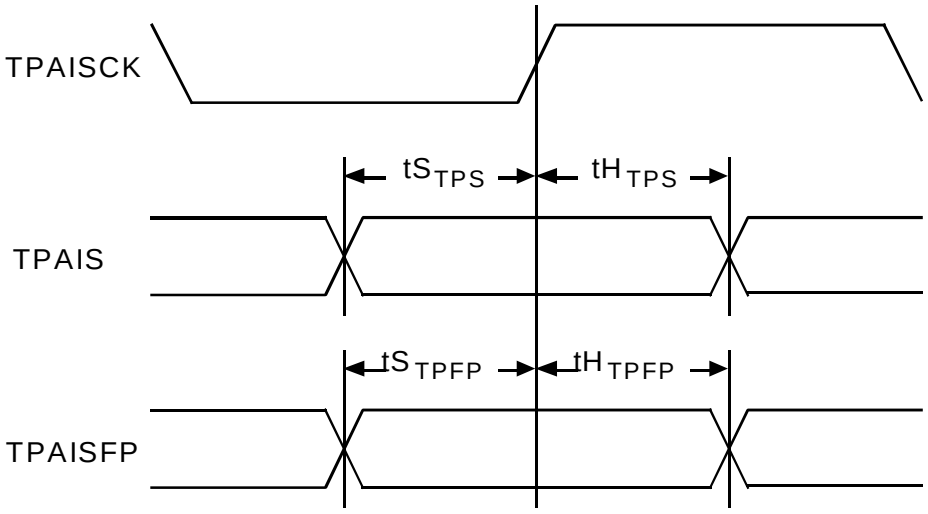


Table 44 - System ADD-side Path Alarm Input Timing

Symbol	Parameter	Min	Max	Units
$f_{TPAISCK}$	TPAISCK Freq.		20	MHz
$D_{TPAISCK}$	TPAISCK Duty Cycle	40	60	
tS_{TPS}	TPAIS Set-up Time	5		ns
tH_{TPS}	TPAIS Hold Time	5		ns
tS_{TPFP}	TPAISFP Set-up Time	5		ns
tH_{TPFP}	TPAISFP Hold Time	5		ns

Figure 99 - System ADD-side Path Alarm Input Timing



19.7 ADD Bus Timing

Table 45 - Telecom ADD Bus Input Timing

Symbol	Parameter	Min	Max	Units
f_{ACK}	ACK Freq. STS-3 (STM-1) Byte Telecom Bus Nominally 19.44 MHz		20	MHz
f_{ACK}	ACK Freq. STS-12 (STM-4) Byte Telecom Bus Nominally 77.76 MHz		80	MHz
D_{ACK}	ACK Duty Cycle	40	60	%
TS_{AD}	AD[7:0], AD[15:8], AD[23:16], AD[31:24] Set-up Time	3.5		ns
TH_{AD}	AD[7:0], AD[15:8], AD[23:16], AD[31:24] Hold Time	1		ns
TS_{AC1}	AC1J1V1[4:1]/AFP[4:1] Set-up Time	3.5		ns
tH_{AC1}	AC1J1V1[4:1]/AFP[4:1] Hold Time	1		ns
tS_{APL}	APL[4:1] Set-up Time	3.5		ns
tH_{APL}	APL[4:1] Hold Time	1		ns
tS_{ADP}	ADP[4:1] Set-up Time	3.5		ns
tH_{ADP}	ADP[4:1] Hold Time	1		ns

Figure 100 - Telecom ADD Bus Input Timing

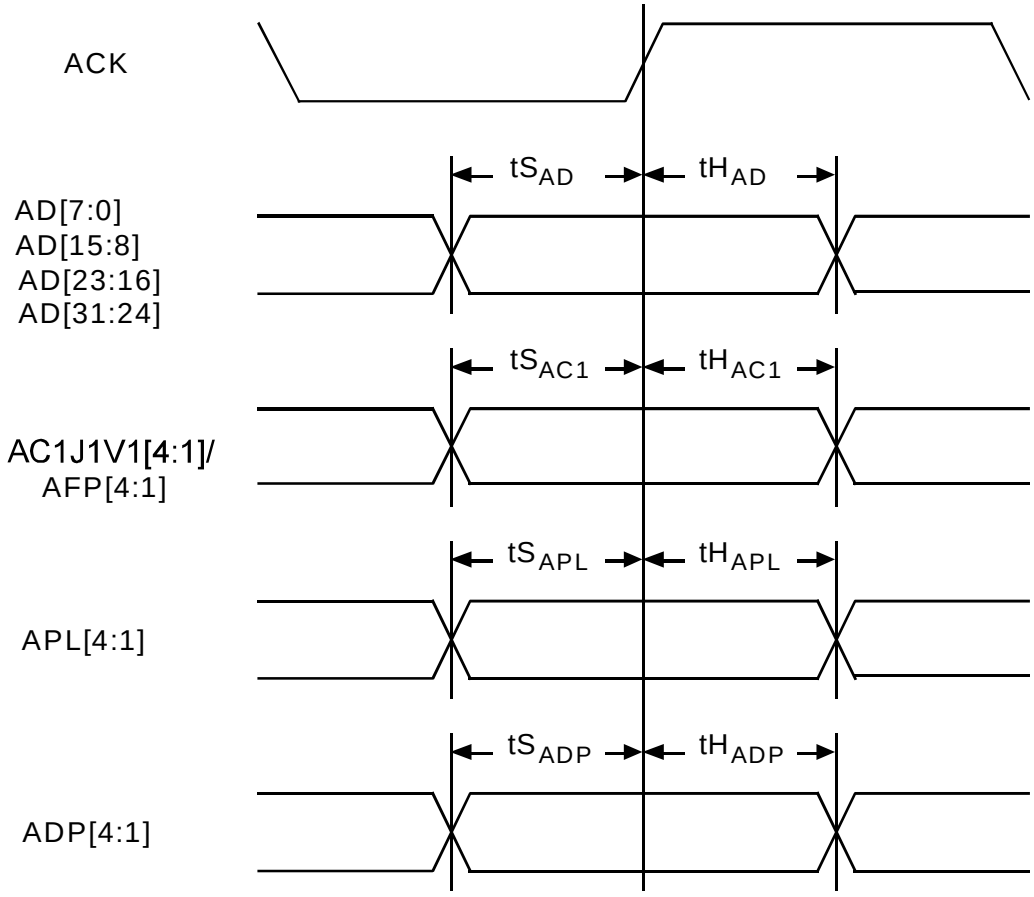
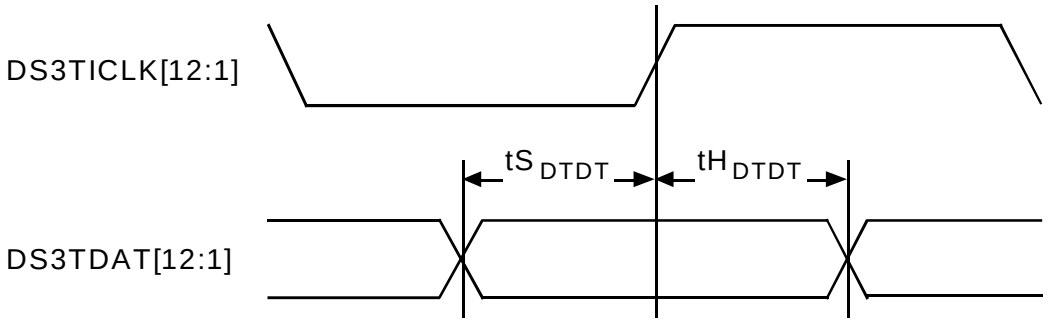


Table 46 - DS3 ADD Interface Input Timing

Symbol	Parameter	Min	Max	Units
$f_{DS3TICLK}$	DS3TICLK[12:1] Freq. 44.736 MHz	-100	+100	ppm
$D_{DS3TICLK}$	DS3TICLK[12:1] Duty Cycle (for consecutive transitions of the gapped clock)	40	60	%
tS_{DTDT}	DS3TDAT[12:1] Set-up Time	2		ns
tH_{DTDT}	DS3TDAT[12:1] Hold Time	3		ns

Figure 101 - DS3 ADD Interface Input Timing (Internal DS3 Framer)



19.8 Transmit Timing

Table 47 - Transmit Path Overhead Input Timing

Symbol	Parameter	Min	Max	Units
TS_{TPOH}	TPOH Set-up Time	15		ns
TH_{TPOH}	TPOH Hold Time	15		ns
TS_{TPEN}	TPOHEN Set-up Time	15		ns
TH_{TPEN}	TPOHEN Hold Time	15		ns

Figure 102 - Transmit Path Overhead Input Timing

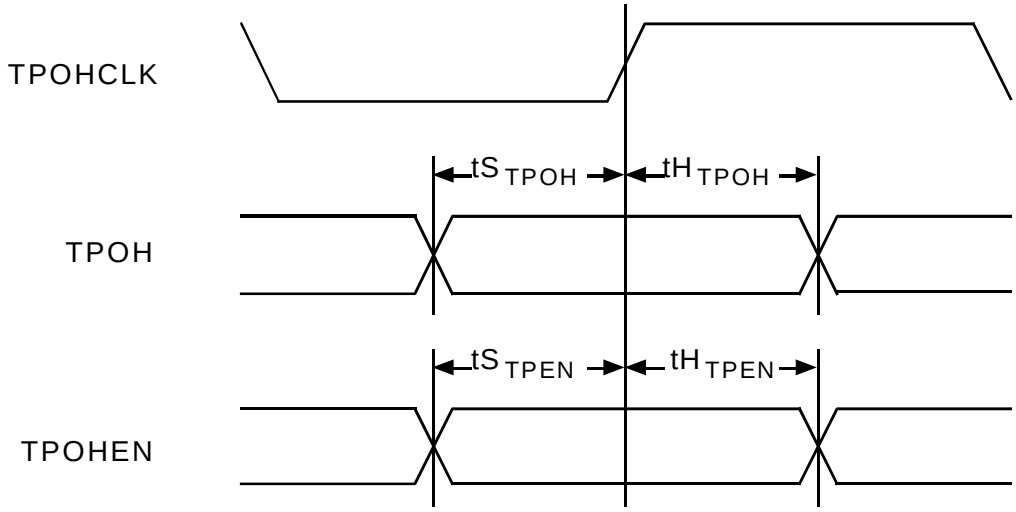


Table 48 - Transmit Alarm Port Input Timing

Symbol	Parameter	Min	Max	Units
f_{TACK}	TACK Frequency	5	15	MHz
D_{TACK}	TACK Duty Cycle	40	60	%
tS_{TAD}	TAD Setup Time	15		ns
tH_{TAD}	TAD Hold Time	15		ns
tS_{TAFP}	TAFP Set-up Time	15		ns
tH_{TAFP}	TAFP Hold Time	15		ns

Figure 103 - Transmit Alarm Port Input Timing

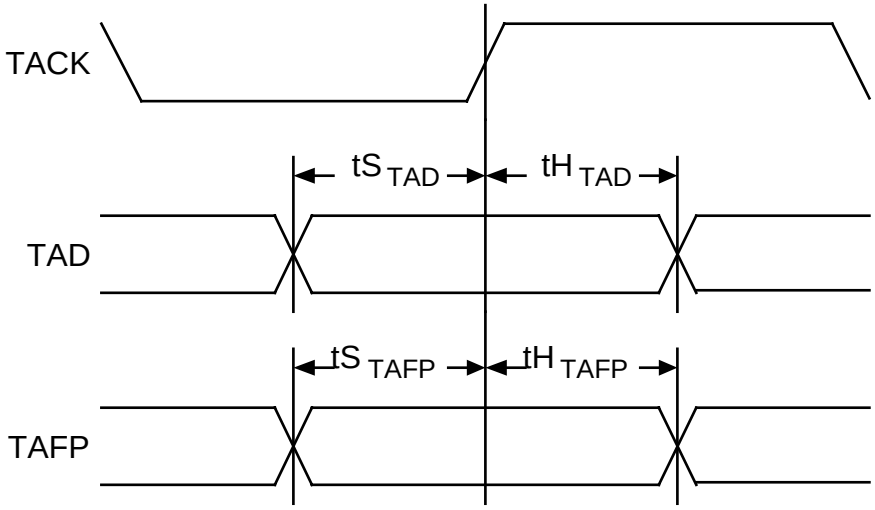


Table 49 - Transmit Transport Overhead Input Timing

Symbol	Description	Min	Max	Units
tS_{TLD}	TLD Set-up Time to TLDCLK	250		ns
tH_{TLD}	TLD Hold Time to TLDCLK	0		ns
tS_{TSLD}	TSLD Set-up Time to TSLDCLK	250		ns
tH_{TSLD}	TSLD Hold Time to TSLDCLK	0		ns
tS_{TOW}	TSOW, TLOW, TSUC Set-up Time to TOWCLK	250		ns
tH_{TOW}	TSOW, TLOW, TSUC Hold Time to TOWCLK	0		ns
tS_{TOH}	TOH Set-up Time to TOHCLK	250		ns
tH_{TOH}	TOH Hold Time to TOHCLK	0		ns
tS_{TTOH}	TTOH, TTOHEN Set-up Time to TTOHCLK	17		ns
tH_{TTOH}	TTOH, TTOHEN Hold Time to TTOHCLK	0		ns

Figure 104 - Transmit Transport Overhead Input Timing

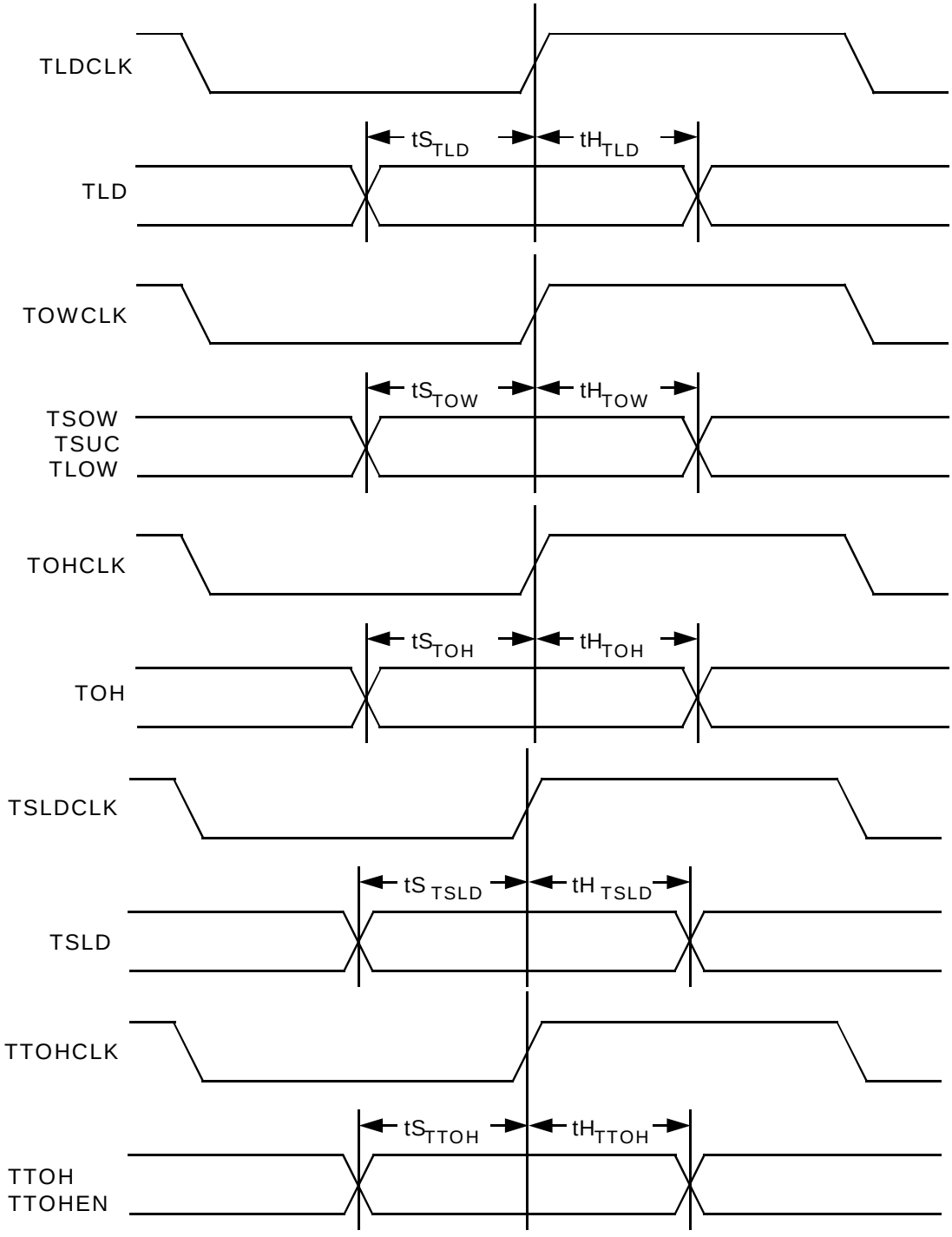


Table 50 - Transmit Ring Control Port Input Timing

Symbol	Description	Min	Max	Units
$f_{TRCPCLK}$	TRCPCLK Frequency (nominally 3.24 MHz)		3.4	MHz
$D_{TRCPCLK}$	TRCPCLK Duty Cycle	33	67	%
tS_{TRCPFP}	TRCPFP Set-up Time to TRCPCLK	10		ns
tH_{TRCPFP}	TRCPFP Hold Time to TRCPCLK	10		ns
tS_{TRCPD}	TRCPDAT Set-up Time to TRCPCLK	10		ns
tH_{TRCPD}	TRCPDAT Hold Time to TRCPCLK	10		ns

Figure 105 - Transmit Ring Control Port Input Timing

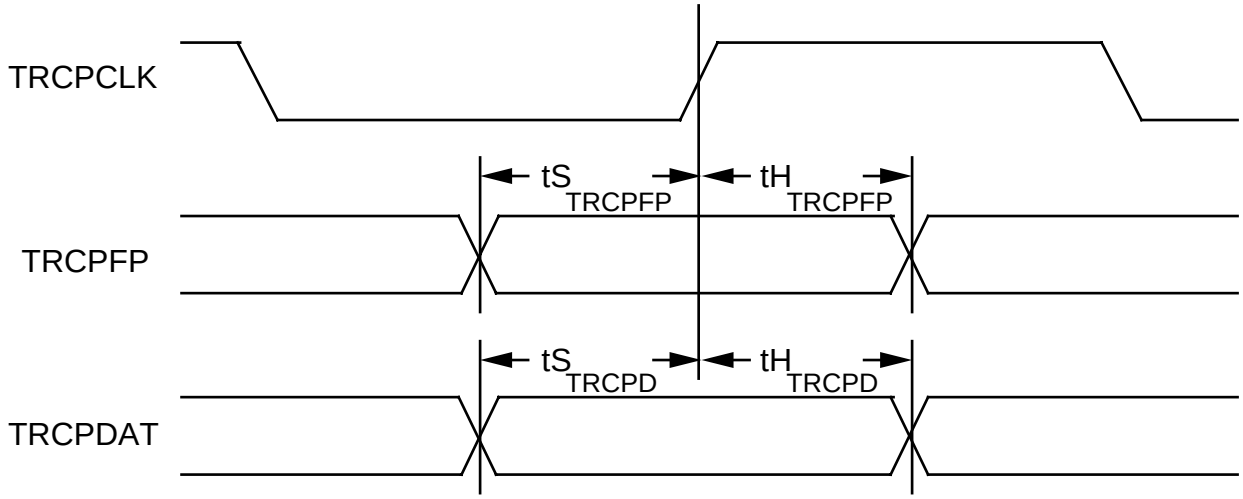
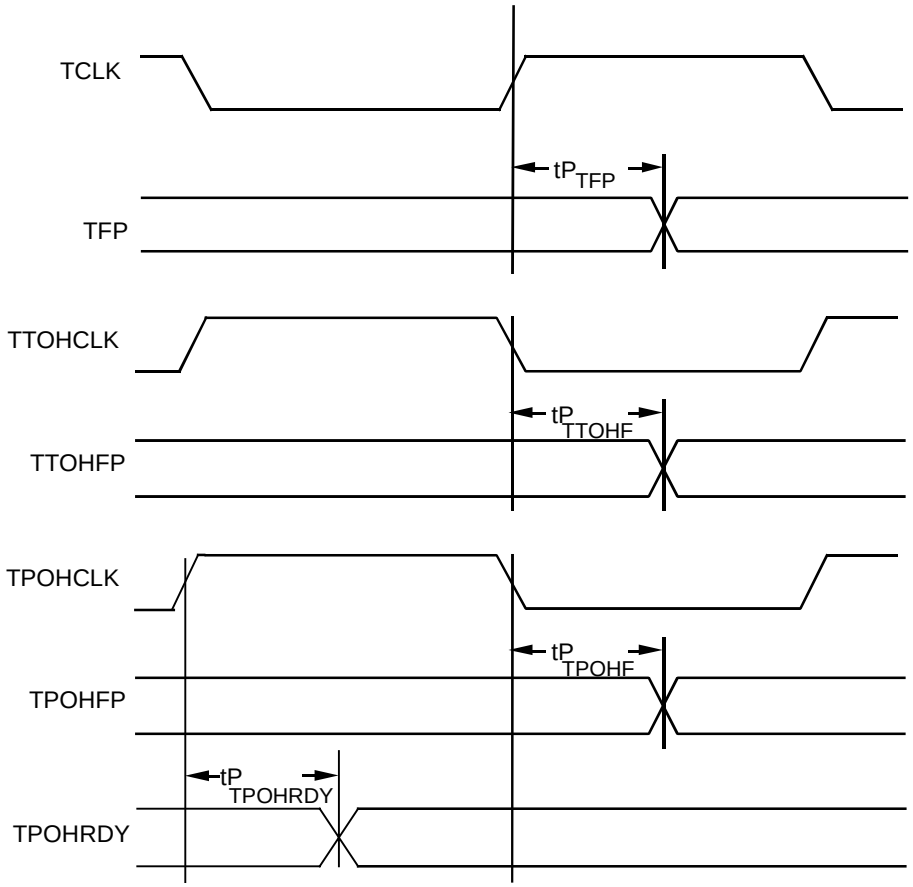


Table 51 - Transmit Overhead Output Timing

Symbol	Description	Min	Max	Units
tP_{TFP}	TCLK High to TFP Valid Prop Delay	-2	7.5	ns
tP_{TTOHFP}	TTOHCLK Low to TTOHFP Valid Prop Delay	-5	10	ns
tP_{TPOHFP}	TPOHCLK Low to TPOHFP Valid	-5	15	ns
$tP_{TPOHRDY}$	TPOHCLK High to TPOHRDY Valid	-5	15	ns

Figure 106 - Transmit Overhead Output Timing

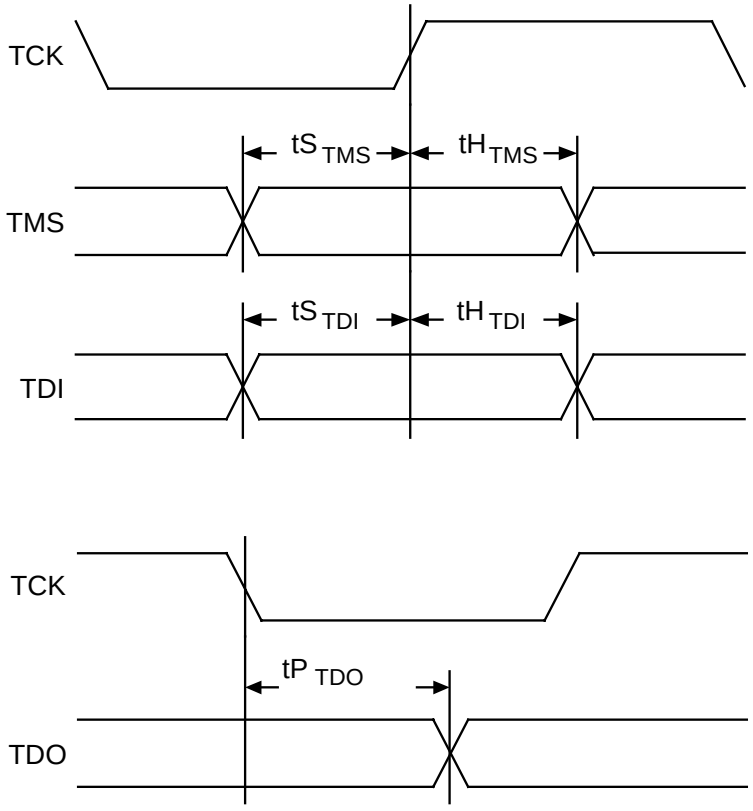


19.9 JTAG Timing

Table 52 - JTAG Port Interface

Symbol	Description	Min	Max	Units
f_{TCK}	TCK Frequency		4	MHz
D_{TCK}	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	65	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 107 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs except where indicated.

20 ORDERING AND THERMAL INFORMATION

Table 53 - Ordering information

PART NO.	DESCRIPTION
PM5313-BI	520 Super Ball Grid Array (SBGA)

Table 54 - Thermal information – Theta Jc

PART NO.	AMBIENT TEMPERATURE	Theta Jc
PM5313-BI	-40°C to 85°C	1 °C/W

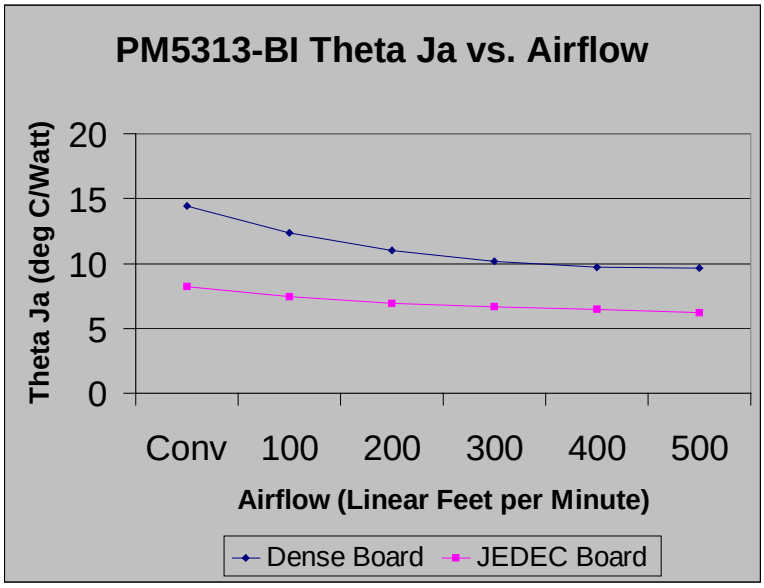
Table 55 - Maximum Junction Temperature

PM5313-BI	Maximum Junction Temperature for Long Term Reliability	105 °C

Table 56 - Thermal information – Theta Ja vs. Airflow

		Forced Air (Linear Feet per Minute)				
Theta Ja @ specified power	Convection	100	200	300	400	500
Dense Board	14.4	12.4	11.0	10.1	9.7	9.7
JEDEC Board	8.2	7.4	7.0	6.7	6.5	6.2

Figure 108 - Theta Ja vs. Airflow Plot



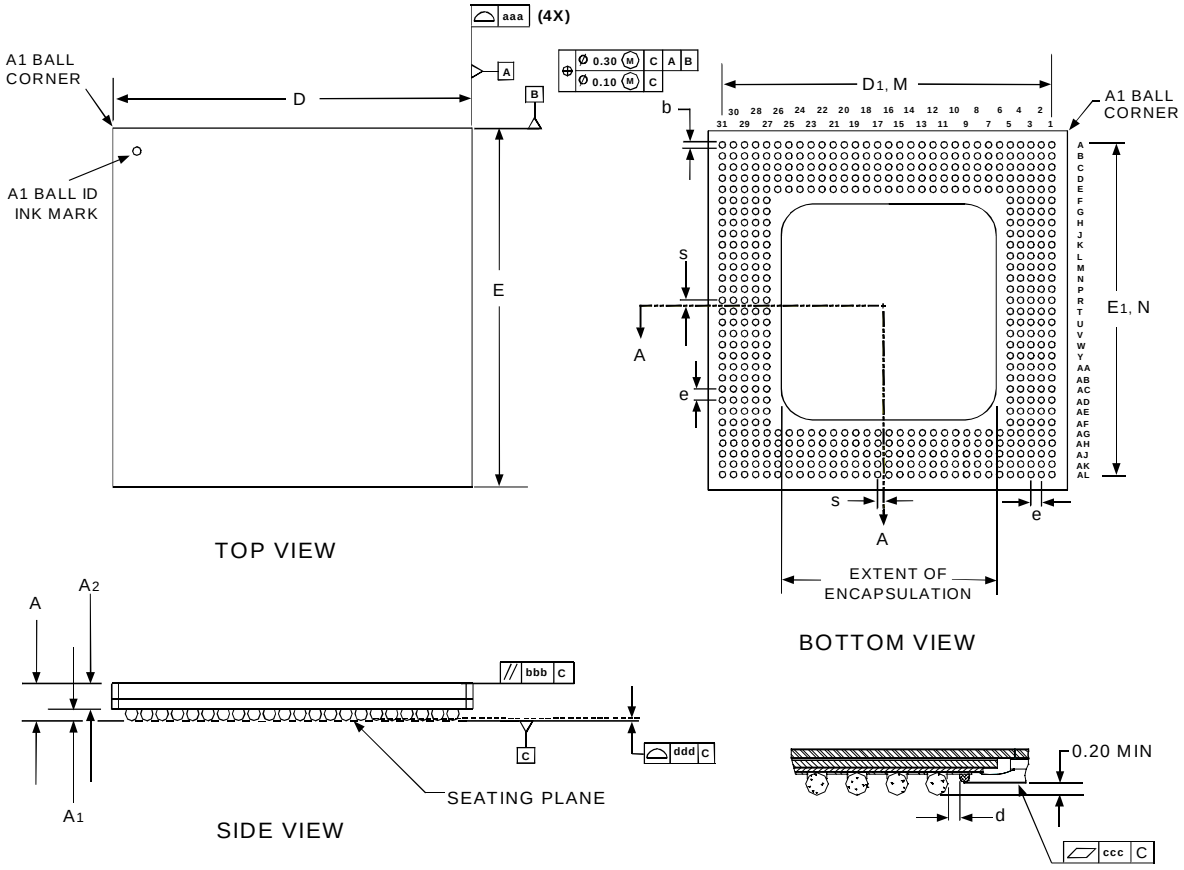
Notes on Theta Ja vs. Airflow:

1. Dense Board – Board with 3x3 array of the same device with spacing of 4mm between device. 6 layer board (3 signal layers, 3 power layers). Chart represents device in the center of the array. Chart represents values obtained through simulation.

2. JEDEC Board – Single component on a board. 4 layer board (2 signal layers, 2 power layers), metallization length x width = 94 mm x 94 mm. Board dimension = 114mmx142mm. JEDEC Measurement as per EIA/GESD51-1.

21 MECHANICAL INFORMATION

Figure 109 - Mechanical Drawing 520 Pin Super Ball Grid Array (SBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 520 THERMALLY ENHANCED BALL GRID ARRAY - SBGA																
BODY SIZE : 40 x 40 x 1.54 MM																
Dim.	A	A1	A2	D	D1	E	E1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.30	0.50	0.80	39.90	38.00	39.90	38.00		0.60	0.5	-	-	-	-		-
Nom.	1.51	0.60	0.91	40.00	38.10	40.00	38.10	31x31	0.75	-	1.27	-	-	-		0.00
Max.	1.70	0.70	1.00	40.10	38.20	40.10	38.20		0.90	-	-	0.20	0.25	0.20	0.20	-

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