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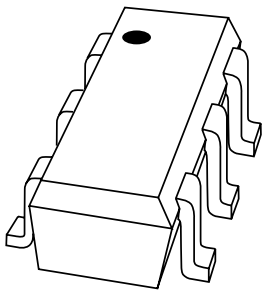
DATA SHEET



PUMF11
NPN resistor-equipped transistor; PNP general purpose transistor

Product specification

2002 Apr 09

Philips Semiconductors

PHILIPS

NPN resistor-equipped transistor; PNP general purpose transistor

PUMF11

FEATURES

- Resistor-equipped transistor and general purpose transistor in one package
- 100 mA collector current
- 50 V collector-emitter voltage
- 300 mW total power dissipation
- SOT363 package; replaces two SOT323 (SC-70) packaged devices on same PCB area
- Reduced pick and place costs.

APPLICATIONS

- Power management switch for portable equipment, e.g. cellular phone and CD player
- Switch for regulator.

DESCRIPTION

NPN resistor-equipped transistor and a PNP general purpose transistor in a SOT363 (SC-88) plastic package.

MARKING

TYPE NUMBER	MARKING CODE(1)
PUMF11	R1∗

Note

1. ∗ = p: Made in Hong Kong.
   ∗ = t: Made in Malaysia.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
TR1 (NPN)			
V_{CEO}	collector-emitter voltage	50	V
I_O	output current (DC)	100	mA
R1	bias resistor	22	kΩ
R2	bias resistor	47	kΩ
TR2 (PNP)			
V_{CEO}	collector-emitter voltage	50	V
I_C	collector current (DC)	100	mA
I_{CM}	peak collector current	200	mA

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

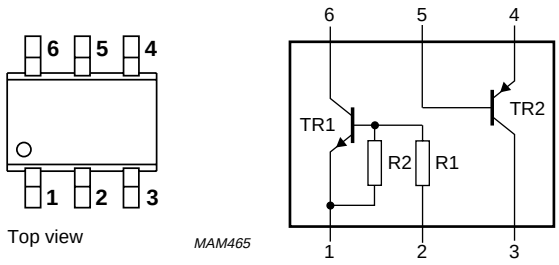


Fig.1 Simplified outline (SOT363) and symbol.

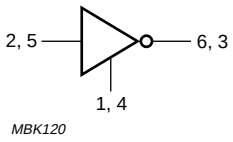


Fig.2 Equivalent inverter symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
TR1 (NPN)					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_i	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I_O	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
TR2 (PNP)					
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–200	mA
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	300	mW

Note

1. Device mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air; note 1	416	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TR1 (NPN)						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0	–	–	1	μA
		V_{CE} = 30 V; I_B = 0; T_j = 150 °C	–	–	50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0	–	–	0.12	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	–	–	150	mV
$V_{i(off)}$	input off voltage	V_{CE} = 5 V; I_C = 100 μA	–	0.9	0.5	V
$V_{i(on)}$	input on voltage	V_{CE} = 0.3 V; I_C = 2 mA	2	1.1	–	V
R1	input resistor		15.4	22	28.6	kΩ
$\frac{R2}{R1}$	resistor ratio		1.7	2.1	2.6	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0; f = 1 MHz	–	–	2.5	pF
TR2 (PNP)						
I_{CBO}	collector-base cut-off current	V_{CB} = –30 V; I_E = 0	–	–	–100	nA
I_{CEO}	collector-emitter cut-off current	V_{CB} = –30 V; I_B = 0; T_j = 150 °C	–	–	–10	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = –4 V; I_C = 0	–	–	–100	nA
h_{FE}	DC current gain	V_{CE} = –6 V; I_C = –1 mA	120	–	–	
V_{CEsat}	saturation voltage	I_C = –50 mA; I_B = –5 mA; note 1	–	–	–200	mV
C_c	collector capacitance	V_{CB} = –12 V; I_E = i_e = 0; f = 1 MHz	–	–	2.2	pF
f_T	transition frequency	V_{CE} = –12 V; I_C = –2 mA; f = 100 MHz	100	–	–	MHz

Note

1. Device mounted on an FR4 printed-circuit board.

APPLICATION INFORMATION

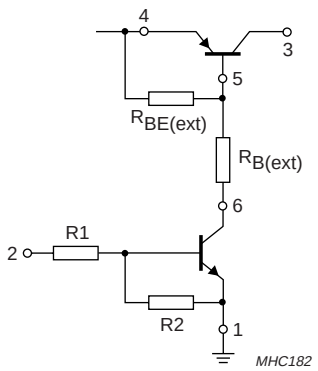
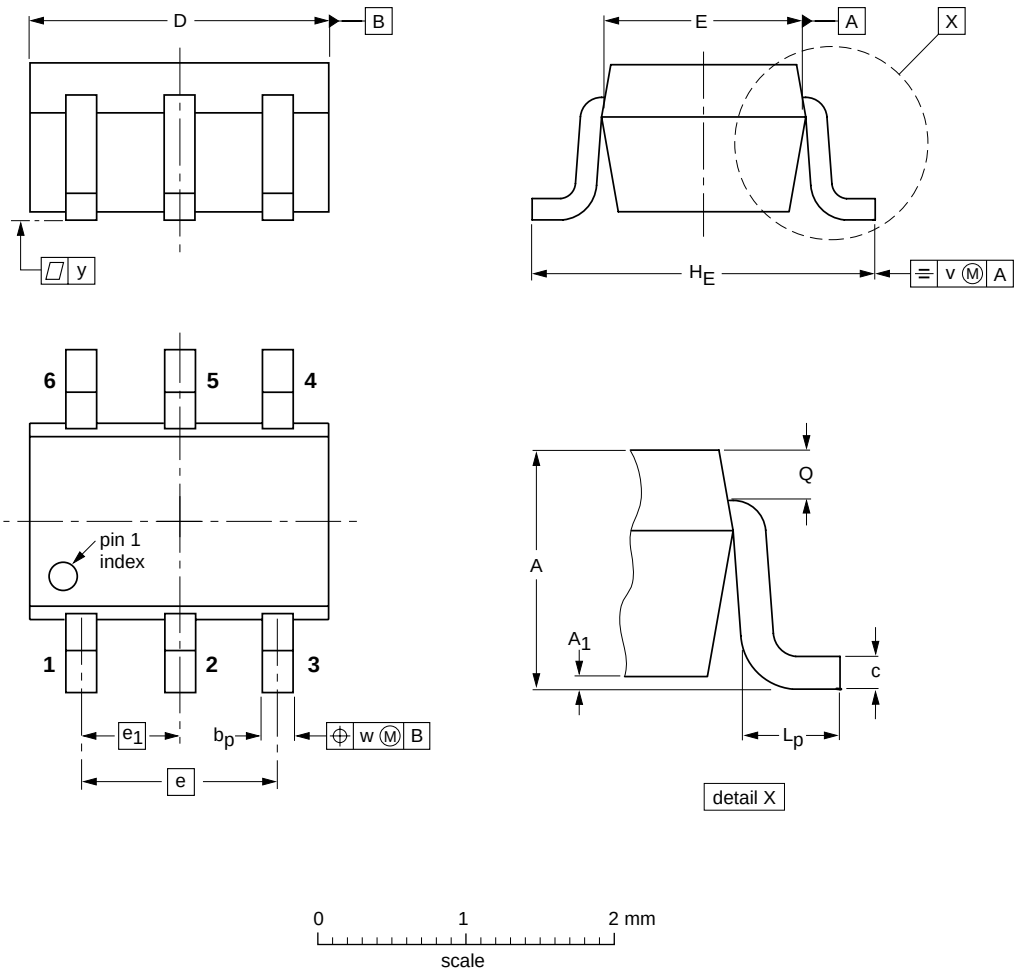


Fig.3 Typical power management circuit.

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

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