Intel® Wireless Flash Memory (W18/W30 SCSP)

128-Mbit WQ Family with Asynchronous SRAM

Datasheet

- **Flash Architecture**
  - — Flexible, Multiple-Partition, Dual-Operation: Read-While-Write / Read-While-Erase
  - — 32 Partitions, 4 Mbits each
    - —31 Main Partitions, 8 Main Blocks each
    - —1 Parameter Partition, 8 Parameter + 7 Main Blocks
    - —32-Kword Main Blocks, 4-Kword Parameter Blocks
  - — Top or Bottom Parameter - single Flash die
  - — Dual Parameter - dual Flash die
- **Flash Performance**
  - — 65 ns Initial Access at 1.8 V or 3.0 V I/O
  - — 25 ns Async Page at 1.8 V or 3.0 V I/O
  - — 14 ns Sync Read (t_{CHQV}) at 1.8V I/O
  - — 20 ns Sync Read (t_{CHQV}) at 3.0 V I/O
  - — 4-, 8-, 16-, Continuous-Word Burst Lengths
  - — Burst Suspend
  - — Programmable WAIT Configuration
  - — Enhanced Factory Programming Mode: 3.1µs/Word
  - — Flash Protection Register
    - —64 Unique Device Identifier Bits
    - —64 User-Programmable OTP Bits
- **Flash Automation Suspend Operations**
  - — Erase Suspend to Program or Read
  - — Program Suspend to Read
  - — 5/9 µs (typ) Program/Erase Suspend Latency
- **Flash Data Protection**
  - — Absolute Protection with VPP and WP#
  - — Individual Dynamic zero-Latency Block Locking
  - — Individual Block Lock-Down
  - — Erase/Program Lockout during Power Transitions
- **Flash Software**
  - — Intel® Flash Data Integrator (FDI) Optimized
  - — Common Flash Interface (CFI)
- **SCSP Architecture**
  - — Flash
  - — Flash + Flash
  - — Flash + PSRAM
  - — Flash + Flash + PSRAM
  - — Reduces Board Space Requirement
  - — Simplifies PCB Design Complexity
  - — Easy Migration to Future SCSP Devices
- **SCSP Voltage**
  - — Core: V_{CC} =1.8 V (Typ)
  - — I/O: V_{CCQ} = 1.8 V or 3.0 V (Typ)
- **SCSP Packaging**
  - — 0.8 mm Ball-Pitch Intel® SCSP
  - — Area: 8x10 mm
  - — Height: 1.2mm and 1.4mm
  - — 88-Ball (8 x 10 Matrix): 80 Active Balls with 2 Support Balls at Each Corner
- **PSRAM Architecture and Performance**
  - — 2.7 V to 3.1 V P-V_{CC}
  - — 65 ns Access Speed
  - — 8-Word Page Read
  - — 18 ns for 32 M/64 M Page Read Speed
  - — Low Power Mode
- **Flash Quality and Reliability**
  - — Extended Temperature: –25 °C to +85 °C
  - — Minimum 100K Block Erase Cycles
  - — 0.13 µm ETOX™ VIII Process

This versatile and compact Stacked Chip Scale Package (SCSP) solution from Intel is created by combining the Intel® Wireless Flash Memory (W18/W30) device with low-power PSRAM. Ideal for high-performance, low-power, board-constrained memory applications, the Intel® Wireless Flash Memory (W18/W30 SCSP) family retains all the features of the Intel® Wireless Flash Memory (W18/W30) discrete device, such as a flexible multi-partition architecture that provides dual-operation Read-While-Write/Read-While-Erase (RWW/RWE) capability and high performance asynchronous/synchronous burst reads. Device upgrades and migrations are easy with a common package footprint and signal ballout for all SCSP combinations. Manufactured on Intel® 0.13 micron ETOX™ VIII process technology, this device provides the highest levels of quality and reliability.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 252063-006
June 2004

Contents

Revision History

Date of Revision	Version	Description
10/02	-001	Initial draft
4/4/03	-002	General language and format edit; also edited out some line items.
5/6/03	-003	Update the 64M-bit PS, ICC, ISB, and IDP current.
10/03	-004	Updated to resolve some format issues.
5/04	-005	Restructured the datasheet according to the new layout.
6/04	-006	Added part number 128W18+128W18 to Table 1 and Table 16. Updated the DC and AC specifications.

1.0 Introduction

This document contains information pertaining to the Stacked Chip Scale Package (SCSP) products included in the Intel® Wireless Flash Memory (W18/W30 SCSP) family. The intent of this document is to provide information where the SCSP family differs from the Intel® Wireless Flash Memory (W18/W30) discrete device.

Refer to the latest revision Intel® Wireless Flash Memory (W18) datasheet (order number 290701) and Intel® Wireless Flash Memory (W30) datasheet (order number 290702) for flash product details not included in this document.

1.1 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
CUI	Command User Interface
DU	Do not Use
ETOX	EPROM Tunnel Oxide
k (noun)	1 thousand
Kb	1024 bits
KB	1024 bytes
Kword	1024 words
M (noun)	1 million
Mb	1,048,576 bits
MB	1,048,576 bytes
OTP	One Time Programmable
PLR	Protection Lock Register
PR	Protection Register
PRD	Protection Register Data
RCR	Read Configuration Register
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package
SR	Status Register
SRD	Status Register Data
Word	16 bits

1.2 Conventions

Group Membership Brackets: Square brackets will be used to designate group membership or to define a group of signals with a similar function, such as A[21:1] and SR[4,1], for example.

VCC vs. V_{CC}: When referring to a signal or package-connection name, the notation used is VCC, etc. When referring to a timing or electrical level, the notation used is subscripted such as V_{CC}, etc.

Device: This term is used interchangeably throughout this document to denote either a particular die, or the combination of the four die.

CE#[2:1], OE#[2:1]: This is the method used to refer to more than one chip-enable or output enable at the same time. When each is referred to individually, the reference will be CE#1 and OE#1 (for die #1), and CE#2 and OE#2 (for die #2).

VCC, P-VCC, S-VCC: When referencing flash memory signals or timings, the notation used is VCC or $V_{CC,}$ respectively. When the reference is to PSRAM signals or timings, the notation is prefixed with "P-" (e.g., P-VCC, P-V_{CC}). When referencing SRAM signals or timings, the notation is prefixed with "S-" (e.g., S-VCC or S-V_{CC}).

R-OE#, R-LB#, R-UB#, R-WE#: Used to identify OE#, LB#, UB#, WE# RAM signals, and are usually shared between 2 or more RAM die.

2.0 Functional Overview

This section provides an overview of the features and capabilities of the Intel® Wireless Flash Memory (W18/30 SCSP) family.

The Intel® Wireless Flash Memory (W18/W30 SCSP) family encompasses multiple flash memory + PSRAM die combinations. Products range from a flash-only, dual-flash, dual-flash + PSRAM device. The user can choose PSRAM combined with one or two flash memory dies, all offered in the same package footprint and signal ballout.

Table 1, "W18/30 SCSP Family Matrix" on page 9 summarizes the Intel® Wireless Flash Memory (W18/W30 SCSP) family offerings.

Table 1. W18/30 SCSP Family Matrix

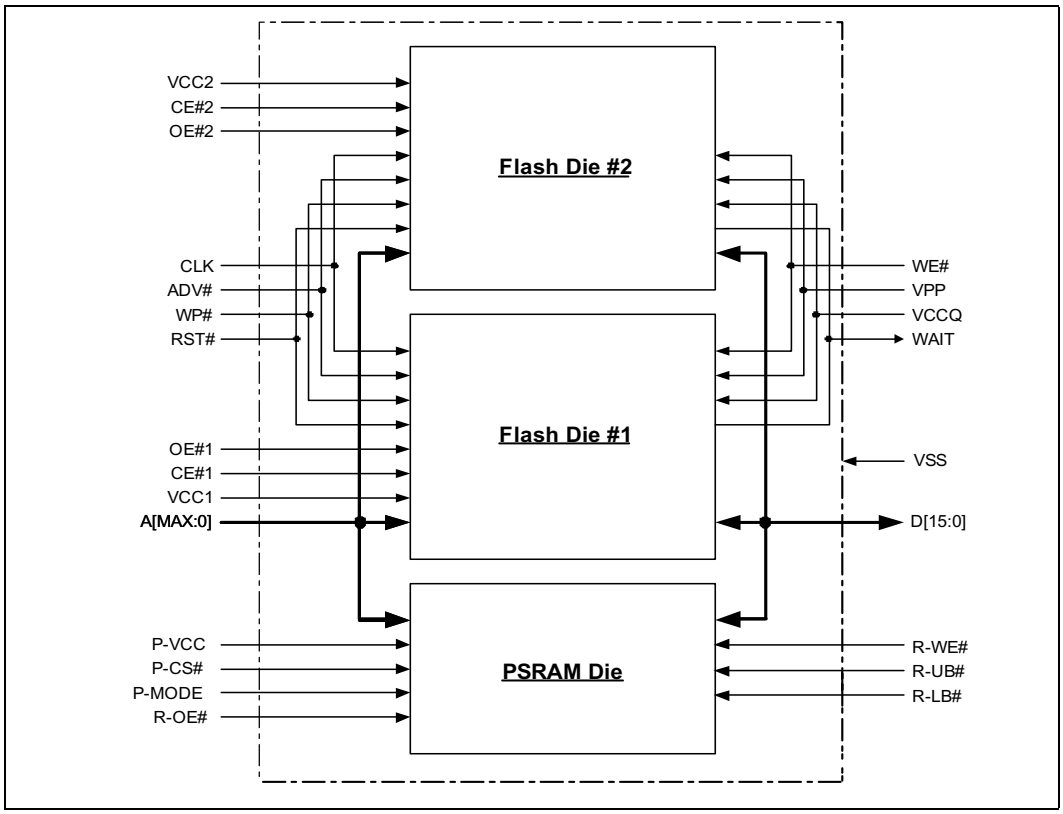
I/O Voltage (V)	Flash	RAM	Package Size (mm)			Part Number	Notes
			Size	Ball	Type		
1.8	128W18+128W18	—	8x10x1.2	Lead-free	SCSP QUAD+	PF48F3300W0YD0	1
3.0	128W30+128W30	64PSRAM	8x10x1.4	Leaded	SCSP QUAD+	RD38F3350W0ZDQ0	1

Notes:
1. D = A 2-Die stack device, where die#1 = Bottom Parameter and Die#2 = Top Parameter.

2.1 Block Diagram

Figure 1 is a block diagram showing all internal package connections for the SCSP family with multiple dies. Refer to Table 1, "W18/30 SCSP Family Matrix" on page 9 for valid combinations of flash and PSRAM die. Unused connections on combinations with less than triple die are reserved and should not be used.

Figure 1. Block Diagram



2.2 Flash Memory Map and Partitioning

Consult the latest Intel® Wireless Flash Memory (W18) datasheet (order number 290701) and Intel® Wireless Flash Memory (W30) datasheet (order number 290702) for individual flash die memory map and partitioning information.

Refer to Table 1, "W18/30 SCSP Family Matrix" on page 9 for valid configurations per SCSP combination. Table 2, "Flash Die Memory Map and Partitioning" on page 11 shows the Memory Map and Partitioning information for two flash memory die. Flash Die#1(with CE#1 as its Chip Select) is configured to bottom boot while Flash Die#2 (with CE#2 as its Chip Select) is configured to top boot.

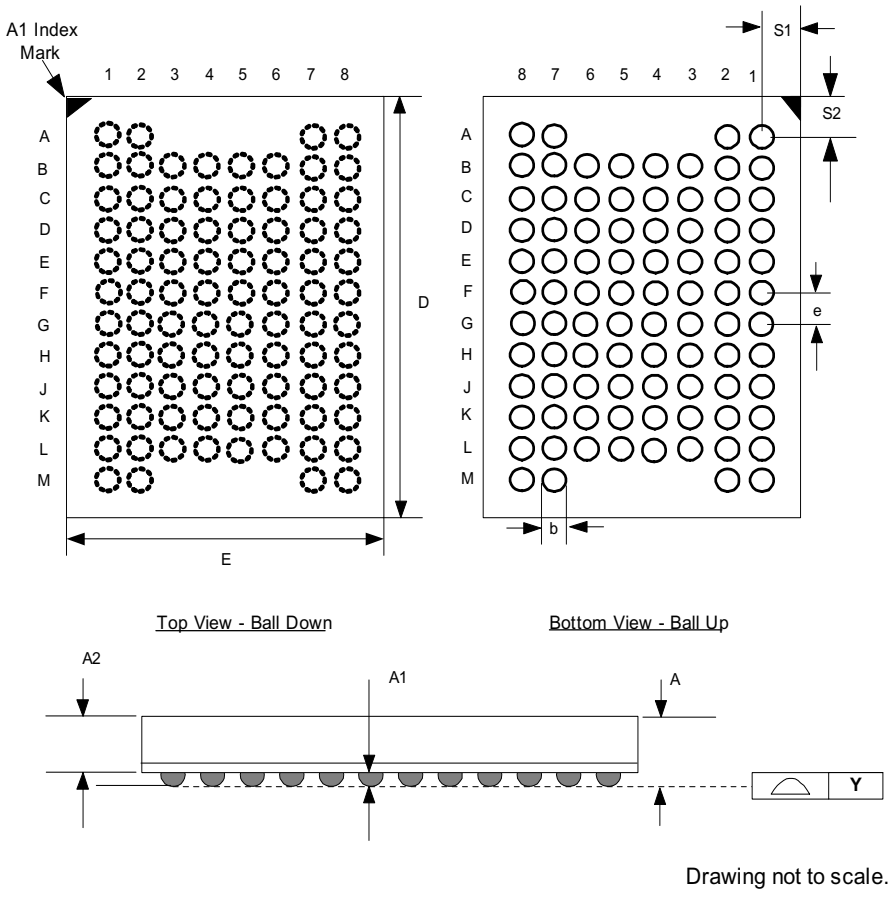
Table 2. Flash Die Memory Map and Partitioning

Flash Die#	Partitioning		Block Size (KW)	Blk#	Address Range
Flash die (Top Parameter) 128M-bit	Parameter Partition	One Partition	4	255-262	7F8000-7FFFFF
			32	248-254	7C0000-7F7FFF
	Main Partitions	One Partition	32	240-247	780000-7BFFFF
		One Partition	32	232-239	740000-77FFFF
		One Partition	32	224-231	700000-73FFFF
		Four Partitions	32	192-223	600000-6FFFFF
		Eight Partitions	32	128-191	400000-5FFFFF
		Sixteen Partitions	32	0-127	000000-3FFFFF
Flash die (Bottom Parameter) 128 Mbit	Main Partitions	Sixteen Partitions	32	135-262	400000-7FFFFF
		Eight Partition	32	71-134	200000-3FFFFF
		Four Partitions	32	39-70	100000-1FFFFF
		One Partition	32	31-38	0C0000-0FFFFF
		One Partition	32	23-30	080000-0BFFFF
		One Partition	32	15-22	040000-07FFFF
	Parameter Partition	One Partition	32	8-14	008000-03FFFF
			4	0-7	000000-007FFF

3.0 Package Information

3.1 80-Active Ball Single or Double-Die SCSP

Figure 2. SCSP QUAD+ Mechanical Specifications (8x10x1.2 mm)

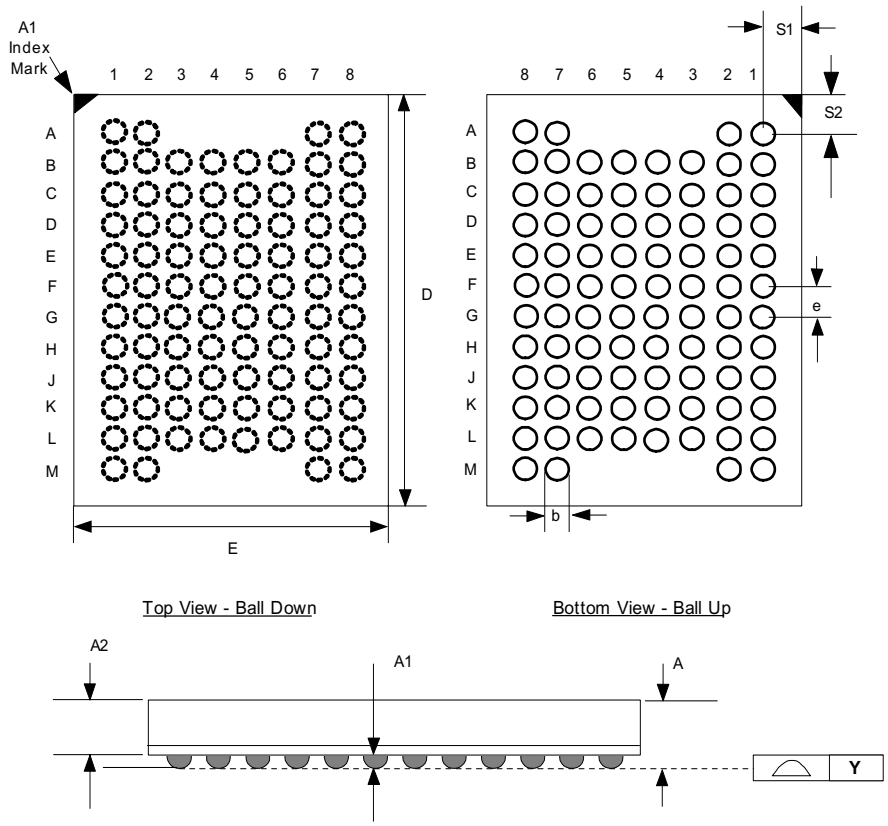


Drawing not to scale.

		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

3.2 80-Active Ball Triple-Die SCSP

Figure 3. SCSP QUAD+ Mechanical Specifications (8x10x1.4 mm)



Drawing not to scale.

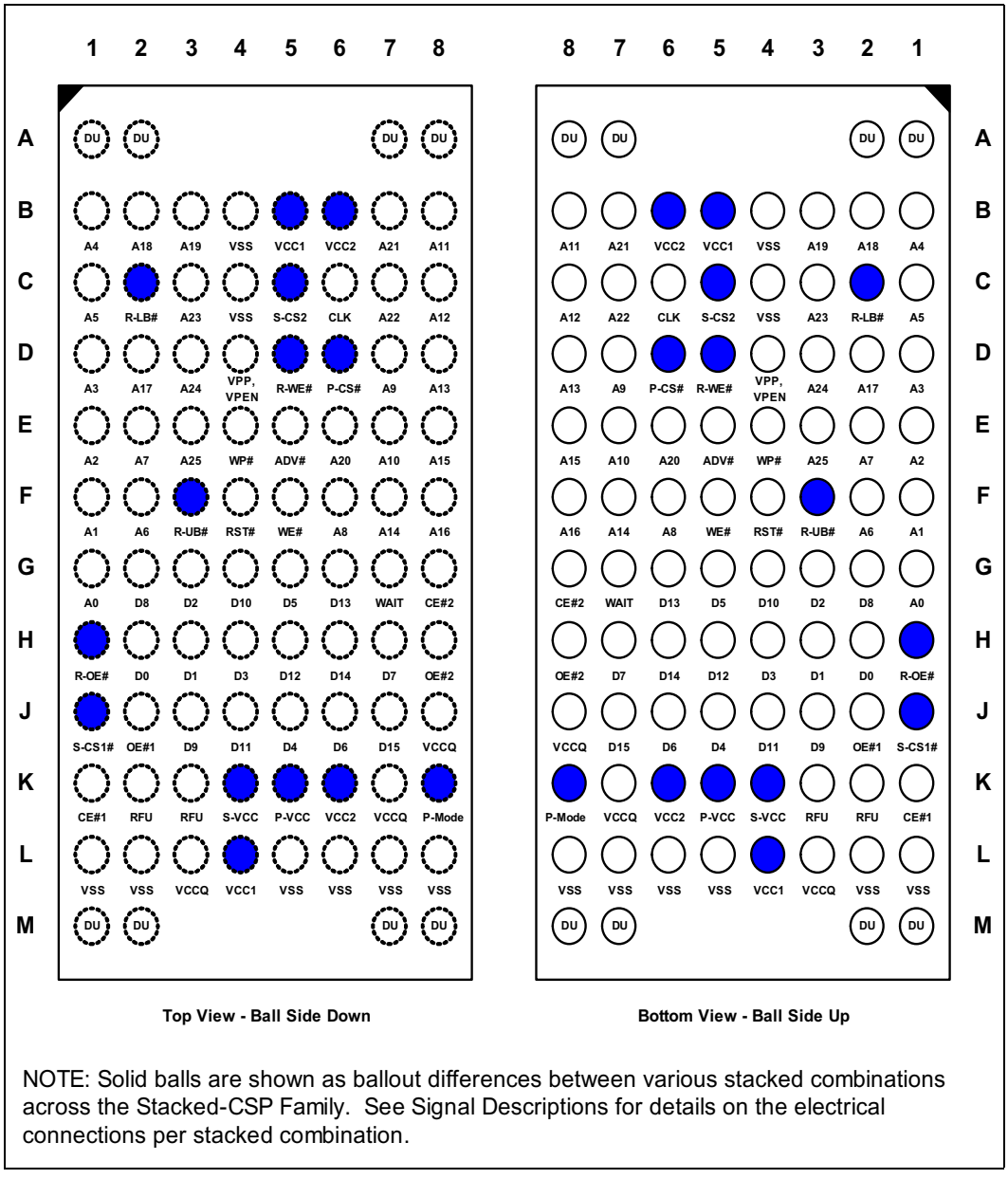
		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.400				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

4.0 Ballout and Signal Descriptions

4.1 Signal Ballout

The Intel® Wireless Flash Memory (W30 SCSP) family is available in an 88-ball (80-active ball) Stacked Chip Scale Package (SCSP) with a ball pitch of 0.8 mm, as shown in Figure 4.

Figure 4. 88-Ball (80-Active Ball) SCSP Package Ballout



NOTE: Solid balls are shown as ballout differences between various stacked combinations across the Stacked-CSP Family. See Signal Descriptions for details on the electrical connections per stacked combination.

4.2 Signal Descriptions

Table 3 describes the active signals used on the Intel® Wireless Flash Memory (W30 SCSP) family.

Table 3. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Descriptions
A[Max:0]	Input	**ADDRESS INPUTS** for memory addresses of a SCSP device with: • 4 Mbit density: A[Max]=A17 • 8 Mbit density: A[Max]=A18 • 32 Mbit density: A[Max]=A20 • 64 Mbit density: A[Max]=A21 • 128 Mbit density: A[Max]=A22
D[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs data and commands during writing cycles, outputs data during memory, status register, protection register and configuration code reads. These signals float when the die or outputs are deselected. Data is internally latched during writes.
CE#1 CE#2	Input	**FLASH CHIP ENABLE:** CE#-low selects the flash component. When asserted, the flash internal control logic, input buffers, decoders, and sense amplifiers are activated. When deasserted, the flash die is deselected, power reduces to standby levels, and data and WAIT outputs are placed in high-Z state. CE#1 connects to Flash Die#1 Chip Enable while CE#2 connects to Flash Die#2 Chip Enable. CE#2 is only connected for SCSP combinations with 2 flash dies.
RST#	Input	**FLASH RESET:** RST#-low resets flash internal circuitry and inhibits write operations. This function may be employed to provide data protection during power transitions. After exiting the reset state (RST# returned to logic-high), the selected flash die resumes operation in asynchronous read-array mode.
OE#1 OE#2	Input	**FLASH OUTPUT ENABLE:** OE#-low activates device output through the flash data buffers during a flash read cycle. When deasserted, the flash outputs tri-state to high-Z. OE#1 connects to Flash Die#1 Output Enable while OE#2 connects to Flash Die#2 Output Enable. OE#2 is only connected for SCSP combinations with 2 flash dies.
WE#	Input	**FLASH WRITE ENABLE:** WE# controls writes to the selected flash die. WE#-low allows input to the flash CUI, array, PR/PLR, RCR, or block lock bits. Addresses and data are latched on this signal's rising edge.
ADV#	Input	**FLASH ADDRESS VALID:** ADV# indicates valid address presence on address inputs of the selected flash die. During synchronous read operations, all addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
CLK	Input	**FLASH CLOCK:** CLK synchronizes the selected flash die to the system bus frequency in synchronous-read configuration and increments an internal burst address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first. CLK is only used for synchronous mode. Refer to flash product discrete datasheet for information how to use this signal in asynchronous mode.
WAIT	Output	**FLASH WAIT:** Wait is driven when CE# is asserted. Flash RCR[10][WP] determines the WAIT asserted logic level. • In synchronous array read modes, WAIT indicates invalid data when asserted and valid data when de-asserted. • In synchronous non-array read modes, asynchronous page mode, and all write modes, WAIT is asserted. Refer to flash product discrete datasheet for more information.

Table 3. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Descriptions
WP#	Input	**FLASH WRITE PROTECT:** Enables/disables the lock-down mechanism of the selected flash die. When WP# is logic low, the lock-down mechanism is enabled and blocks marked lock-down can not be unlocked through software.
VPP	Power	**FLASH PROGRAM / ERASE SUPPLY:** Valid V_{PP} voltage on this ball allow block erase and program functions. Flash memory array contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block Erase and program at invalid V_{PP} Voltage should not be attempted.
VCC1 VCC2	Power	**FLASH POWER SUPPLY:** Supplies power to the flash core. VCC1 connects to Flash Die#1 power supply while VCC2 connects to Flash Die#2 power supply. VCC2 is only connected for SCSP combinations with 2 flash dies.
VCCQ	Power	**OUTPUT BUFFER POWER SUPPLY:** Supplies power for the input and output buffers.
VSS	Power	**GROUND:** Do not float any VSS connection.
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** Activates the SRAM internal control logic, input buffers, decoders, and sense amplifiers. When either are deasserted (S-CS1# = V_{IH} or S-CS2 = V_{IL}), the SRAM is deselected and its power reduces to standby levels. S-CS1# and S-CS2 are only connected for SCSP combinations with SRAM die.
R-OE#	Input	**RAM OUTPUT ENABLE:** R-OE#-low activates device output through the selected RAM data buffers during a RAM read cycle. When deasserted, the selected RAM outputs tri-state to high-Z. R-OE# is only connected for SCSP combinations with 1 or more RAM die.
R-WE#	Input	**RAM WRITE ENABLE:** R-WE#-low allows writes to the selected RAM array. R-WE# is only connected for SCSP combinations with 1 or more RAM die.
R-UB# R-LB#	Input	**RAM UPPER / LOWER BYTE ENABLES:** R-UB#-low enables the selected RAM high-order bytes (D[15:8]). R-LB#-low enables the selected RAM low-order bytes (D[7:0]). R-UB# and R-LB# are only connected for SCSP combinations with 1 or more RAM die.
S-VCC	Power	**SRAM POWER SUPPLY:** Supplies power for SRAM operations. S-VCC is only connected for SCSP combinations with SRAM die.
P-CS#	Input	**PSRAM CHIP SELECT:** Activates the PSRAM internal control logic, input buffers, decoders, and sense amplifiers. When deasserted, the PSRAM is deselected and its power reduces to standby levels. P-CS# is only connected for SCSP combinations with PSRAM die.
P-Mode	Input	**PSRAM REFRESH:** When deasserted, it enables PSRAM Lower Power Mode with partial array refresh or zero array refresh according to the Mode register setting. P-Mode is only connected for SCSP combinations with PSRAM die.
P-VCC	Power	**PSRAM POWER SUPPLY:** Supplies power for PSRAM operations. P-VCC is only connected for SCSP combinations with PSRAM die.
RFU	—	**RESERVED for FUTURE USE:** Do not drive RFU balls and leave them disconnected. Contact Intel regarding their future use.
DU	—	**DO NOT USE:** Do not connect to any other signal, or power supply; must be left floating.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 4. Absolute Maximum Ratings

Parameter		Min	Max	Unit	Notes
Temperature under Bias Expanded		–25	+85	°C	
Storage Temperature		–55	+125	°C	
Voltage On Any Signal (except V_{CC1}, V_{CC2}, V_{CCQ}, V_{PP}, and P-V_{CC})	1.8 V I/O	–0.2	+2.45	V	1
	3.0 V I/O	–0.2	+3.6	V	1
V_{CC1} and V_{CC2} Voltage		–0.2	+2.45	V	1
V_{CCQ}, and P-V_{CC} Voltage		–0.2	+3.6	V	1
V_{PP} Voltage		–0.2	+14.0	V	1,2,3
I_{SH} Output Short Circuit Current		–	100	mA	4

Notes:

1. All Specified voltages are relative to V_{SS}. Minimum DC voltage is –0.2 V on input/output signals, –0.2 V on VCCX and VPP signals. During transitions, this level may overshoot to –2.0 V for periods < 20 ns, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
2. Maximum DC voltage on VPP may overshoot to +14.0 V for periods < 20 ns.
3. V_{PP} program voltage is normally V_{PP1}. The maximum DC voltage on V_{PP} may overshoot to +14 V for periods < 20 ns. V_{PP} can be V_{PP2} for 1000 erase cycles on main blocks, 2500 cycles on parameter blocks.
4. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Table 5. Extended Temperature Operation

Symbol	Parameter		Flash/ Flash+Flash		Flash+PSRAM/ Flash+Flash+PSRAM		Unit
			Min	Max	Min	Max	
T_C	Operating Temperature		–25	+85	–25	+85	°C
V_{CC}	Flash Supply Voltage		1.7	1.95	1.7	1.95	V
V_{CCQ} $P\text{-}V_{CC}$	Flash I/O Voltage PSRAM Supply Voltage	1.8 V I/O	1.7	1.95	—	—	V
		3.0 V I/O	2.2	3.3	2.7	3.1	V
V_{PP1}	Flash Program Logic Level		0.9	1.95	0.9	1.95	V
V_{PP2}	Flash Factory Program Voltage		11.4	12.6	11.4	12.6	V

Note: VPP is normally V_{PP1}. VPP can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles on parameter blocks at extended temperature.

5.3 Capacitance

NOTICE: Refer to the Intel® Wireless Flash Memory (W18 and W30) datasheets (order number 290701 and 29702) for flash capacitance details. For SCSP products with two flash die, flash capacitances for each of the flash die need to be considered accordingly.

Table 6. PSRAM Capacitance

Symbol	Parameter	Max	Unit	Condition
C_{IN}	Input Capacitance	8	pF	TA=25°C, f=1MHz, V_{IN}=0V
C_{OUT}	Output Capacitance	10	pF	

6.0 Electrical Specifications

6.1 DC Characteristics

PSRAM DC characteristics are shown in Table 7. Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for Flash DC Characteristics.

NOTICE: DC Characteristics of all die in a SCSP device need to be considered accordingly, depending on the SCSP device operation.

Table 7. PSRAM DC Characteristics

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
P-V_{CC}	Voltage Range				2.7	–	3.1	V
I_{CC}	Operating Current at min cycle time	I_{out}=0mA	32M		–	–	45	mA
			64M		–	–	50	
I_{SB1}	Standby Current	P-CS#>=P-V_{CC}-0.2V, P-Mode>=P-V_{CC}-0.2V	32M		–	90	100	µA
			64M		–	110	150	
I_{SB2}	Partial Array Refresh Current (Standby Mode 2)	P-CS#>=P-V_{CC}-0.2V, P-Mode<=0.2V	32M	16Mbits	–	60	70	µA
				8Mbits	–	50	60	
				4Mbits	–	40	50	
				0Mbits	–	20	30	
			64M	16Mbits	–	90	110	
				8Mbits	–	80	100	
				4Mbits	–	70	90	
				0Mbits	–	60	80	
I_{sbd}	Deep Power Down	P-CS#>=P-V_{CC}-0.2V, P-Mode<=0.2V	32M		–	20	30	µA
			64M		–	60	80	
V_{OH}	Output High Voltage	I_{OH} = -0.5mA	32M		0.8P-Vcc	–	–	V
			64M		0.8P-Vcc	–	–	
V_{OL}	Output Low Voltage	I_{OL} = 1mA	32M		–	–	0.2P-Vcc	V
			64M		–	–	0.2P-Vcc	
V_{IH}	Input High Voltage				0.8P-Vcc	–	P-V_{CC} + 0.3	V
V_{IL}	Input Low Voltage				-0.3	–	0.2P-V_{CC}	V
*I_{IL}	Input Leakage Current	V_{IN}=0V to P-Vcc			–1.0	–	+1.0	µA
*I_{OL}	Input/Output Leakage Current	$V_{I/O}$=0V to P-Vcc, P-CS#=V_{IH} or R-WE#=V_{IH} or R-OE#=V_{IH}			–1.0	–	+1.0	

* V_{IN}: Input voltage, $V_{I/O}$: Input/Output voltage

7.0 AC Characteristics

7.1 Flash AC Characteristics

Refer to the *Intel® Wireless Flash Memory (W18/W30) Datasheets* (order number 290701 and 290702) for Flash AC Characteristics details not included in Table 8 below.

Table 8. Flash AC Read Characteristics

Spec Number	Sym	Parameter	128W18		128W30		64W30		Unit
			Min	Max	Min	Max	Min	Max	
Asynchronous Specifications									
R1	t_{AVAV}	Read Cycle Time	65		65		65		ns
R2	t_{AVQV}	Address to Output Delay		65		65		65	ns
R3	t_{ELQV}	CE# Low to Output Delay		65		65		65	ns
R103	t_{VLQV}	ADV# Low to Output Delay		65		65		65	ns
Latching Specifications									
R108	t_{APA}	Page Address Access Time		25		25		25	ns
Clock Specifications									
R304	t_{CHQV}	CLK to Output Delay		14		20		20	ns

7.2 PSRAM AC Characteristics

Table 9. PSRAM AC Characteristics—Read-Only Operations

#	Symbol	Parameter	32M		64M		Unit	Note
			Min	Max	Min	Max		
Read Cycle								
R1	t_{RC}	Read Cycle Time	65	–	65	–	ns	
R2	t_{AA}	Address access time	–	65	–	65	ns	
R3	t_{CO}	P-CS# Low to Output Valid	–	65	–	65	ns	
R4	t_{OE}	R-OE# Low to Output Valid	–	45	–	45	ns	
R5	t_{BA}	R-UB#, R-LB# Low to Output Valid	–	65	–	65	ns	
R6	t_{LZ}	P-CS# Low to Output in Low-Z	10	–	10	–	ns	
R7	t_{OLZ}	R-OE# Low to Output in Low-Z	5	–	5	–	ns	
R8	t_{HZ}	P-CS# High to Output in High-Z	–	25	–	25	ns	
R9	t_{OHZ}	R-OE# High to Output in High-Z	–	25	–	25	ns	
R10	t_{OH}	Output Hold from Address change	5	–	5	–	ns	
R11	t_{BLZ}	R-UB#, R-LB# Low to Output in Low-Z	5	–	5	–	ns	
R12	t_{BHZ}	R-UB#, R-LB# High to Output in High-Z	–	25	–	25	ns	
R13	t_{ASO}	Address set to R-OE# low level	0	–	0	–	ns	1
R14	t_{OHAH}	R-OE# high level to address hold	-5	–	-5	–	ns	
R15	t_{CHAH}	P-CS# high level to address hold	0	–	0	–		1
R16	t_{BHAH}	R-LB#, R-UB# high level to address hold	0	–	0	–		1,2
R17	t_{CLOL}	P-CS# low level to R-OE# low level	0	10,000	0	10,000		3
R18	t_{OLCH}	R-OE# low level to P-CS# high level	45	–	45	–		
R19	t_{CP}	P-CS# high level pulse width	10	–	10	–		
R20	t_{BP}	R-UB#, R-LB# high level pulse width	10	–	10	–		
R21	t_{OP}	R-OE# high level pulse width	–	10,000	–	10,000		3
Page Mode								
PR1	t_{PC}	Page Cycle Time	18	–	18	–	ns	4
PR2	t_{PA}	Page Mode Address Access Time	–	18	–	18	ns	

Note:

1. When.R13>=|R15|, |R16|. The minimum of R15 and R16 are -15ns. (See Figure 5, “Conditions for Calculating R15 and R16 Minimum Values” on page 22.)
2. R16 is specified from when both R-LB# and R-UB# become high level.
3. R17and R21(MAX) are applied while P-CS# is being hold at low level.
4. See Figure 7, “AC Waveform of PSRAM Read Operations” on page 23.

Figure 5. Conditions for Calculating R15 and R16 Minimum Values

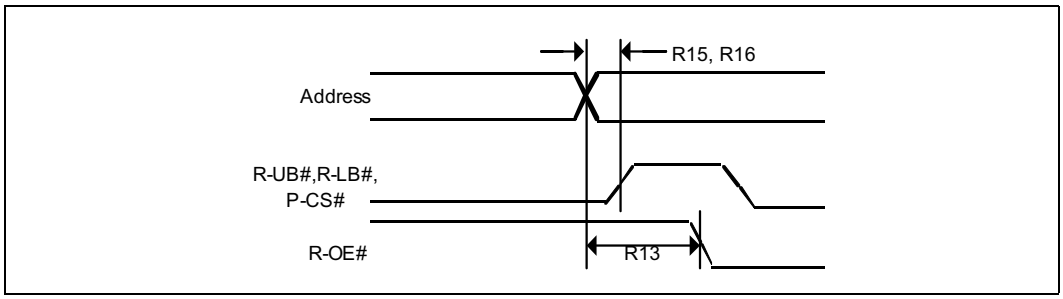


Table 10. PSRAM AC Characteristics—Write Operations

#	Symbol	Parameter	32M		64M		Unit	Note
			Min	Max	Min	Max		
W1	t_{WC}	Write Cycle Time	65	–	65	–	ns	
W2	t_{AS}	Address Setup Time	0	–	0	–	ns	
W3	t_{WP}	Write Pulse Width	50	–	50	–	ns	
W4	t_{DW}	Data valid to Write End	30	–	30	–	ns	
W5	t_{AW}	Address valid to end of write	55	–	55	–	ns	
W6	t_{CW}	P-CS# to end of write	55	–	55	–	ns	
W7	t_{DH}	Data Hold time	0	–	0	–	ns	
W8	t_{WR}	Write Recovery	0	–	0	–	ns	
W9	t_{BW}	R-UB#, R-LB# Setup to end of Write	55	–	55	–	ns	
W10	t_{CP}	P-CS# High level pulse width	10	–	10	–	ns	
W11	t_{BP}	R-UB#, R-LB# High level pulse width	10	–	10	–	ns	
W12	t_{WHP}	R-WE# High level pulse width	10	–	10	–	ns	
W13	t_{OHAH}	R-OE# High level to address hold	-5	–	-5	–	ns	
W14	t_{CHAH}	P-CS# High level to address hold	0	–	0	–	ns	1
W15	t_{BHAH}	R-UB#, R-LB# High level to address hold	0	–	0	–	ns	1,2
W16	t_{OES}	R-OE# High level to R-WE# set	0	10,000	0	10,000	ns	3
W17	t_{OEH}	R-WE# High level to R-OE# set	0	10,000	0	10,000	ns	

Notes:
1. When W2>=|W14|, |W15| and W10>=18ns, W14 and W15 (MIN) are -15ns. (See Figure 6, “Conditions for Calculating R14 and R15 Minimum Values” on page 23.)
2. W15 is specified from when both R-LB# and R-UB# become high level.
3. W16 and W17(MAX) are applied while P-CS# is being hold at low level.
4. See Figure 9, “AC Waveform PSRAM Write Operation”

Figure 6. Conditions for Calculating R14 and R15 Minimum Values

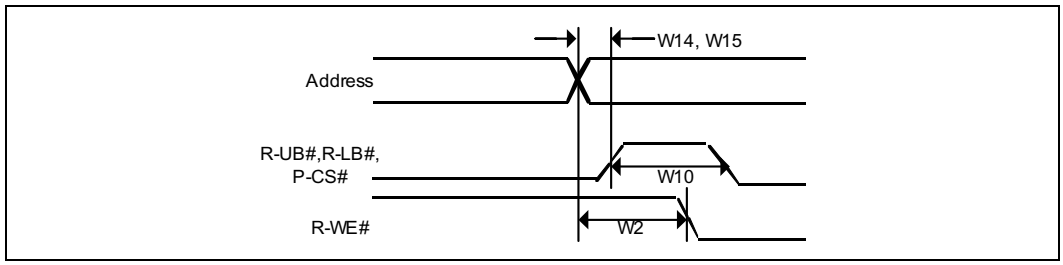
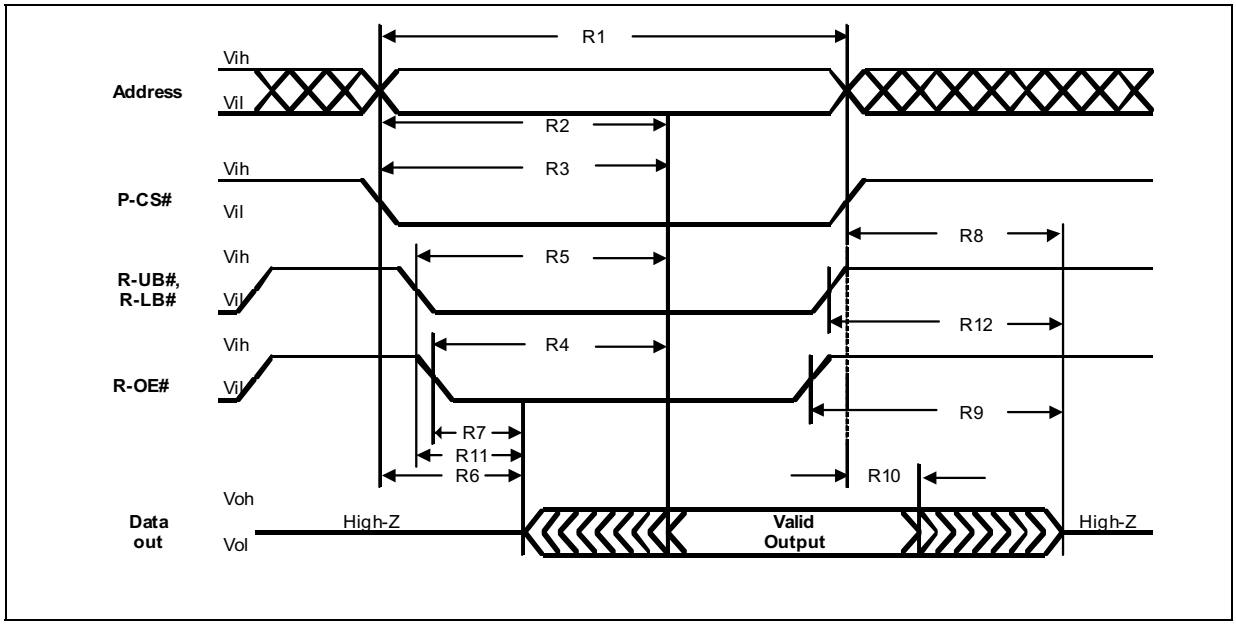
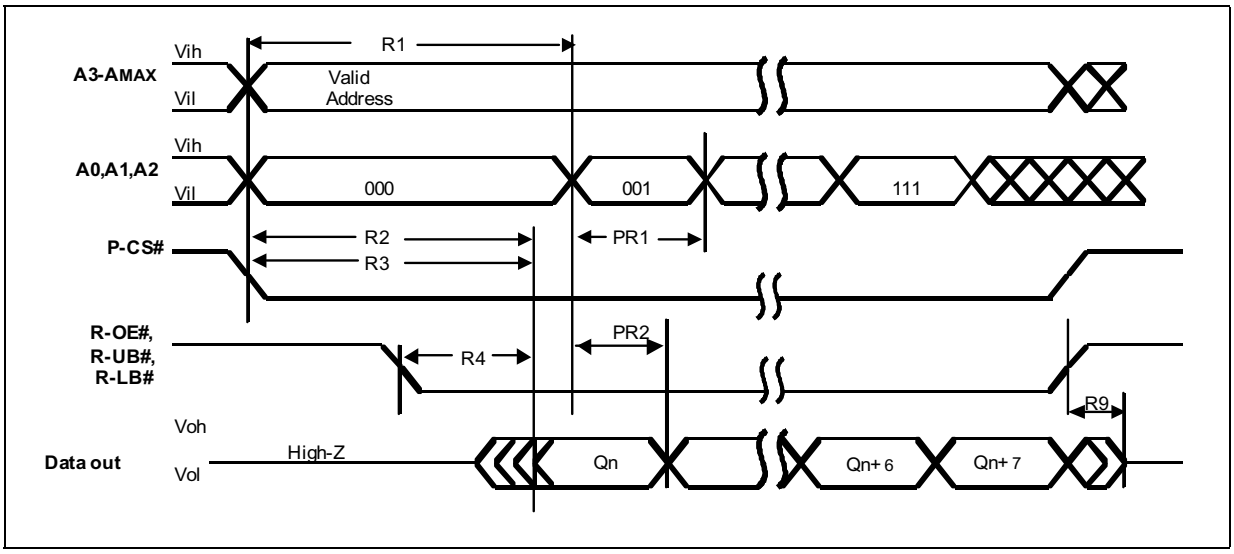


Figure 7. AC Waveform of PSRAM Read Operations



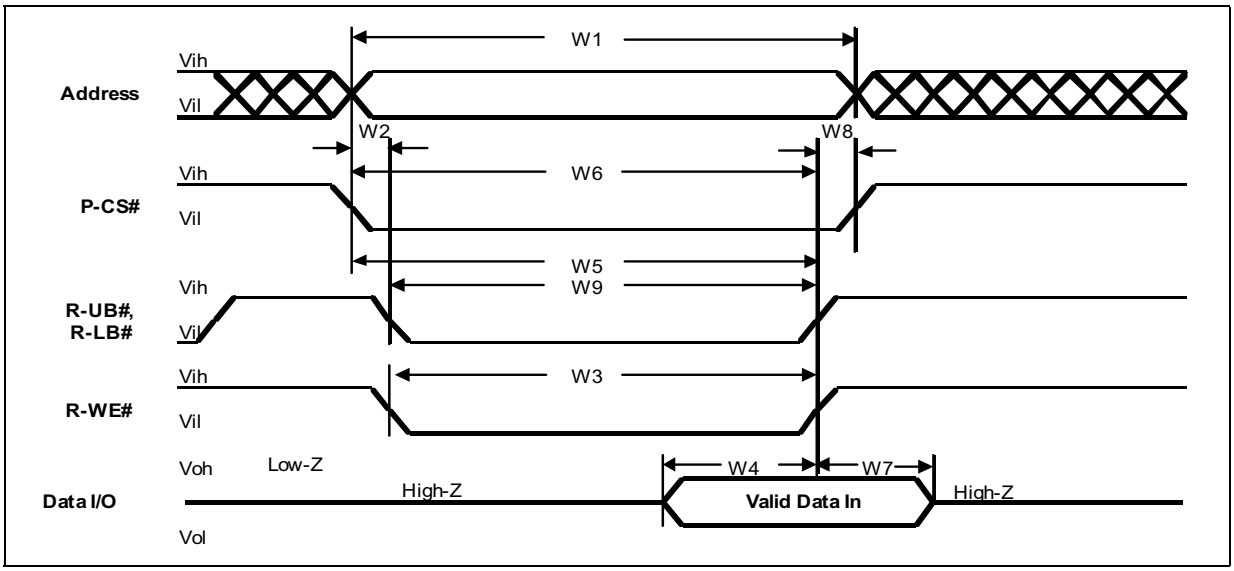
Note: In read cycle, P-Mode and R-WE# should be fixed to high level

Figure 8. AC Waveform of PSRAM 8-Word Page Read Operation



Note: In page read cycle, P-Mode and R-WE# should be fixed to high level, and R-UB#, R-LB# are low level.

Figure 9. AC Waveform PSRAM Write Operation



Notes:

1. During address transition, at least one of pins P-CS#, R-WE#, or both of R-UB# and R-LB# pins should be inactivated.
2. Do not input data to the I/O pins while they are in the output state.
3. In write cycle, P-Mode and R-OE# should be fixed to high level.
4. Write operation is done during the overlap time of a low level P-CS#, R-WE#, R-LB# and/or R-UB#.

7.3 PSRAM Operations

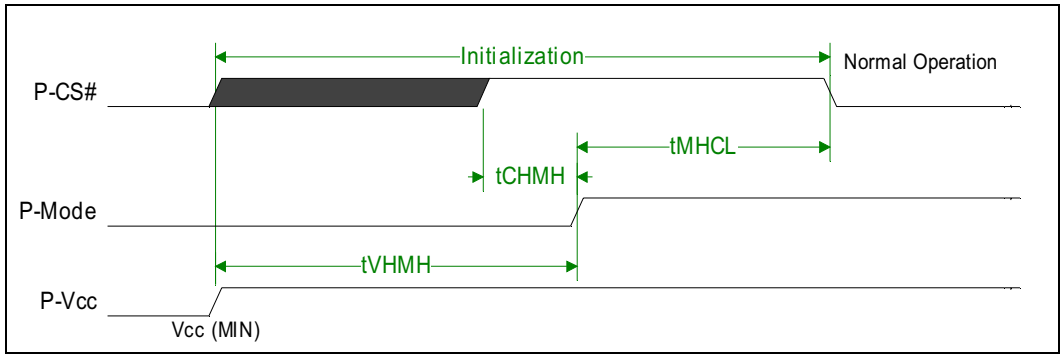
7.4 Power-up Sequence and Initialization

The PSRAM functionality and reliability are independent of the power-up slew rate of the core P-V_{CC}. Any power-up slew rate is possible under use conditions.

The following power up sequence and operation should be used before starting normal operation. The PSRAM power-up sequence is represented in Figure 10. Following power application, make P-Mode high level after fixing P-Mode to low level for the period of t_{VHMH}. Make P-CS# high level before making P-Mode high level. Then, P-CS# and P-Mode are fixed to high level for the period of t_{MHCL}.

Normal Operation is possible once the power up sequence is complete.

Figure 10. Timing Waveform for Power up sequence



Notes:
1. Make P-Mode low level when starting the power supply.
2. t_{VHMH} is specified from when the power supply voltage reaches the prescribed minimum value (P-Vcc (MIN))

Table 11. Initialization timing

Parameter	Symbol	MIN	MAX	Unit
Power application to P-Mode low level hold	t_{VHMH}	50		us
P-CS# high level to P-Mode high level	t_{CHMH}	0		ns
Following power application, P-Mode high level hold to P-CS# low level	t_{MHCL}	200		us

7.5 Mode Register

The PSRAM die has an internal register that helps control the Low Power mode of the PSRAM. This register is called the Mode register, or Mode register. The densities that can be selected for performing refresh are 16 Mbits, 8 Mbits, 4 Mbits and 0 Mbit. The density for performing refresh can be set with the Mode register. Once the refresh density has been set in the Mode register, these

settings are retained until they are set again, while applying the power supply. However, the Mode register setting will become undefined if the power is turned off, so set the Mode register again after power application.

7.5.1 Mode Register Setting

Since the initial value of the Mode register at power application is undefined, be sure to set the Mode register after initialization at power application. When setting the density of partial refresh, data before entering the Low Power Mode is not guaranteed.(This is the same for re-setup) However, since Low Power Mode is not entered unless P-Mode=L, when partial refresh is not used, it is not necessary to set the Mode register. Moreover, when using page read without using partial refresh, it is not necessary to set the Mode register.

The Mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address. The Mode register setting is a continuous four-cycle operation -two read cycles and two writes cycles. See Table 12 for setting Mode register command sequence.

Table 12. Setting Mode Register Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
Partial refresh density	Address	Data	Address	Data	Address	Data	Address	Data
16 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	04H
8 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	05H
4 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	06H
0 Mbit	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	07H

For the timing chart and flow chart, refer to Figure 11 and Figure 12.

Figure 11. Mode Register Update--Timing Waveform

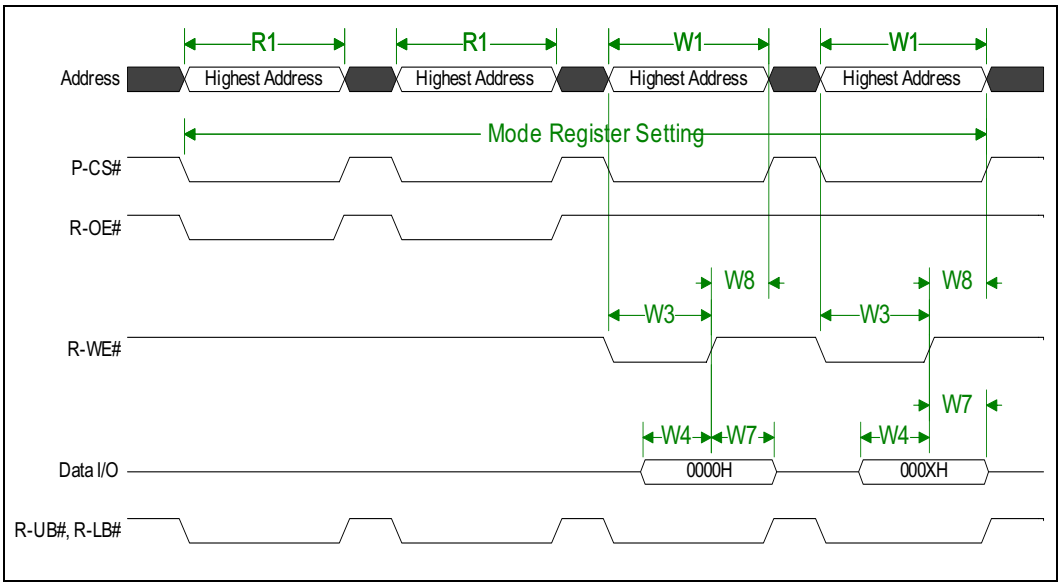
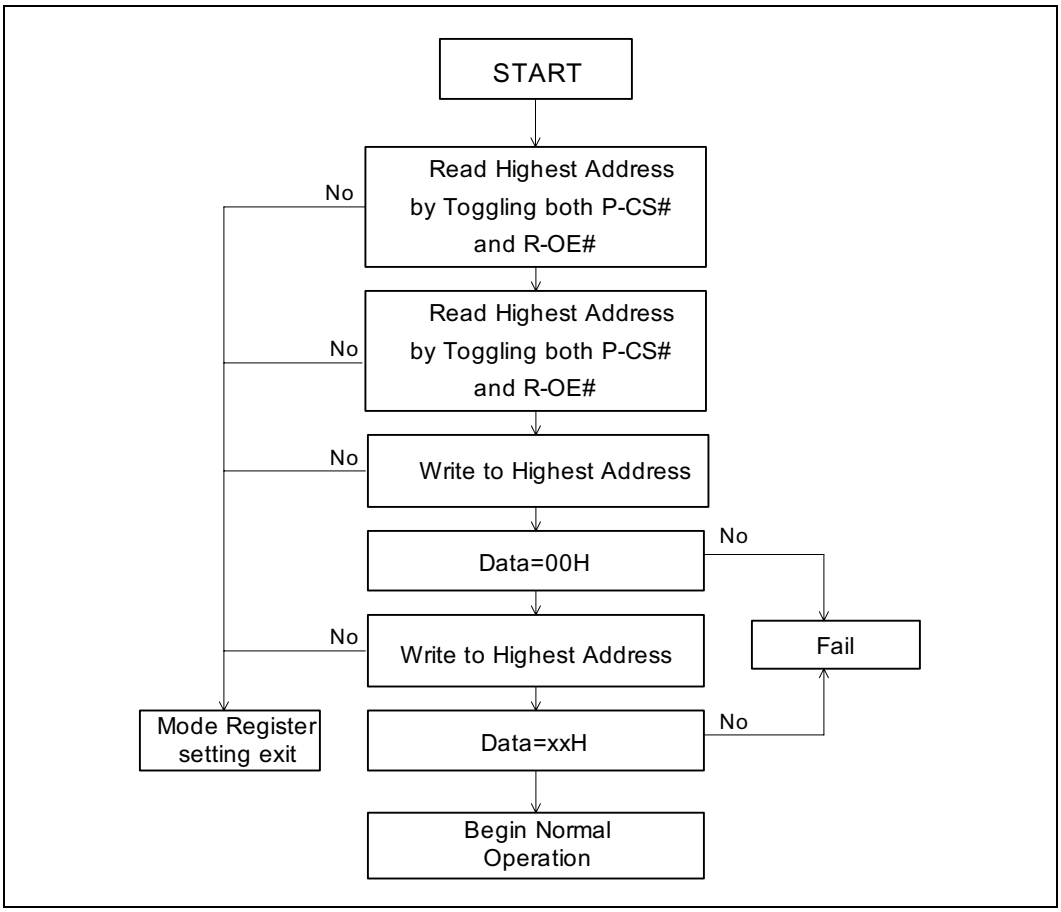


Figure 12. Mode Register Setting Flow Chart



Note: xxH=04H, 05H, 06H or 07H

7.5.2 Cautions for setting Mode Register

Since, for the Mode register setting, the internal counter status is judged by toggling P-CS# and R-OE#, toggle P-CS# at every cycle during entry (read cycle twice, write cycle twice), and toggle R-OE# like P-CS# at the first and second read cycles. If incorrect addresses or data are written, or if addressed or data are written in the incorrect order, the setting of the Mode register is not performed correctly.

When the highest address is read consecutively three or more times, the Mode register setting entries are not performed correctly. (Immediately after the highest address is read, the setting of the Mode register is not performed correctly.) Perform the setting of the Mode register after power application or after accessing other than the highest address.

Once the refresh density has been set in the Mode register, these settings are retained until they are set again, while applying the power supply. However, the Mode register setting will become undefined if the power is turned off, so set the Mode register again after power application.

7.6 Low Power mode

In addition to the regular Standby mode with a full density data hold, Low Power mode performs partial density data refresh or zero density data refresh.

The Low Power mode allows customers to turn off sections of the PSRAM die to save refresh current. The PSRAM die is divided into four sections allowing certain sections to be refreshed with P-Mode tied Low.

In regular Standby mode, both P-CS# and P-Mode are high level. But in Low Power mode, P-Mode is low level. In Low Power mode, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Low Power mode. Refer to Figure 10, "Timing Waveform for Power up sequence" on page 25 for timing charts. When the density has been to set to 16 Mbits, 8 Mbits, or 4 Mbits in Low Power mode, it is not necessary to perform initialization to return to normal operation from Low Power mode. For timing charts, refer to Figure 13, "Low Power mode -Entry/Exit (16/ 8/ 4/ 0 Mbits)" .

Figure 13. Low Power mode -Entry/Exit (16/ 8/ 4/ 0 Mbits)

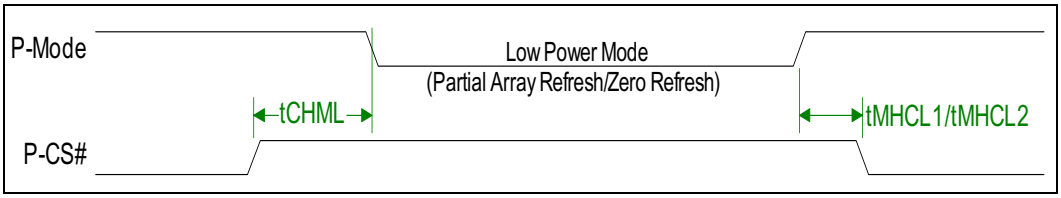


Table 13. Low Power mode-Entry/Exit

Parameter	Description	Min	Max	Unit
t_{CHML}	Low Power mode entry, P-CS# high level to P-Mode# Low level	0		ns
t_{MHCL1}	Low Power mode(16/8/4 Mbits hold) exit to normal operation, P-Mode High level to P-CS# Low level	30		ns
t_{MHCL2}	Low Power Mode(0 Mbit data hold) exit to normal operation, P-Mode High level to P-CS# Low level	200		us

Notes:

1. t_{MHCL1} is the time it takes to return to normal operation from Low Power Mode (data hold: 16 /8 /4 Mbits).
2. t_{MHCL2} is the time it takes to return to normal operation from Low Power Mode (0 Mbits data hold).

8.0 Device Operation

8.1 Bus Operations

Bus operations for the Intel® Wireless Flash Memory (W18/W30 SCSP) family involve the following chip enable and output enable signals, respectively.

- CE#1 for Flash Die#1 and CE#2 for Flash Die#2
- OE#1 for Flash Die#1 and OE#2 for Flash Die#2

All other control signals are shared between the two flash die. Table 14 to Table 15 explains the bus operations of products across this SCSP family. Refer to the W18 and W30 datasheets (order numbers 290701 and 290702) for single flash die SCSP bus operations.

Table 14. Flash Die#1 + Flash Die#2 Bus Operations

Device	Mode	RST#	CE#1	OE#1	WE#	ADV	VPP	WAIT	CE#2	OE#2	D[15:0]	Notes
Flash Die#1 Enabled	Sync Array Read	H	L	L	H	L	X	Active	H	X	Flash D_{OUT}	2,3,4
	All Async / Sync Non-Array Read	H	L	L	H	X	X	Asserted	H	X	Flash D_{OUT}	1,3,4,5
	Write	H	L	H	L	X	V_{PP1} or V_{PP2}	Asserted	H	X	Flash D_{IN}	3,4,6
	Output Disable	H	L	H	H	X	X	Active	X	X	Flash High-Z	4
	Standby	H	H	X	X	X	X	High-Z	X	X	Flash High-Z	4
	Reset	L	X	X	X	X	X	High-Z	X	X	Flash High-Z	4

Device	Mode	RST#	CE#1	OE#1	WE#	ADV	VPP	WAIT	CE#2	OE#2	D[15:0]	Notes
Flash Die#2 Enabled	Sync Array Read	H	H	X	H	L	X	Active	L	L	Flash D_{OUT}	2,3,4
	All Async / Sync Non-Array Read	H	H	X	H	X	X	Asserted	L	L	Flash D_{OUT}	1,3,4,5
	Write	H	H	X	L	X	V_{PP1} or V_{PP2}	Asserted	L	H	Flash D_{IN}	3,4,6
	Output Disable	H	X	X	H	X	X	Active	L	H	Flash High-Z	4
	Standby	H	X	X	X	X	X	High-Z	H	X	Flash High-Z	4
	Reset	L	X	X	X	X	X	High-Z	X	X	Flash High-Z	4

Notes:
1. For asynchronous read operation, both die may be simultaneously selected, but may not simultaneously drive the memory bus. See Section 8.2, "Flash Command Definitions" on page 32 for details regarding Flash selection overlap.
2. WAIT is only active during synchronous Flash reads. WAIT is driven if CE# is asserted. Refer to the Intel® Wireless Flash Memory (W18 and W30) datasheets (order numbers 290701 and 290702) for further information regarding WAIT Signal.
3. For either Flash die, OE#1/OE#2 and WE# should never be asserted simultaneously. If done so on a particular Flash die, OE#1/OE#2 will override WE#.
4. L means V_{IL} while H means V_{IH}. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
5. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
6. Refer to W30 datasheet for valid D_{IN} during Flash writes.

Table 15. Flash (Single Die/Dual Die) + PSRAM Bus Operations

Device	Mode	RST#	CE#X	OE#X	WE#	ADV#	VPP	WAIT	P-CS#	P-Mode	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
Flash Die(#1 or #2) Enabled	Sync Array Read	H	L	L	H	L	X	Active	PSRAM must be in High-Z					Flash D_{OUT}	1,2,3, 4,6
	All Async/ Sync Non-array Read	H	L	L	H	X	X	Asserted						Flash D_{OUT}	1,2,3, 4,6,7
	Write	H	L	H	L	L	V_{PP1} or V_{PP2}	Asserted						Flash D_{IN}	3,4,6, 8
	Output Disable	H	L	H	H	X	X	Active	Any PSRAM mode allowed					Flash High-Z	6
	Standby	H	H	X	X	X	X	High-Z						Flash High-Z	6
	Reset	L	X	X	X	X	X	High-Z						Flash High-Z	6

Table 15. Flash (Single Die/Dual Die) + PSRAM Bus Operations

Device	Mode	RST#	CE#X	OE#X	WE#	ADV#	VPP	WAIT	P-CS#	P-Mode	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
PSRAM Enabled	Read	Flash must be in High-Z						Note 2	L	H	L	H	L	PSRAM D_{OUT}	1,5
	Write								L	H	H	L	L	PSRAM D_{IN}	5
	Output Disable	Any flash mode allowed							L	H	H	H	X	PSRAM High-Z	6
	Standby								H	H	X	X	X	PSRAM High-Z	6
	Low Power Mode								X	L	X	X	X	PSRAM High-Z	6

Notes:

1. For asynchronous read operation, all dies may be simultaneously selected, but may not simultaneously drive the memory bus. For synchronous burst-mode reads, only two die (one flash and the PSRAM) may be simultaneously selected.
2. WAIT is only valid during synchronous flash reads. Refer to the discrete datasheet for detailed Wait functionality.
3. CE#X is CE#1 for Flash Die#1, CE#2 for Flash Die#2. OE#X is OE#1 for Flash Die#1, OE#2 for Flash Die#2.
4. For either flash die, OE#X and WE# should never be asserted simultaneously. If done so on a particular flash die, OE#X will override WE#.
5. For PSRAM, R-OE# and R-WE# should never be asserted simultaneously.
6. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
7. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
8. Refer to W30 datasheet for valid D_{IN} during flash writes.

8.2 Flash Command Definitions

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding Flash Command Definitions.

9.0 Flash Read Operations

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash read modes and operations.

10.0 Flash Program Operations

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash program operations.

11.0 Flash Erase Operations

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash erase operations.

12.0 Flash Security Modes

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash security modes and operations.

13.0 Flash Read Configuration Register

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash Read Configuration Register (RCR) functions and programming.

14.0 Flash Power Consumption

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for information regarding flash power considerations and consumption.

Appendix A Write State Machine

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for the Write State Machine details.

Appendix B Common Flash Interface

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for the Common Flash Interface details.

Appendix C Flash Flowcharts

Refer to the *Intel® Wireless Flash Memory (W18 and W30) Datasheets* (order number 290701 and 290702) for the flash flowchart details.

Appendix D Additional Information

Order Number	Document
290701	*Intel® Wireless Flash Memory (W18) Datasheet*
290702	*Intel® Wireless Flash Memory (W30) Datasheet*

Notes:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel® Flash memory products, software and tools, visit our website at http://developer.intel.com/design/flash.

Appendix E Ordering Information

E.1 Device Name Decoder

Figure 14 shows the decoder for products in this SCSP family with both flash and RAM. Figure 15 shows the decoder for products in this SCSP family with flash die only (no RAM).

Figure 14. Decoder for Flash + RAM SCSP Device Name

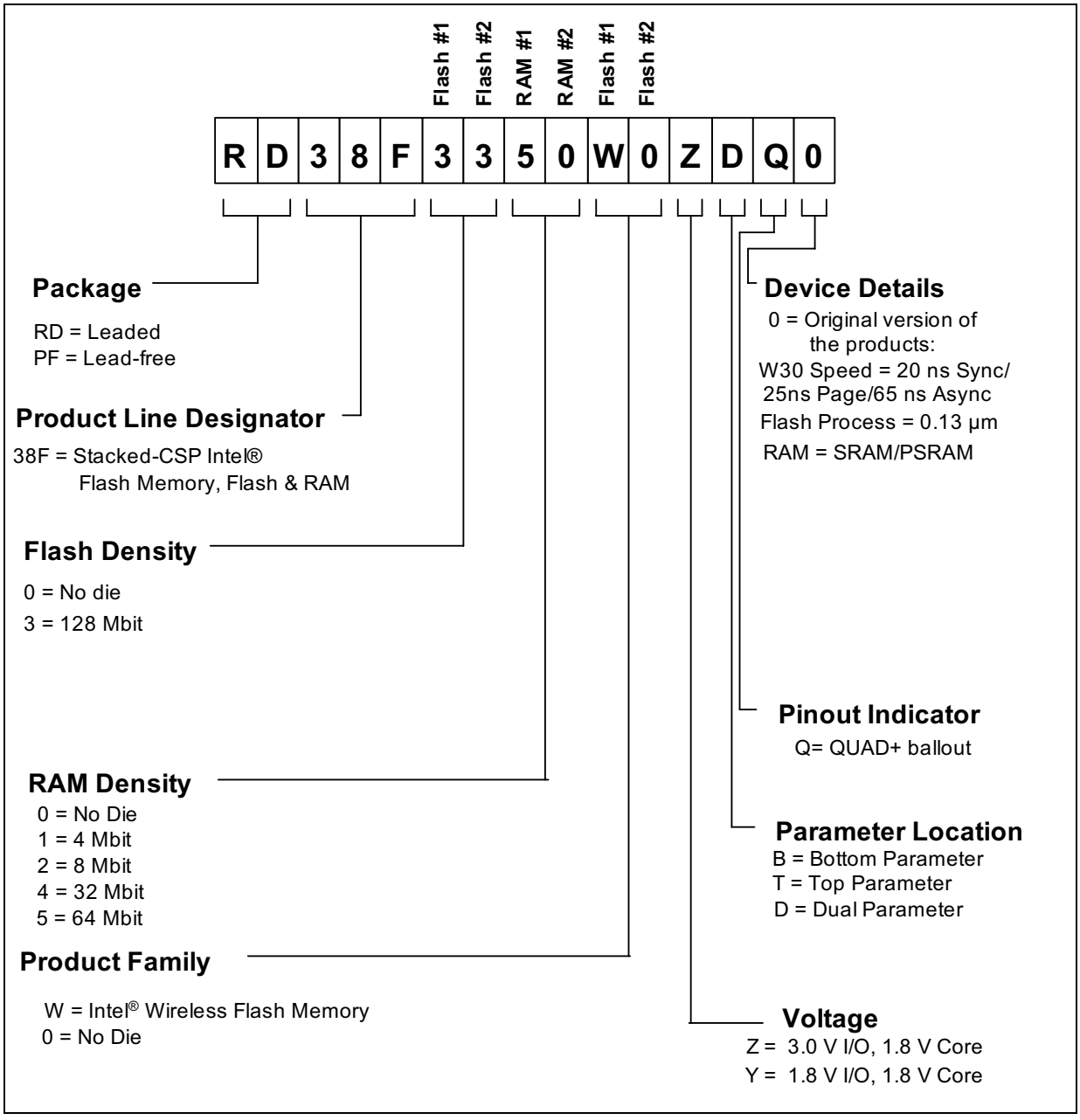
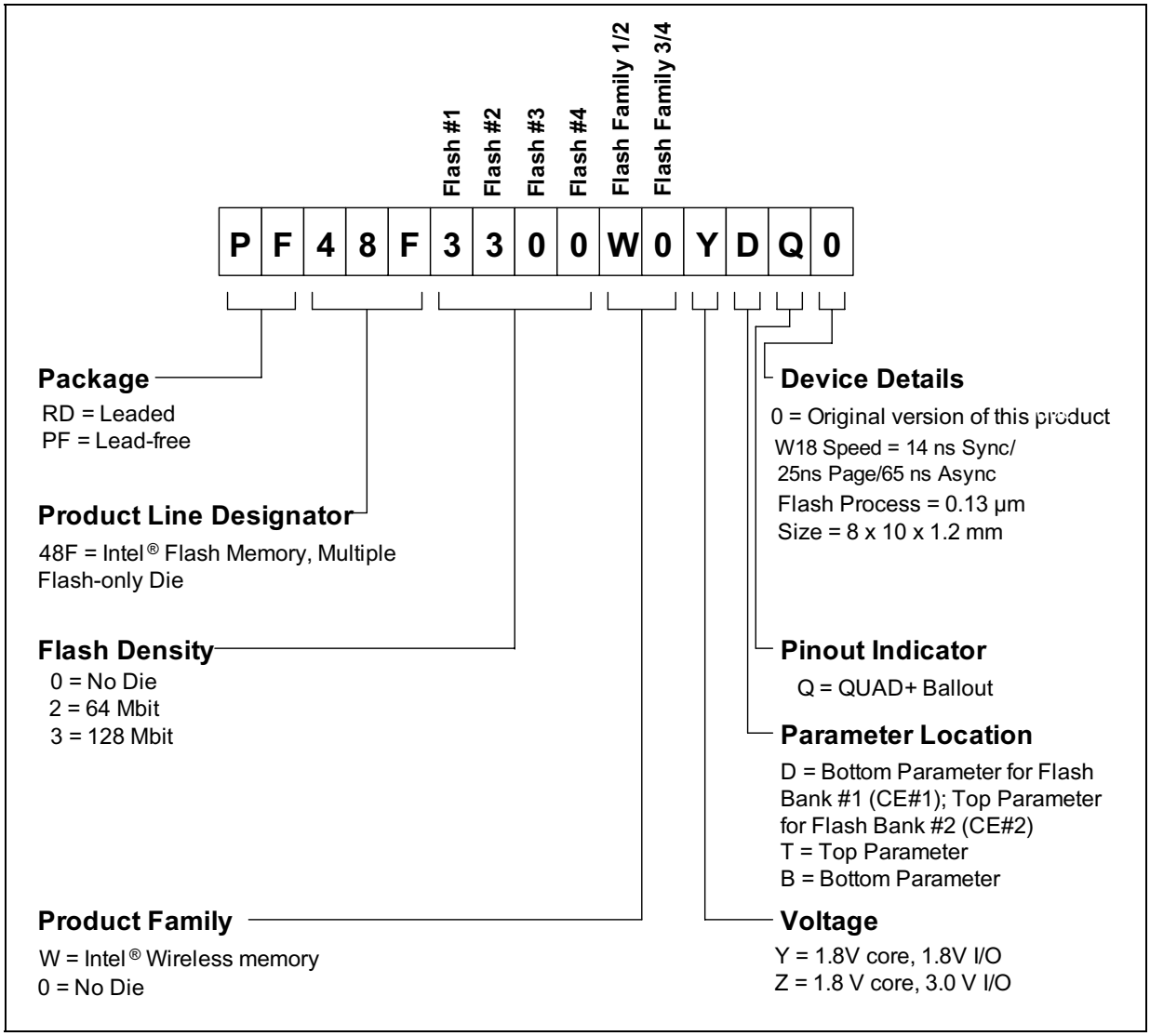


Figure 15. Decoder for Flash-Only SCSP Device Name



E.2 Device Name List

Table 16, "W18/30 SCSP Family Matrix" on page 38 shows the complete list of device names for products with double flash dies. Flash Die#1 is configured bottom parameter while Flash Die#2 is configured top parameter.

Table 16. W18/30 SCSP Family Matrix

I/O Voltage (V)	Flash	RAM	Package Size (mm)			Part Number	Notes
			Size	Ball	Type		
1.8	128W18+128W18	—	8x10x1.2	Lead-free	SCSP QUAD+	PF48F3300W0YD0	1
3.0	128W30+128W30	64PSRAM	8x10x1.4	Leaded	SCSP QUAD+	RD38F3350W0ZDQ0	1

Notes:
3. D = A 2-Die stack device, where die#1 = Bottom Parameter and Die#2 = Top Parameter.