

International  
**IR** Rectifier

**AUTOMOTIVE MOSFET**

**IRFBA1404P**

HEXFET® Power MOSFET

**Typical Applications**

- Anti-lock Braking Systems (ABS)
- Electric Power Steering (EPS)
- Electric Braking
- Radiator Fan Control

**Benefits**

- Advanced Process Technology
- Ultra Low On-Resistance
- Increase Current Handling Capability
- 175°C Operating Temperature
- Fast Switching
- Dynamic dv/dt Rating
- Repetitive Avalanche Allowed up to Tjmax

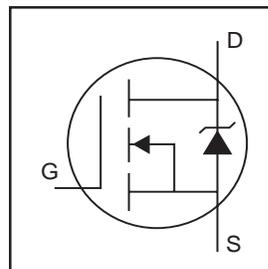
**Description**

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this MOSFET are a 175°C junction operating temperature, fast switching speed and improved ruggedness in single and repetitive avalanche. The Super-220™ is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. The result is significantly increased current handling capability over both the TO-220 and the much larger TO-247 package. The combination of extremely low on-resistance silicon and the Super-220™ package makes it ideal to reduce the component count in multiparalleled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline. This package has been designed to meet automotive, Q101, qualification standard.

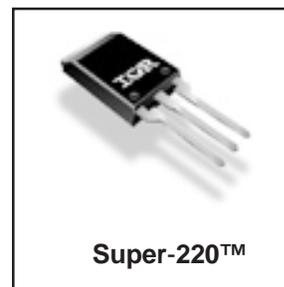
These benefits make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	206 <sup>Ⓒ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	145 <sup>Ⓒ</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>Ⓓ</sup>	650	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>Ⓔ</sup>	See Fig.12a, 12b, 15, 16	mJ
I <sub>AR</sub>	Avalanche Current <sup>Ⓓ</sup>		A
E <sub>AR</sub>	Repetitive Avalanche Energy <sup>Ⓓ</sup>	30	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>Ⓔ</sup>	5.0	V/ns
T <sub>J</sub>	Operating Junction and	-40 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to + 175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Recommended clip force	20	N

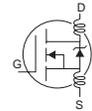


V<sub>DSS</sub> = 40V  
R<sub>DS(on)</sub> = 3.7mΩ  
I<sub>D</sub> = 206A<sup>Ⓒ</sup>



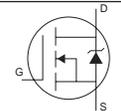
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.7	mΩ	$V_{GS} = 10V, I_D = 95A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	106	—	—	S	$V_{DS} = 25V, I_D = 60A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	160	200	nC	$I_D = 95A$
$Q_{gs}$	Gate-to-Source Charge	—	35	—		$V_{DS} = 32V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	42	60		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 20V$
$t_r$	Rise Time	—	140	—		$I_D = 95A$
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	26	—		$R_D = 0.21\Omega$ ④
$L_D$	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	5.0	—		
$C_{iss}$	Input Capacitance	—	7360	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	1680	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	240	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	6630	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	1490	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance ⑤	—	1540	—		$V_{GS} = 0V, V_{DS} = 0V\ to\ 32V$



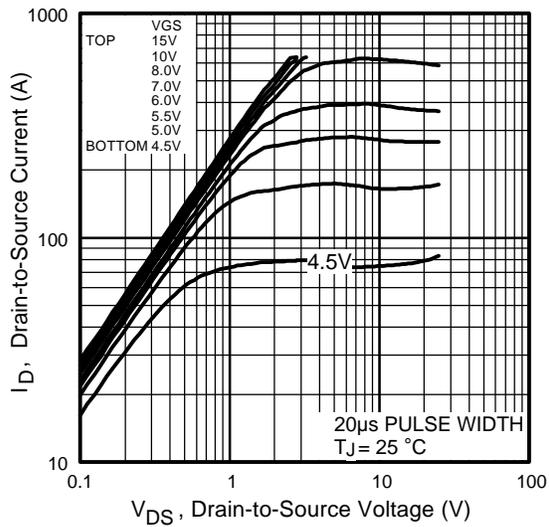
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	206	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	650		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 95A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}, I_F = 95A$
$Q_{rr}$	Reverse Recovery Charge	—	180	270	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

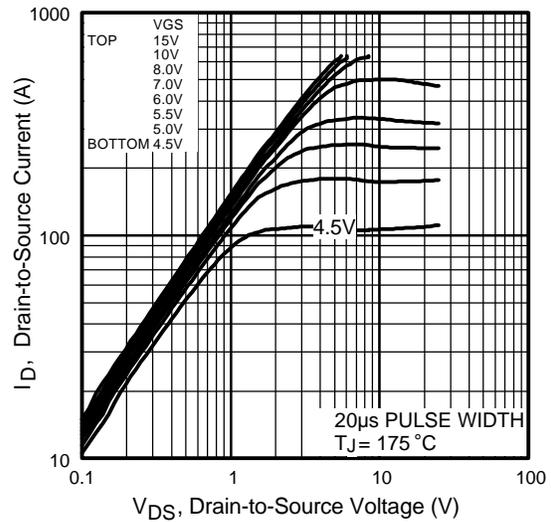


## Thermal Resistance

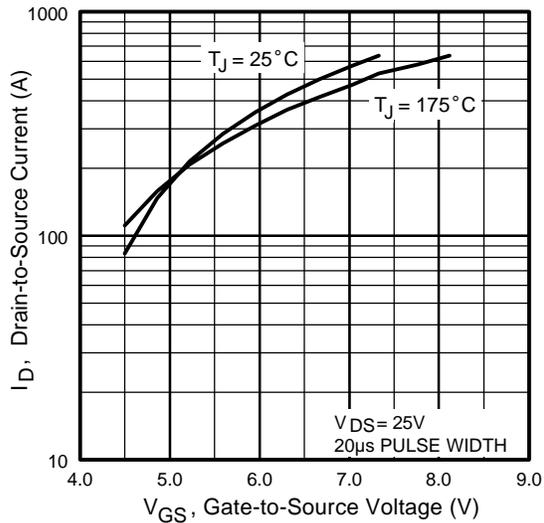
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	58	



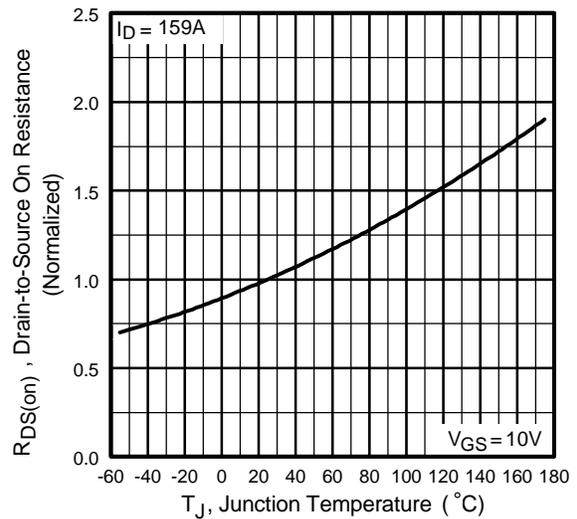
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

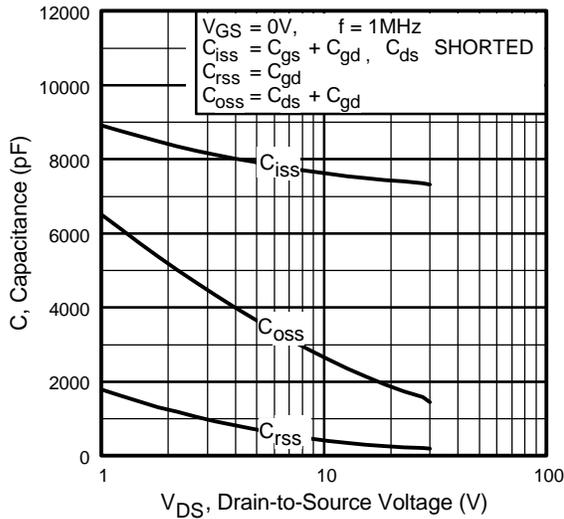


**Fig 3.** Typical Transfer Characteristics

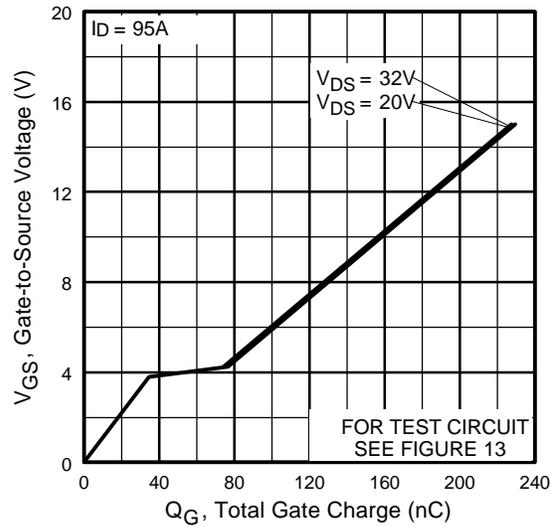


**Fig 4.** Normalized On-Resistance Vs. Temperature

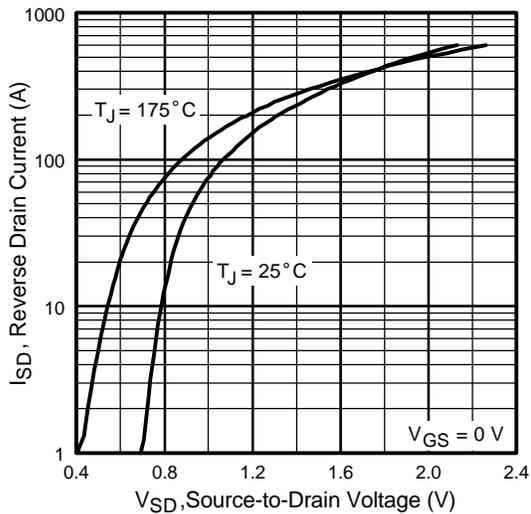
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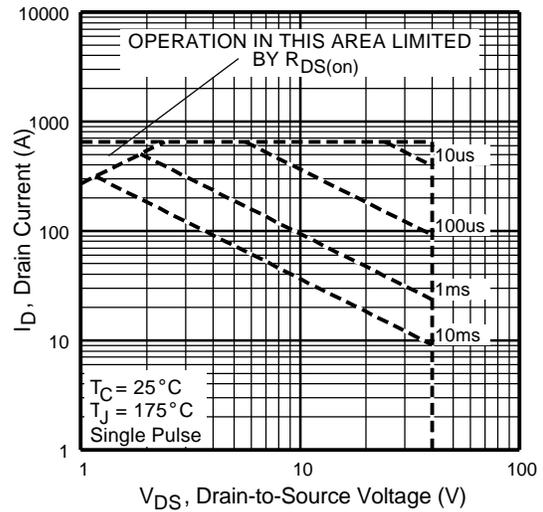
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



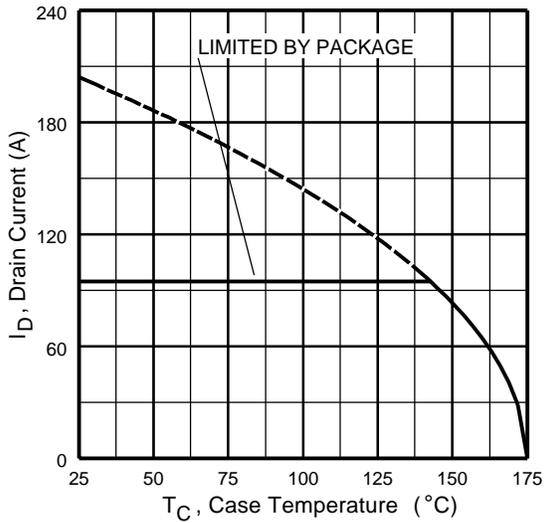
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



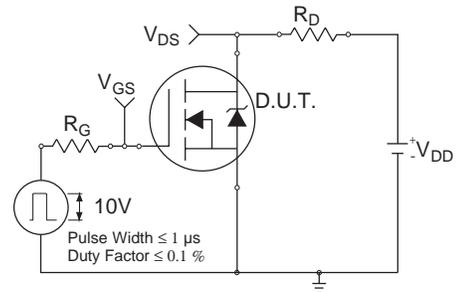
**Fig 7.** Typical Source-Drain Diode Forward Voltage



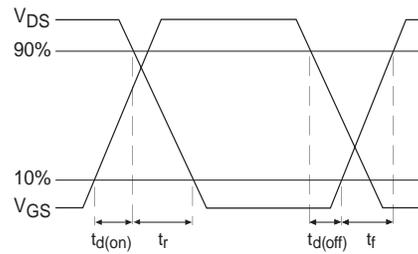
**Fig 8.** Maximum Safe Operating Area



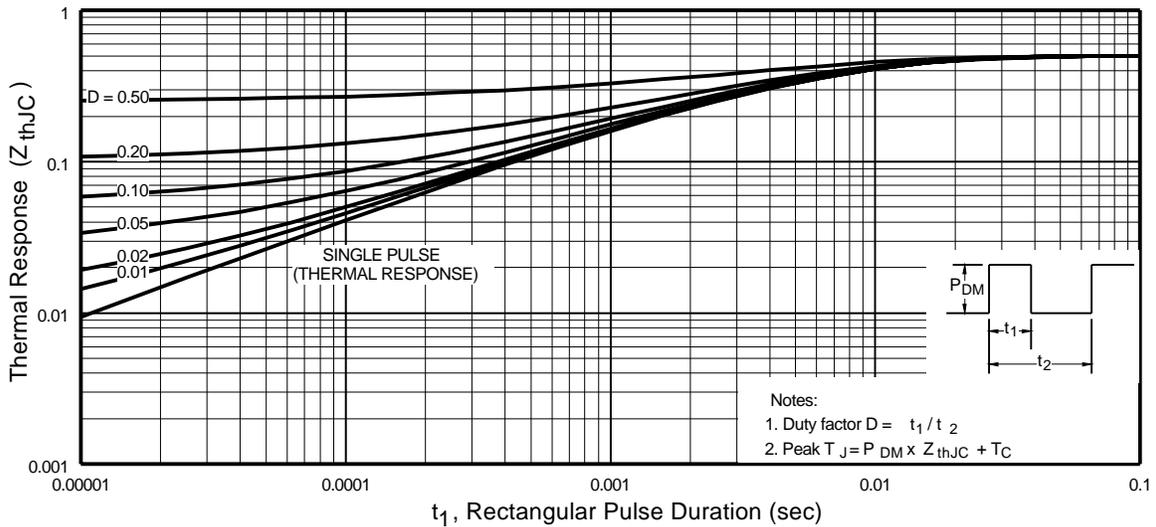
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

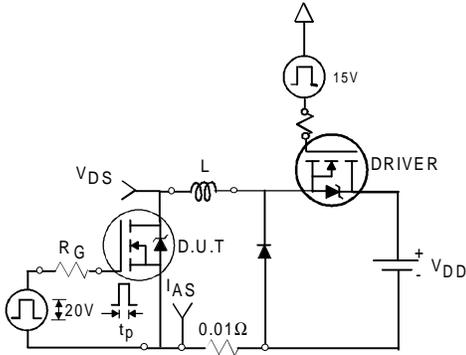


**Fig 10b.** Switching Time Waveforms

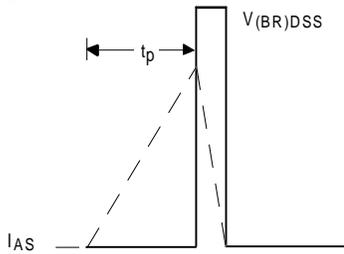


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

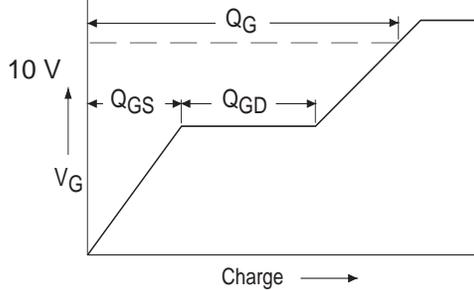
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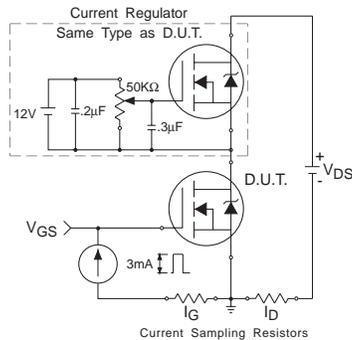
**Fig 12a.** Unclamped Inductive Test Circuit



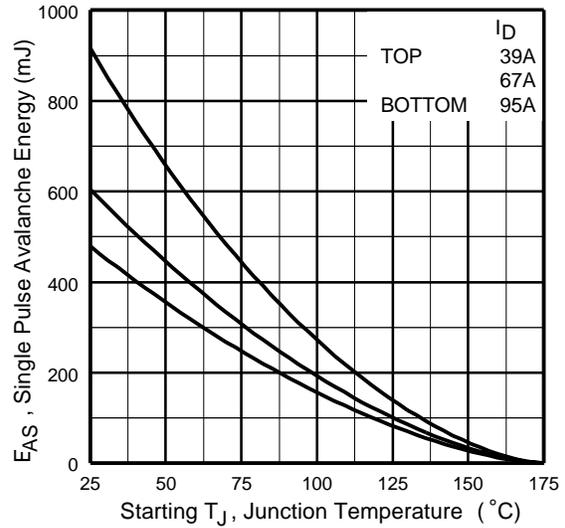
**Fig 12b.** Unclamped Inductive Waveforms



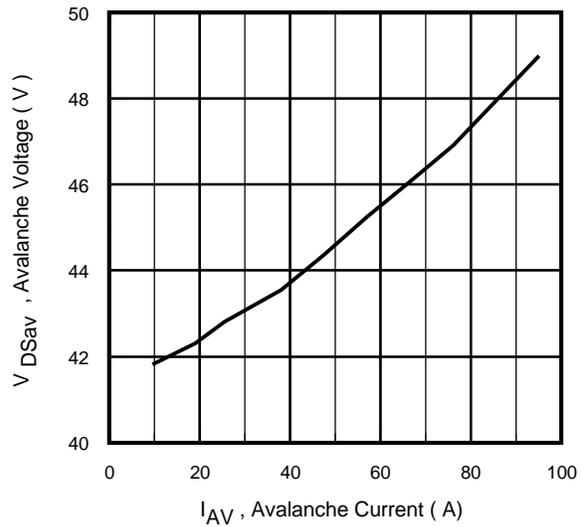
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

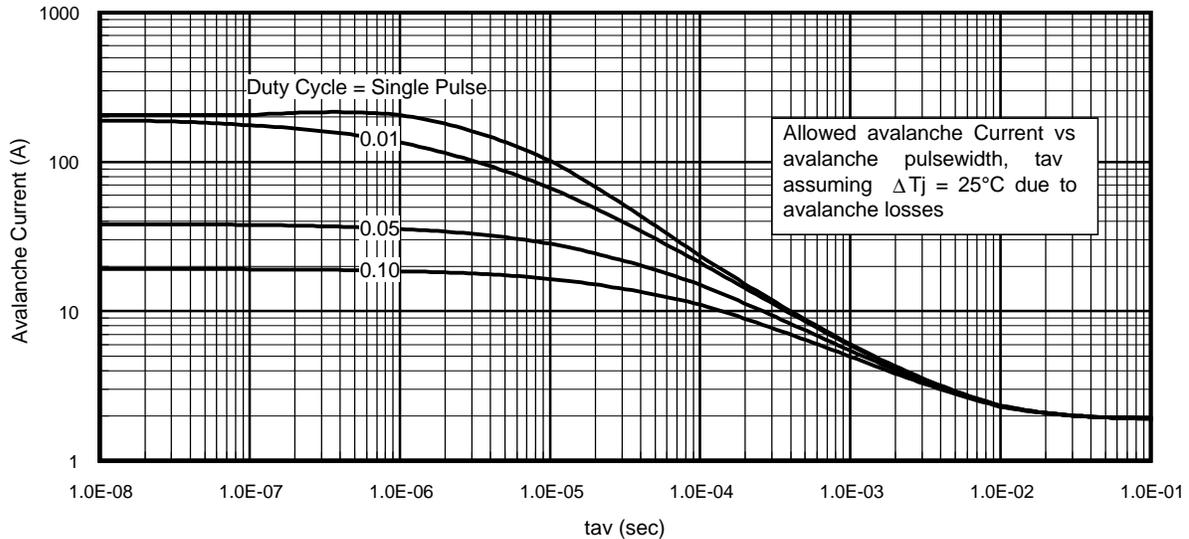


Fig 15. Typical Avalanche Current Vs.Pulsewidth

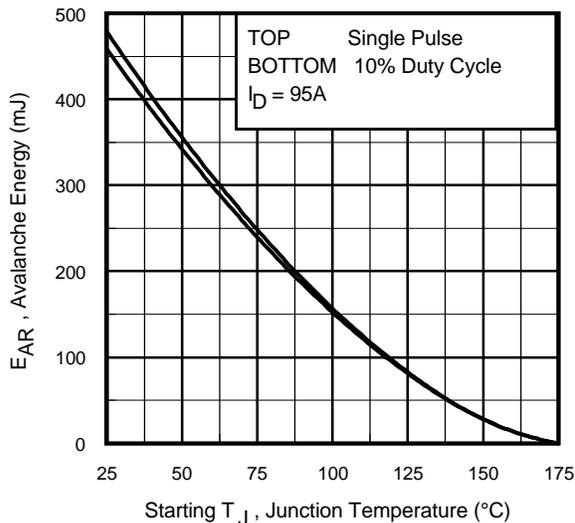


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

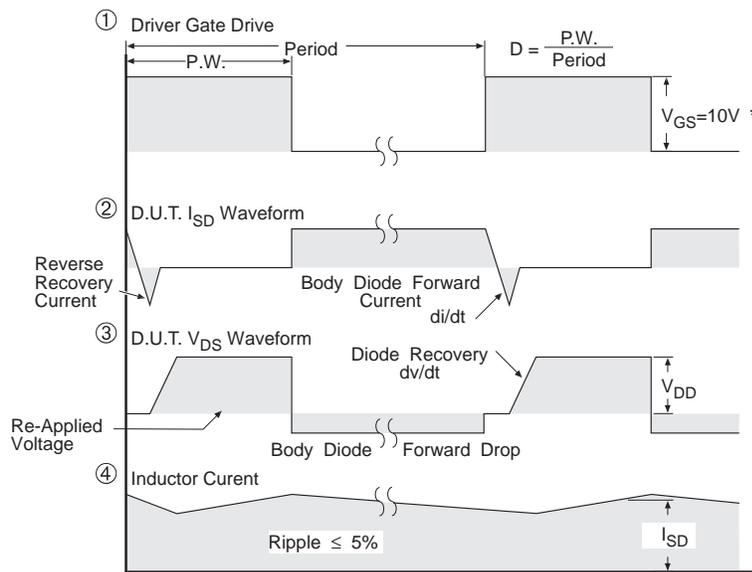
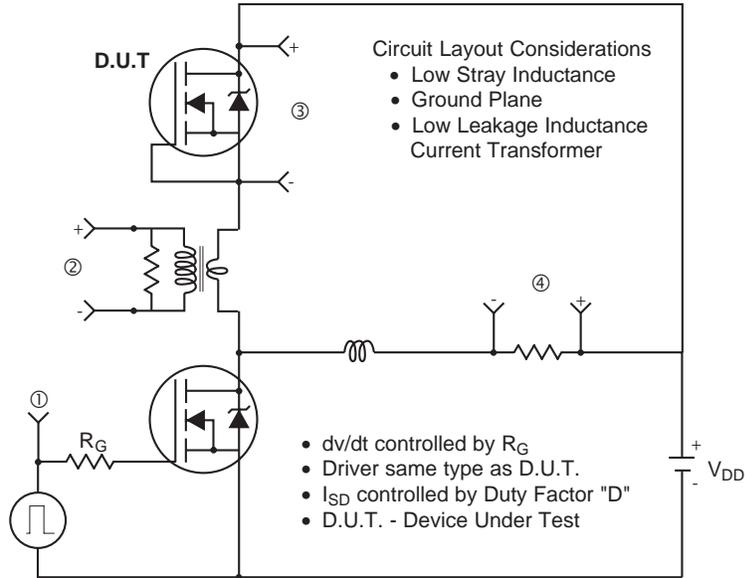
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit

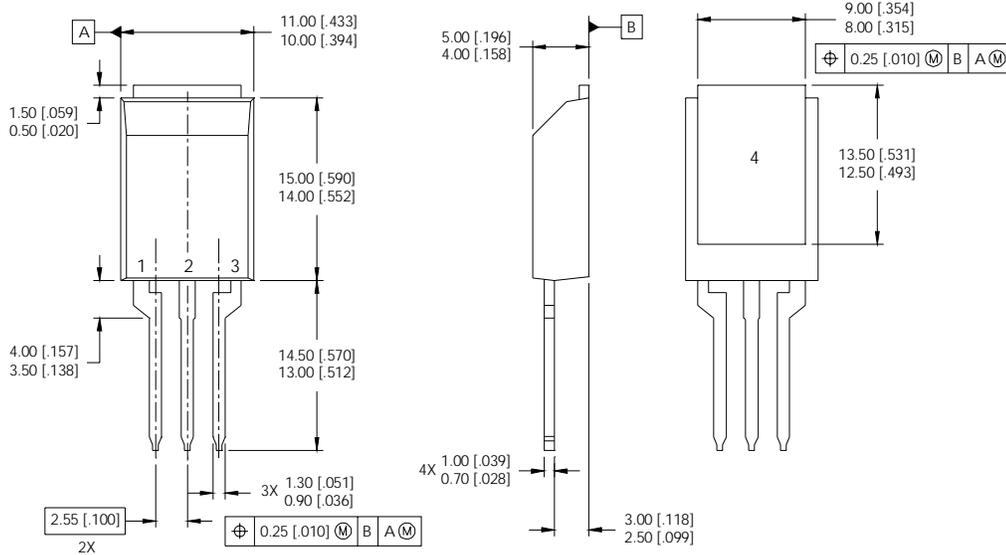


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 17.** For N-Channel HEXFET® Power MOSFETs

International  
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 Super-220™ Package Outline

# IRFBA1404P



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

**LEAD ASSIGNMENTS**

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.12\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 95\text{A}$ .
- ③  $I_{SD} \leq 95\text{A}$ ,  $di/dt \leq 150\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ . Refer to AN-1001
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
**IR EUROPEAN REGIONAL CENTRE:** 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000  
**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200  
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590  
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111  
**IR JAPAN:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086  
**IR SOUTHEAST ASIA:** 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630  
**IR TAIWAN:** 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936  
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