SINGLE-CHIP CHARGE AND SYSTEM POWER-PATH MANAGEMENT IC (bqTINY™-III)

FEATURES

- **Small 3.5 mm × 4.5 mm QFN package**
- **Designed for single-cell Li-Ion or Li-Pol based portable applications**
- **Integrated dynamic power-path management (DPPM) feature allowing the AC adapter or the USB port to simultaneously power the system and charge the battery**
- **Power supplement mode allows battery to supplement the USB or AC input current**
- **Autonomous power source selection (AC Adapter or USB)**
- **Integrated USB charge control with selectable 100-mA and 500-mA charge rates**
- **Dynamic total current management for USB**
- **Supports up to 2-A total current**
- **3.3 V Integrated LDO output**
- **Thermal regulation for charge control**
- **Charge status outputs for LED or system interface indicates charge and fault conditions**
- **Reverse current, short-circuit and thermal protection**
- **Power Good (AC adapter and USB port present) Status outputs**

APPLICATIONS

- **Smartphones and PDA**
- **MP3 players**
- **Digital cameras Handheld devices**
- **Internet appliances**

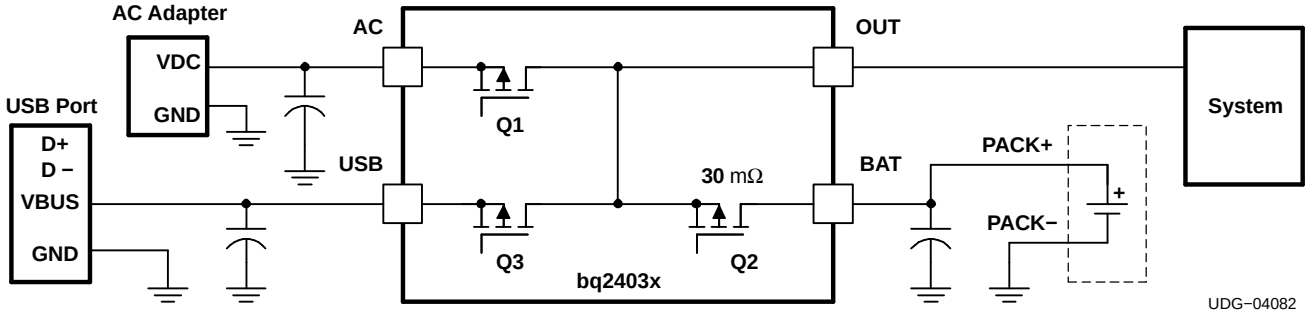
DESCRIPTION

The bqTINY-III series are highly integrated and flexible Li-Ion linear charge and system power path management devices targeted at space limited portable applications. The bqTINY-III series offer integrated USB-port and DC supply (AC adapter) and power-path management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device.

The bqTINY-III powers the system while independently charging the battery. This features reduces the charge and discharge cycles on the battery, allows for proper charge termination and allows the system to run with an absent or defective battery pack. This feature also allows for system to instantaneously turn on from an external power source in the case of a deeply discharged battery pack.

The bqTINY-III automatically selects the USB-Port or the AC-adapter as the power source for the system. In the USB configuration, the host can select from the 2 preset charge rates of 100 mA and 500 mA. The bqTINY-III dynamically adjusts the USB charge rate based on system load to stay within the 100 mA or 500 mA charge rates. In the ac-adapter configuration an external resistor sets the magnitude of the charge current. The AC input can also be programmed using the PSEL pin to perform like a USB input.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOSFET gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE (V)	OUT PIN FOR AC INPUT CONDITIONS	PART NUMBER(1)(2)	STATUS	PACKAGE MARKING
-40°C to 125°C	4.2	Regulated to 6 V	bq24030RHLR	Preview	ANB
	4.2	Regulated to 4.4 V	bq24032RHLR	Released	AMZ
	4.2	Cut off at 6 V	bq24035RHLR	Preview	ANA

(1) The RHL package isavailable taped and reeled only in quantities of 3,000 devices perreel.
(2) This product is RoHScompatible, including a lead concentration that does not exceed 0.1% of totalproduct weight, and is suitable for use in specified lead-free solderingprocesses. In addition, this product uses package materials that do not containhalogens, including bromine (Br) or antimony (Sb) above 0.1% of total productweight.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		bq24030 bq24032 bq24035	UNIT
Input voltage	AC (DC voltage wrt VSS)	-0.3 to 18	V
Input voltage	BAT, CE, DPPM, $\overline{ACPG}$, PSEL, OUT, ISET1, ISET2, STAT1, STAT2, TS, $\overline{USBPG}$ (all DC voltages wrt VSS)	-0.3 to 7	
	LDO (DC voltage wrt VSS)	-0.3 to $V_{O(OUT)}$ + 0.3	
Input current	AC	2.75	A
	USB	600	mA
Output current	OUT	4	A
	BAT(2)	-4 to 1.75	
Output source current (in regulation at 3.3 V LDO)	LDO	30	mA
Output sink current	$\overline{ACPG}$, STAT1, STAT2, $\overline{USBPG}$,	1.5	
Storage temperature range, T_{stg}		-65 to 150	°C
Junction temperature range, T_J		-40 to 150	
Lead temperature (solderig, 10 seconds)		300	

(1) Stresses beyond thoselisted under "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect device reliability. All voltagevalues are with respect to the network ground terminal unless otherwisenoted.
(2) Negative current isdefined as current flowing into the BAT pin.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage (from AC input) (1)(2)	4.35	16.00	V
V_{CC}	Supply voltage (from USB input) (1)	4.35	6.5	
I_{AC}	Input current, AC		2	A
I_{USB}	Input current, USB		0.5	
T_J	Operating junction temperature range	-40	125	°C

(1) V_{CC} is defined as the greater of AC or USBinput.
(2) Verify that powerdissipation and junction temperatures are within limits at maximum V_{CC} .

DISSIPATION RATINGS

PACKAGE	$T_A \leq 40°C$ POWER RATING	DERATING FACTOR $T_A > 40°C$	θ_{JA}
20-pin RHL(1)	1.81 W	21 mW/°C	46.87 °C/W

(1) This data is based onusing the JEDEC High-K board and the exposed die pad is connected to a Cu padon the board. This is connected to the ground plane by a 2×3 viamatrix.

ELECTRICAL CHARACTERISTICS

over junction temperature range ($0°C \leq T_J \leq 125°C$) and the recommended supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT							
$I_{CC(SPLY)}$	Active supply current, VCC		$V_{VCC} > V_{VCC(min)}$		1	2	mA
$I_{CC(SLP)}$	Sleep current (current into BAT pin)		$V_{(AC)} < V_{(UVLO)}$, $V_{(USB)} < V_{(UVLO)}$, $2.6\ V \leq V_{I(BAT)} \leq V_{O(BAT-REG)}$, Excludes load on OUT pin		2	5	µA
$I_{CC(AS-STDBY)}$	AC standby current		$V_{I(AC)} \leq 6V$, Total current into AC pin with chip disabled, Excludes all loads, (1) CE=LOW, after $t_{(CE-HOLDOFF)}$ delay			200	
$I_{CC(USB-STDBY)}$	USB standby current		Total current into USB pin with chip disabled, Excludes all loads, (1)CE=LOW, after $t_{(CE-HOLDOFF)}$ delay			200	
$I_{CC(BAT-STDBY)}$	BAT standby current		Total current into BAT pin with AC and/or USB present and chip disabled, Excludes all loads, CE=LOW, after $t_{(CE-HOLDOFF)}$ delay(1)		45	60	
$I_{IB(BAT)}$	Charge done current, BAT		Charge DONE, AC or USB supplying the load		1	5	
LDO OUTPUT							
$V_{O(LDO)}$	Output regulation voltage		Active only if AC or USB is present, $V_{I(OUT)} \geq V_{O(LDO)} + (I_{O(LDO)} \times R_{DS(on)})$		3.3		V
	Regulation accuracy			(2)-5%		5%	
$I_{O(LDO)}$	Output current					20	mA
$R_{DS(on)}$	On resistance		OUT to LDO			50	Ω
$C_{(OUT)}$	Output capacitance					(3)1	µF
OUT TERMINAL AND DPPM MODE							
$V_{O(OUT-REG)}$	Output regulation voltage	bq24030	$V_{I(AC)} \geq 6\ V + V_{DO}$		6.0	6.3	V
		bq24032	$V_{I(AC)} \geq 4.4\ V + V_{DO}$		4.4	4.5	
$V_{(DPPM-SET)}$	DPPM set point(4)			2.6		3.7	
$I_{(DPPM-SET)}$	DPPM current source		AC or USB present	95	100	105	µA

(1) This includes thequiescent current for the integrated LDO.
(2) In standby mode (CElow) the accuracy is ±10%.
(3) LDO output capacitornot required but one with a value of 0.1-µF is recommended.
(4) $V_{(DPPM-SET)}$ is scaled up by the scale factor forcontrolling the output voltage $V_{(DPPM-REG)}$.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SF	DPPM scale factor	$V_{(DPPM-REG)}$ = $V_{(DPPM-SET)}$ × SF	1.139	1.150	1.162	V
	DPPM disable set point		1.8	2.0	2.2	
$V_{(ACDO)}$	AC to OUT dropout voltage (5)	$V_{I(AC)}$ ≥ $V_{CC(min)}$, PSEL=High, $I_{I(AC)}$ = 1 A, ($I_{O(OUT)}$+$I_{O(BAT)}$)		300	475	mV
$V_{(usbDO)}$	USB to OUT dropout voltage	$V_{I(USB)}$ ≥ $V_{CC(min)}$, PSEL=Low, ISET2 = High $I_{I(USB)}$ = 0.4 A, ($I_{O(OUT)}$+$I_{O(BAT)}$)		140	180	
		$V_{I(USB)}$ ≥ $V_{CC(min)}$, PSEL=Low, ISET2 = Low $I_{I(USB)}$ = 0.08 A, ($I_{O(OUT)}$+$I_{O(BAT)}$)		28	36	
	Enter battery supplement mode (battery supplements OUT current in the presence of input source	$V_{I(BAT)}$ > 2 V	$V_{I(OUT)}$ ≤ $V_{I(BAT)}$ - 60 mV			V
	Exit battery supplement mode	$V_{I(BAT)}$ > 2 V			$V_{I(OUT)}$ ≥ $V_{I(BAT)}$ - 20 mV	
	BAT to OUT short circuit recovery	Series resistor between BAT to OUT for short circuit recovery to $V_{I(OUT)}$ ≤ $V_{I(BAT)}$ -200mV		10		mA
	AC to OUT short circuit limit	$V_{I(OUT)}$ ≤ 1 V		500		Ω
	USB to OUT short circuit limit	$V_{I(OUT)}$ ≤ 1 V		500		
BATTERY CHARGE VOLTAGE REGULATION, $V_{O\ (BAT-REG)}$ + $V_{(DO-MAX)}$ < V_{CC}, I_{TERM} < $I_{BAT(OUT)}$ ≤ 1 A						
$V_{O(BAT-REG)}$	Battery charge voltage			4.2		V
	Battery charge voltage regulation accuracy	T_A = 25°C	--0.5%		0.5%	
			-1%		1%	
$V_{(DO)}$	BAT to OUT dropout voltage (discharging)	$V_{I\ (BAT)}$ ≥ 3 V, $I_{i(BAT)}$ = 1.0 A, V_{CC} < $V_{i(BAT)}$		30	100	mV
$V_{(DO)}$	USB dropout voltage	3.0 V ≤ $V_{O(BAT)}$ < $V_{O(BAT-REG)}$, $I_{I(BAT)}$ = 1 A, 1 A current source on AC input, $V_{I(DPPM)}$ < 2.2 V		30	100	
CURRENT REGULATION						
$I_{O(BAT)}$	AC battery charge current range (6)(7)	V_{VCC} ≥ 4.35 V, $V_{i\ (BAT)}$ > $V_{(LOWV)}$, $V_{I(OUT)}$ - $V_{I\ (BAT)}$ > $V_{(DO-MAX)}$, PSEL = High $I_{OUT(BAT)}$ = ($K_{(SET)}$ × $V_{(SET)}$ / R_{SET}),	100	1000	1500	mA
	AC to OUT and USB to OUT short-circuit pull-up	$V_{I(OUT)}$ < 1 V		500		Ω
$V_{(SET)}$	Battery charge current set voltage (8)	Voltage on ISET1, V_{VCC} ≥ 4.35 V, $V_{I(OUT)}$ - $V_{I(BAT)}$ > $V_{(DO-MAX)}$, $V_{I(BAT)}$ > $V_{(LOWV)}$	2.475	2.500	2.525	V
$K_{(SET)}$	Charge current set factor, BAT	100 mA ≤ $I_{O(BAT)}$ ≤ 1 A	400	425	450	
		10 mA ≤ $I_{O(BAT)}$ ≤ 100 mA (9)	300	450	600	

(5) $V_{DO(max)}$, dropout voltage is a function of the FET,$R_{DS(on)}$, and drain current. the dropoutvoltage increases proportionally to the increase in current.
(6) When input currentremains below 2 A, the battery charging current may be raised until the thermalregulation limits the charge current.
(7) When PSEL is pulledlow, and $\overline{\text{USBPG}}$ is high, the AC inputfunctions as a USB input.
(8) For half-chargerate, $V_{(SET)}$ is 1.25 V ± 25mV.
(9) Specification is formonitoring charge current via the ISET1 pin during voltage regulation mode, notfor a reduced fast charge level.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	USB input current range	$V_{VCC(min)}$ ≥ 4.35 V, $V_{I(BAT)}$ > $V_{(LOWV)}$, $V_{I(USB)}$ - $V_{I(BAT)}$ > $V_{(DO-MAX)}$, ISET2= Low, PSEL = Low(10)	80		100	mA
		$V_{VCC(min)}$ ≥ 4.35 V, $V_{I(BAT)}$ > $V_{(LOWV)}$, $V_{I(USB)}$ - $V_{I(BAT)}$ > $V_{(DO-MAX)}$, ISET2= High, PSEL = Low(11)	400		500	
PRECHARGE and SHORT-CIRCUIT CURRENT REGULATION						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	Voltage on BAT	2.9	3.0	3.1	V
	Deglitch time for fast-charge to precharge transition(12)	$V_{VCC(min)}$ ≥ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, $V_{I(BAT)}$ decreasing below threshold		22.5		ms
$I_{O(PRECHG)}$	Precharge range	1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$, $I_{O(PRECHG)}$ = ($K_{(SET)}$× $V_{(PRECHG)}$)/ R_{SET}	10		150	mA
$V_{(PRECHG)}$	Precharge set voltage	1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	230	250	270	mV
	Short circuit pull-up, BAT	$V_{I(BAT)}$ ≤ 1 V		1		kΩ
CHARGE TAPER DETECTION						
$I_{(TAPER)}$	Charge taper detection range	$V_{I(BAT)}$ < $V_{(RCH)}$, $I_{(TAPER)}$ = ($K_{(SET)}$× $V_{(TAPER)}$)/ R_{SET}	10		150	mA
$V_{(TAPER)}$	Charge taper detection set voltage	Voltage on ISET1, $V_{REG(BAT)}$ = 4.2 V, $V_{I(BAT)}$ > $V_{(RCH)}$	235	250	265	mV
	Deglitch time for taper detection	$V_{VCC(min)}$ ≥ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} increasing above or decreasing below threshold		22.5		ms
TEMPERATURE SENSE COMPARATORS						
V_{HTF}	High voltage threshold		2.465	2.500	2.535	V
V_{LTF}	Low voltage threshold		0.485	0.500	0.515	V
I_{TS}	Temperature sense current source		94	100	106	µA
	Deglitch time for temperature fault detection(12)	$V_{VCC(min)}$ ≥ 4.5 V, $R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing above and below; 100-ns fall time, 10-mv overdrive		22.5		ms
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage		$V_{O(BAT-REG)}$ -0.075	$V_{O(BAT-REG)}$ -0.100	$V_{O(BAT-REG)}$ -0.125	V
	Deglitch time for recharge detection(12)	$V_{VCC(min)}$ ≥ 4.5 V, $R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing below threshold, 100-ns fall time, 10-mv overdrive		22.5		ms
STAT1, STAT2. $\overline{\text{ACPG}}$ AND $\overline{\text{USBPG}}$ OUTPUTS						
V_{OL}	Low-level output saturation voltage	I_{OL} = 5 mA			0.25	V
	Input leakage current			1	5	µA
ISET2, CE AND PSEL INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			

(10) With the PSEL= low,the bqTINY-III defaults to USB charging. If USB input is grounded, then thebqTINY-III charges from the AC input at the USB charge rate. In thisconfiguration the specification is 75 mA (min) and 95 mA (max).
(11) With the PSEL= low,the bqTINY-III defaults to USB charging. If USB input is grounded, then thebqTINY-III charges from the AC input at the USB charge rate. In thisconfiguration the specification is 375 mA (min) and 475 mA (max).
(12) All deglitch periodsare a function of the timer setting.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current, CE or PSEL		-1			µA
I_{IH}	High-level input current, CE or PSEL				1	
I_{IL}	Low-level input current, ISET2	V_{ISET2} = 0 V	-20			
I_{IH}	High-level input current, ISET2	V_{ISET2} = V_{CC}			40	
$t_{(CE-HLDOFF)}$	Hold off time, CE	CE going low only	4		6	
TIMERS						
$K_{(TMR)}$	Timer set factor	$t_{(CHG)}$ = $K_{(TMR)}$ × $R_{(TMR)}$	0.313	0.360	0.414	s/Ω
$R_{(TMR)}$	External resistor limits		30		100	kΩ
$t_{(PRECHG)}$	Precharge timer		0.09 × $t_{(CHG)}$	0.01 × $t_{(CHG)}$	0.11 × $t_{(CHG)}$	s
$I_{(FAULT)}$	Timer fault recovery pull-up from OUT to BAT			1		mA
CHARGER SLEEP THRESHOLDS						
$V_{(SLPENT)}$	Sleep mode entry threshold	$V_{(UVLO)}$ ≤ $V_{I(BAT)}$ ≤ $V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay			V_{VCC} ≤ $V_{I(BAT)}$ +125 mV	V
$V_{(SLPEXIT)}$	Sleep mode exit threshold	$V_{(UVLO)}$ ≤ $V_{I(BAT)}$ ≤ $V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay	V_{VCC} ≥ $V_{I(BAT)}$ +190 mV			
$t_{(DEGL)}$	Deglitch time for sleep mode(13)	$R_{(TMR)}$ = 50 kΩ, $V_{(AC)}$ or $V_{(USB)}$ or decreasing below threshold, 100-ns fall time, 10-mv over-drive		22.5		ms
START-UP CONTROL and USB BOOT-UP						
$t_{(BOOT-UP)}$	Boot-up time	Upon the first application of USB input power or AC input with PSEL low	120	150	180	ms
SWIITCHING POWER SOURCE TIMING						
	Switching power source from inputs (AC or USB) to battery	After $\overline{ACPG}$ or $\overline{USBPG}$ detection, low to high (no ($t_{(BOOT-UP)}$) delay) or after CE hold off time			50	µs
	Switching from AC to USB, or, USB to AC by input source removal. (14)	After $\overline{ACPG}$ or $\overline{USBPG}$ detection, low to high (no ($t_{(BOOT-UP)}$) delay)			100	
	Switching from AC to USB, or USB to AC by toggling PSEL	Toggling PSEL High to Low or Low to High			50	
THERMAL SHUTDOWN REGULATION(15)						
$T_{(SHTDWN)}$	Temperature trip	T_J (Q1 and Q3 only)		155		°C
	Thermal hysteresis	T_J (Q1 and Q3 only)		30		
$T_{J(REG)}$	Temperature regulation limit	T_J (Q2)	115		135	
UVLO						
$V_{(UVLO)}$	Undervoltage lockout	Decreasing V_{CC}	2.45	2.50	2.65	V
	Hysteresis			27		mV

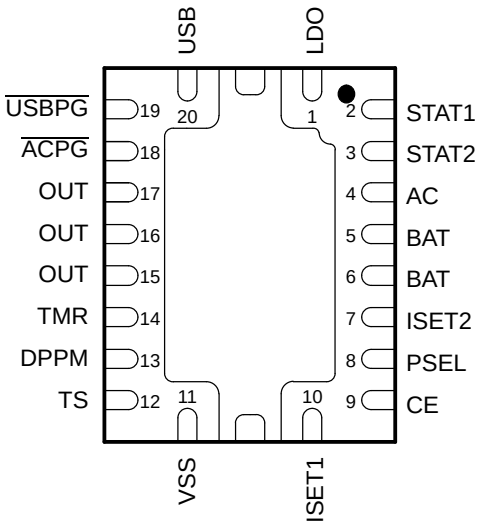
(13) Doesn'tdeclare sleep mode until after the deglitch time and implement the needed powertransfer immediately according to the switching specification.

(14) The power handoff isimplemented once the $\overline{PG}$ pin goes goeshigh (removed source's PG) which is when the removed source drops to thebattery voltage. if the battery voltage is critically low the system may loosepower unless the system takes control of the PSEL pin and switches to theavailable power source prior to shutdown. the USB source often has less currentavailable so the system may have to reduce its load when switching from AC toUSB.

(15) Reaching thermalregulation reduces the charging current. Battery supplement current is notrestricted by either thermal regulation or shutdown. Input power FETs turn offduring thermal shutdown. The battery FET is only protected by a short circuitlimit which typically doesn't cause a thermal shutdown (input FETs turning off)by itself.

DEVICE INFORMATION

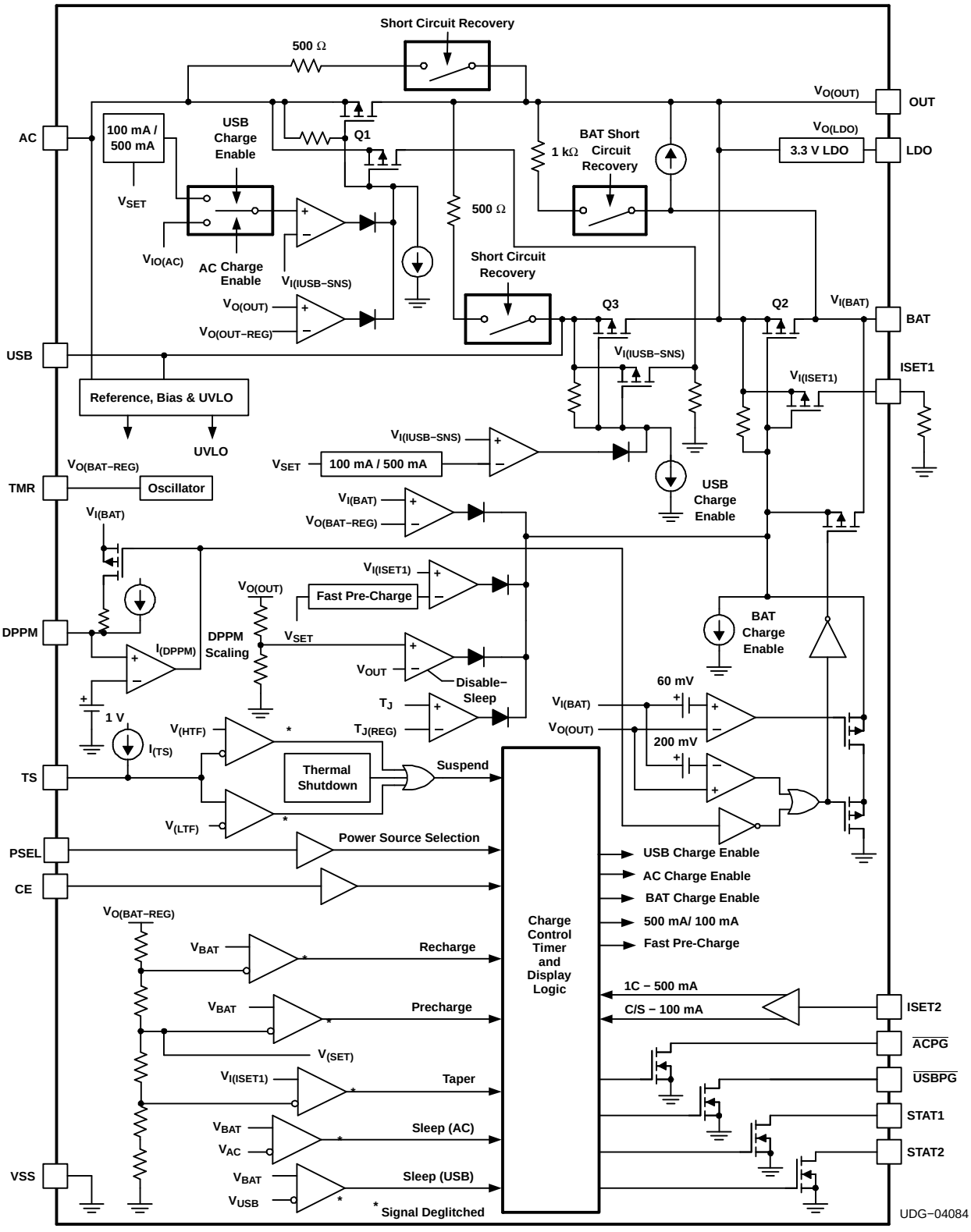
bq24030RHL bq 24032RHL, bq24035RHL
RHL PACKAGE
(BOTTOM VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AC	4	I	Charge input voltage from AC adapter
$\overline{\text{ACPG}}$	18	O	AC powergood status output (open-drain)
BAT	5	I/O	Battery input and output.
BAT	6	I/O	
CE	9	I	Chip enable input (active high)
DPPM	13	I	Dynamic power path management set point (account for scale factor)
ISET1	10	I/O	Charge current set point for AC input and precharge and taper set point for both AC and USB
ISET2	7	I	Charge current set point for USB port. (High = 500 mA, Low = 100 mA) For bq24032 see half charge current mode using ISET2.
LDO	1	O	3.3 V LDO regulator
OUT	15	O	Output terminal to the system
OUT	16		
OUT	17		
PSEL	8	I	Power source selection input (low for USB, High for AC)
STAT1	2	O	Charge status output 1 (open-drain)
STAT2	3	O	Charge status output 2 (open-drain)
TMR	14	I/O	Timer program input
TS	12	I/O	Temperature sense input
USB	20	I	USB charge input voltage
$\overline{\text{USBPG}}$	19	O	USB powergood status output (open-drain)
VSS	11	-	Ground input (the thermal pad on the underside of the package) There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

CHARGE CONTROL

The bqTINY-III supports a precision Li-Ion or Li-Pol charging system suitable for single-cell portable devices. See a typical charge profile, application circuit and an operational flow chart in Figure 1 through Figure 4 respectively.

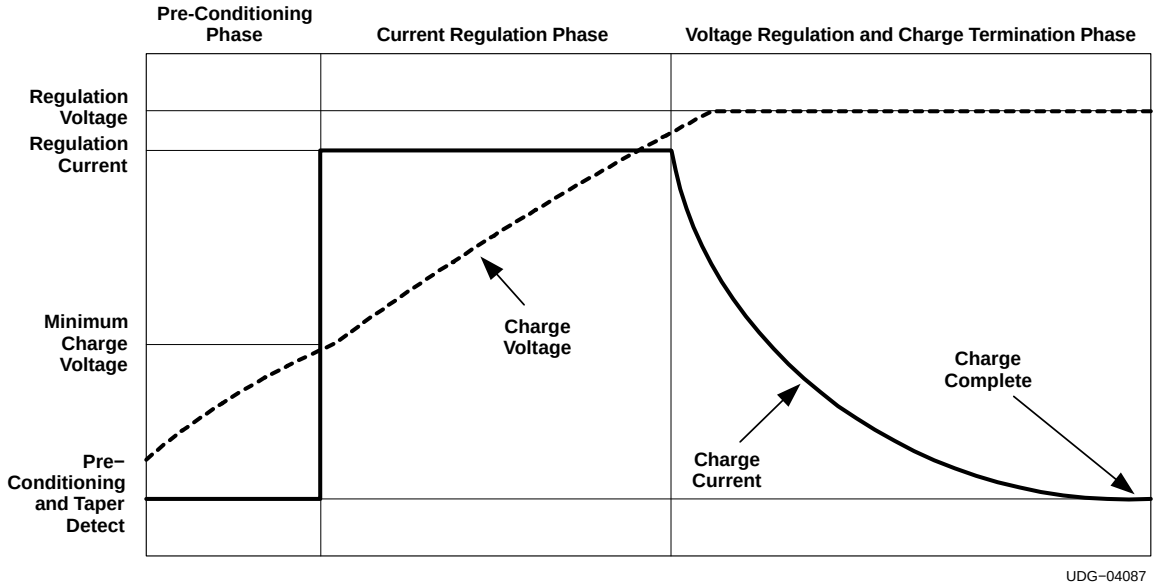


Figure 1. Charge Profile

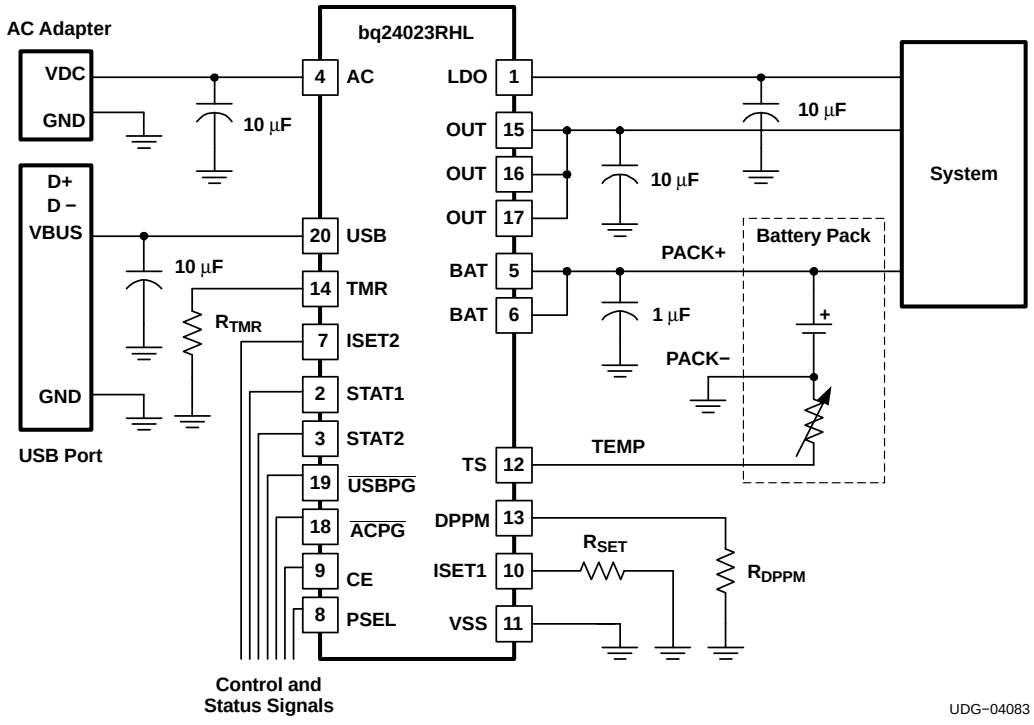


Figure 2. Typical Application Circuit

FUNCTIONAL DESCRIPTIONS (continued)

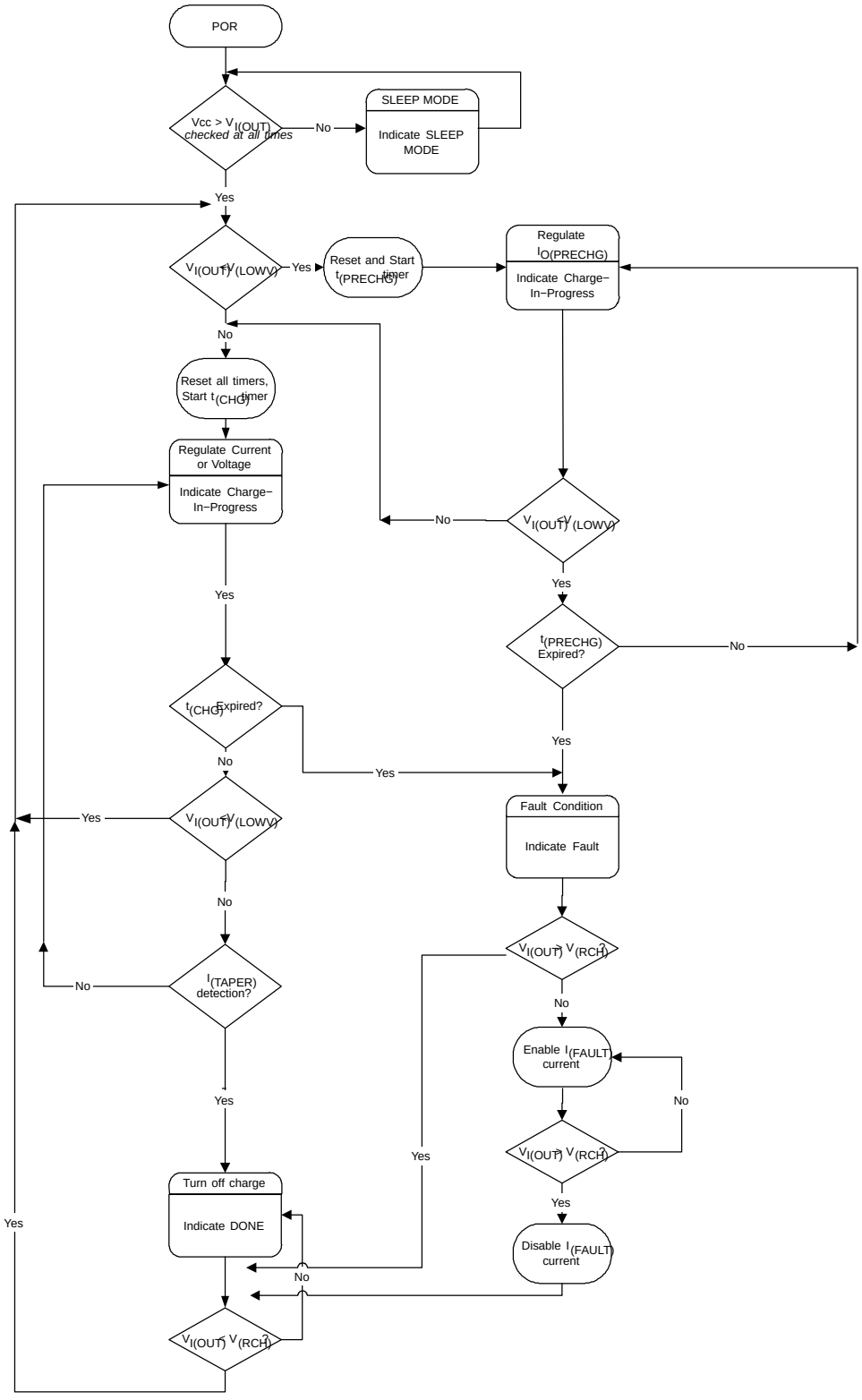


Figure 3. Charge Control Operational Flow Chart

FUNCTIONAL DESCRIPTIONS (continued)

Autononous Power Source Selection

Note that the PSEL pin selects the priority of the input sources (High = AC, Low = USB), if that primary source is not available (based on $\overline{ACPG}$, $\overline{USBPG}$ signal), then it uses the secondary source. If neither input source is available, then the battery is selected as the source. With the PSEL input high, the bqTINY-III attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC adapter has the priority. With the PSEL input low, the bqTINY-III defaults to USB charging. If USB input is grounded, then the bqTINY-III charges from the AC input at the USB charge rate (as selected by ISET2). This feature can be used in system where AC and USB power source selection is done elsewhere. The PSEL function is summarized in Table 1.

Table 1. Power Source Selection Function Summary

PSEL STATE	AC	USB	CHARGE SOURCE	CHARGE RATE	SYSTEM POWER SOURCE	USB BOOT-UP FEATURE
Low	Present(1)	Absent	AC	ISET2	AC	Enabled
	Absent(2)	Present	USB	ISET2	USB	Enabled
	Present	Present	USB	ISET2	USB	Enabled
	Absent	Absent	N/A	N/A	Battery	Disabled
High	Present	Absent	AC	ISET1	AC	Disabled
	Absent	Present	USB	ISET2	USB	Disabled
	Present	Present	AC	ISET1	AC	Disabled
	Absent	Absent	N/A	N/A	Battery	Disabled

(1) *Present* is defined as input being at ahigher voltage than the BAT voltage.
(2) *AC Absent* is defined as AC input notpresent (sleep mode) or Q1 turned off due to overvoltage inbq24035.

Boot-Up Sequence

In order to facilitate the system startup and USB enumeration, the bqTINY-III offers a proprietarty boot-up sequence. Upon the first application of power to the bqTINY-III, this feature enables the 100 mA USB charge rate for a period of approximately 150 ms, ($t_{(BOOT-UP)}$), ignoring the ISET2 and CE inputs setting. At the end of this period, the bqTINY-III implements CE and ISET2 inputs settings. Table 1 indicates when this feature is enabled.

Power Path Management

The bqTINY-III powers the system while independently charging the battery. This features reduces the charge and discharge cycles on the battery, allows for proper charge termination and allows the system to run with an absent or defective battery pack. This feature gives the system priopirty on input power allowing the system to power up with a deeply discharged battery pack. This feature works as follows (note that PSEL is assumed HIGH for this discussion).

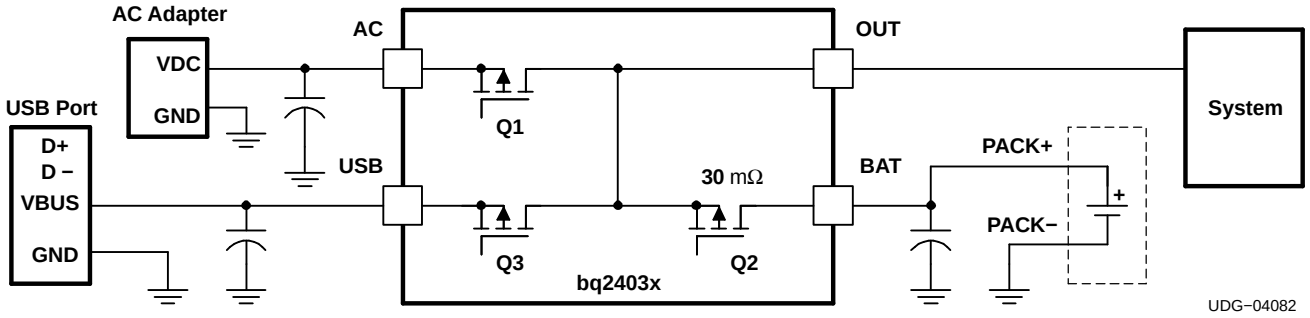


Figure 4. Power Path Management

Case 1: AC (PSEL = High)

System Power

In this case, the system load is powered directly from the AC adapter through the internal transistor Q1 (see Figure 4). For bq24030, Q1 acts as a switch as long as the AC input remains at or below 6 V ($V_{O(OUT-REG)}$). Once the AC voltage goes above 6 V, Q1 starts regulating the output voltage at 6 V. For bq24035, once the AC voltage goes above 6 V, Q1 turns off. For bq24032, the output is regulated at 4.4 V from the AC input. Note that switch Q3 is turned off for both devices. If the system load exceeds the capacity of the supply, the output voltage drops down to the battery's voltage.

Charge Control

When AC is present the battery is charged through switch Q2 based on the charge rate set on the ISET1 input.

Dynamic Power Path Management (DPPM)

This feature monitors the output voltage (system voltage) for input power loss due to brown outs, current limiting or removal of the input supply. If the voltage on the OUT pin drops to a preset value, $V_{DPPM} \times$ SF, due to a limited amount of input current, then the battery charging current is reduced until the output voltage stops dropping. The DPPM control tries and reach a steady state condition where the system gets its needed current and the battery is charged with the remaining current. There is no active control to limit the current to the system. Therefore if the system demands more current than the input can provide, the output voltage drops to the battery voltage and the battery tries and supplement the input current to the system. There are three main advantages of DPPM.

1. This feature allows the designer to select a lower power wall adapter, if the average system load is moderate compared to its peak power. For example if the peak system load is 1.75 A, average system load is 0.5 A and battery fast charge current is 1.25 A, the total peak demand could be 3.0 A. With DPPM a 2-A adaptor could be selected instead of a 3.25-A supply. During the system peak load of 1.75 A and charge load of 1.25 A, the smaller adaptor's voltage drops until the output voltage reaches the DPPM regulation voltage threshold. The charge current is reduced until there is no further drop on the output voltage. The system gets its 1.75-A charge and the battery charge current is reduced from 1.25 A to 0.25 A. When the peak system load drops to 0.5 A, the charge current returns to 1 A and the output voltage returns to its normal value.
2. There is a power savings using DPPM compared to configurations without DPPM. Without DPPM, if the system current plus charge current exceed the supply's current limit, then the output is pulled down to the battery. Linear chargers, dissipate the unused power $(V_{IN}\text{-}V_{OUT}) \times I_{LOAD}$. The current remains high (at current limit) and the voltage drop is large for maximum power dissipation. With DPPM, the voltage drop is less $(V_{IN}\text{-}V_{DPPM-REG})$ to the system which means better efficiency. The efficiency for charging the battery is the same for both cases. The advantages are less power dissipation, lower system temperature and better overall efficiency.
3. The DPPM's function is to sustain the system voltage no matter what causes it to drop, if at all possible. It does this by reducing the non-critical charging load while maintaining the maximum power output of the adaptor.

   Note that the DPPM voltage, $V_{(DPPM)}$, is programmed as follows:

$$V_{(DPPM)} + I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (1)$$

where

- R_{DPPM} is the external resistor connected between the DPPM and VSS pins
- $I_{(DPPM)}$ is the internal current source
- SF is the scale factor as specified in the specification table

The safety timer is dynamically adjusted while in DPPM mode. The voltage on the ISET1 pin is directly proportional to the programmed charging current. When the programmed charging current is reduced, due to DPPM, the ISET1 voltage is reduced and the timer's clock is proportionally slowed, extending the safety time.

Case 2: USB (PSEL = Low)

System Power

In this case, the system load is powered directly from the USB port through the internal switch Q3 (see Figure 5). Note in this case Q3 regulates the total current to the 100 mA or 500 mA level, as selected on the ISET2 input. Switch Q1 is turned off in this mode. If the system and battery load is less than the selected regulated limit, then Q3 is fully on and V_{OUT} is approximately (V_{USB}-VU_{SB-DO}). The system's power management is responsible for keeping its system load below the USB current level selected (if the battery is critically low or missing), otherwise the output drops to the battery voltage. Therefore, the system should have a low power mode for USB power application. The DPPM feature keeps the output from dropping below its programmed threshold, due to the battery charging current, by reducing the charging current.

Charge Control

When USB is present and selected, Q3 regulates the input current to the value selected by the ISET2 pin (0.1/0.5A). The charge current to the battery is set by the ISET1 resistor (typically > 0.5A). Since the charge current typically is programmed for more current than Q3 allows, the output voltage drops to the battery voltage or DPPM voltage, which ever is higher. If the DPPM threshold is reached first, the charge current is reduced as described below.

Dynamic Power Path Management (DPPM)

The theory of operation is the same as described above, in CASE 1, except that Q3 restricts the amount of input current delivered to the output and battery instead of the input supply.

Note that the DPPM voltage, V(DPPM), is programmed as follows:

$$V_{(DPPM)} + I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (2)$$

where

- R_{DPPM} is the external resistor connected between the DPPM and VSS pins
- $I_{(DPPM)}$ is the internal current source
- SF is the scale factor as specified in the specification table

Battery Temperature Monitoring

The bqTINY-III continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for most-common 10 kΩ negative-temperature coefficient thermistors (NTC) (see Figure 5). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected the device immediately suspends the charge. The device suspends charge by turning off the powerFET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns to the normal range. The allowed temperature range for 103AT type thermistor is 0°C to 45°C. However the user may increase the range by adding two external resistors. See Figure 6.

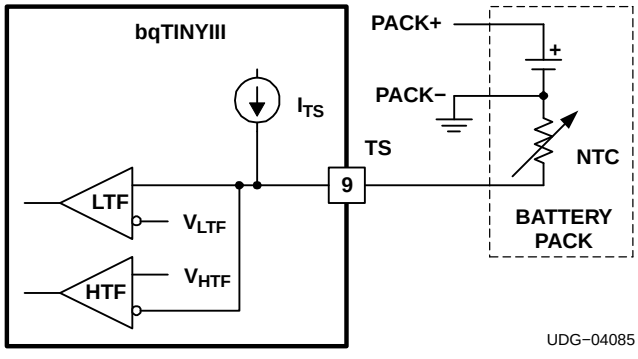


Figure 5. TS Pin Configuration

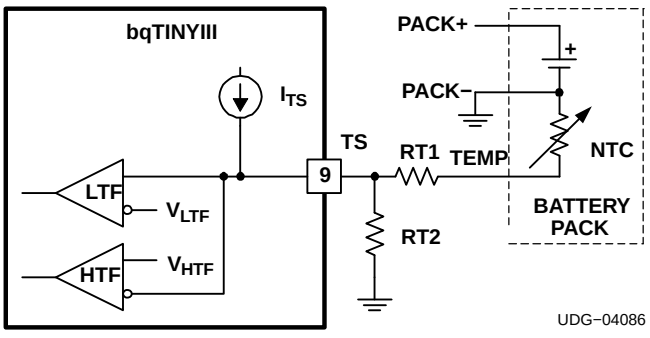


Figure 6. TS Pin Thresholds

Battery Pre-Conditioning

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY-III applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and VSS, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{O\ (PRECHG)} + \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bqTINY-III activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The timeout is extended if the charge current is reduced by DPPM. Please refer to the *Timer Fault Recovery* section for additional details.

Battery Charge Current

The bqTINY-III offers on-chip current regulation with programmable set point. The resistor connected between the ISET1 and VSS, $R_{SET,}$ determines the charge level. The charge level may be reduced to give the system priority on input current (see DPPM). The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} + \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

When powered from a USB port, the input current available (0.1 A/0.5 A) is typically less than the programmed (ISET1) charging current and therefore the DPPM feature attempts to keep the output from being pulled down by reducing the charging current.

For the bq24032 the charge level, during AC operation only (PSEL=High), can be changed by a factor of 2 by setting the ISET2 pin high (full charge) or low (half charge). The voltage on the ISET1 pin, VSET1, is divided by 2 when in the half constant current charge mode. Note that With PSEL low the ISET2 pin controls only the 0.1 A/0.5 A USB current level.

Please also refer to section titled *Power Path Management* for additional details.

Battery Voltage Regulation

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqTINY-III monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY-III also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Refer to the DPPM operation under Case 1, for information on extending the safety timer during DPPM operation. Please refer to the *Timer Fault Recovery* section titled for additional details.

Temperature Regulation and Thermal Protection

In order to maximize charge rate, the bqTINY-III features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the $T_{J(REG)}$ threshold, the bqTINY-III throttles back on the charge current in order to maintain a junction temperature around the $T_{J(REG)}$ threshold. To avoid false termination, the taper detect function is disabled while in this mode.

The bqTINY-III also monitors the junction temperature, T_J, of the die and disconnects the OUT pin from AC or USB inputs if T_J exceeds $T_{(SHTDWN)}$. This operation continues until T_J falls below $T_{(SHTDWN)}$ by the hysteresis level specified in the specification table.

There is no thermal protection for the battery supplement mode. The Q2 FET continues to connect the battery to the output (system), if input power is not sufficient. However, there is a short circuit protection circuit that limits the battery discharge current such that the maximum power dissipation of the part is not exceeded, under typical design conditions

Charge Timer Operation

As a safety backup, the bqTINY-III monitors the charge time in the charge mode. If taper threshold is not detected within the time period, $t_{(CHG)}$, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The resistor connected between the TMR and VSS, R_{TMR}, determines the timer period. The $K_{(TMR)}$ parameter is specified in the specifications table. In order to disable the charge timer, eliminate R_{TMR}, connect the TMR pin directly to the LDO pin. Note that this action eliminates all safety timers also clears any timer fault. TMR pin should not be left floating.

$$t_{(CHG)} + K_{(TMR)} \times R_{(TMR)} \quad (5)$$

While in the thermal regulation mode or DPPM mode, the bqTINY-III dynamically adjusts the timer period in order to provide the additional time needed to fully charge the battery. This proprietary feature is designed to prevent against early or false termination. The maximum charge time in this mode, $t_{(CHG-TREG)}$, is calculated by the equation Equation 6.

$$t_{(CHG+TREG)} \quad \frac{t_{(CHG)} \times V_{(SET)}}{V_{(SET+REG)}} \quad (6)$$

Note that since this adjustment is dynamic and changes as the ambient temperature changes and the charge level changes, the timer clock is adjusted. It is difficult to estimate a total safety time without integrating the above equation over the charge cycle. Therefore, understanding the theory that the safety time is adjusted inversely proportionately with the charge current and the battery is a current-hour rating the safety time dynamically adjusts appropriately.

The $V_{(SET)}$ parameter is specified in the specifications table. $V_{(SET-TREG)}$ is the voltage on the ISET pin during the thermal regulation mode and is a function of charge current. (Note that charge current is dynamically adjusted during the thermal regulation mode).

$$V_{(SET+TREG)} \quad \frac{I_{(OUT)} \times R_{(SET)}}{K_{(SET)}} \quad (7)$$

Charge Taper Detection, Termination and Recharge

The bqTINY-III monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqTINY-III terminates charge. The resistor connected between the ISET1 and VSS, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TAPER)} + \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \quad (8)$$

After charge termination, the bqTINY-III re-starts the charge once the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times. Please see the *Battery Absent Detection* section for additional details.

LDO Register

The bqTINY-III provides a 3.3V LDO regulator. This regulator is typically used to power USB transceiver or drivers in portable applications. Note that this LDO is only enabled when either AC or USB inputs are present.

Sleep and Standby Modes

The bqTINY-III charger circuitry enters the low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery into the bqTINY-III during the absence of input supplies. Note that in SLEEP mode, Q2 remains on (i.e. battery connected to the OUT pin) in order for the battery to continue supplying power to the system.

The bqTINY-III enters the low-power standby mode if while AC or USB is present, the CE input is low. In this suspend mode, internal PowerFETs Q1 and Q3 (refer to block diagram) are turned off, the BAT input is used to power the system through OUT pin and the LDO remains on (powered from output). This feature is designed to limit the power drawn from the input supplies (such as USB suspend mode).

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 2. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off. Note this assumes CE=HIGH..

Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature), timer fault, and sleep mode	OFF	OFF

$\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$Outputs (Power Good)

The two open-drain pins, $\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ (AC and USB Power Good) indicate when the AC adapter or USB port is present and above the battery voltage. The corresponding output turns ON (low) when exiting sleep mode (input voltage above battery voltage). This output is turned off in the sleep mode (open drain). The $\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ pins can be used to drive an LED or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

CE Input (Chip Enable)

The CE (chip enable) digital input is used to disable or enable the IC. A high-level signal on this pin enables the chip and a low-level signal disables the device and initiates the standby mode. The bqTINY-III enters the low-power standby mode when the CE input is low with either AC or USB present. In this suspend mode, internal PowerFETs Q1 and Q3 (refer to block diagram) are turned off, the battery (BAT pin) is used to power the system via Q2 and the OUT pin which also powers the LDO. This feature is designed to limit the power drawn from the input supplies (such as USB suspend mode).

Charge Disable Functions

The DPPM input can be used to disable the charge process. This can be accomplished by floating the DPPM mode. Note that this applies to both AC and USB charging.

TImer Fault Recovery

As shown in Figure 3, bqTINY-III provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: bqTINY-III waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqTINY-III clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

Condition 2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: Under this scenario, the bqTINY-III applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY-III disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqTINY-III clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

APPLICATION INFORMATION

Selecting the Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on each input (AC and USB). A 0.1-µF ceramic, placed in close proximity to AC and USB to VSS pins, works well. In some applications depending on the power supply characteristics and cable length it may be necessary to add an additional 10-µF ceramic to each input.

The bqTINY-III only requires a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the OUT and VSS pin is typically sufficient.

The integrated LDO requires a maximum of 1-µF ceramic capacitor on its output. The output does not require a capacitor for a steady state load but a 0.1-µF minimum capacitance is recommended.

It is recommended to install a minimum of 33-µF between the BAT pin and VSS (in parallel with the battery). This ensures proper hot plug power-up with a no load condition (no system load or battery attached).

Thermal Considerations

The bqTINY-III is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment* (SLUA271). The power pad should be tied to the VSS plane. The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient).

The mathematical expression for θ_{JA} is:

$$\theta_{JA} + \frac{T_J \times T_A}{P} \tag{9}$$

where

- T_J = chip junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from Equation 10:

$$P \quad \left[\left(V_{IN} \quad V_{OUT}\right) \times \left(I_{OUT} + I_{BAT}\right)\right] + \left[\left(V_{OUT} \quad V_{BAT}\right) \times \left(I_{BAT}\right)\right] \tag{10}$$

Due to the charge profile of Li-xx batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Please see Figure 2. Typically the Li-Ion battery's voltage quickly (< 2 V minimum) ramps to approximately 3.5 V, when entering fast charge (1-C charge rate and battery above 3 V). Therefore it is customary to perform the steady state thermal design using 3.5 V as the minimum battery voltage since the system board and charging device doesn't have time to reach a maximum temperature due to the thermal mass of the assembly during the early stages of fast charge. This theory is easily verified by performing a charge cycle on a discharged battery while monitoring the battery voltage and charger's power pad temperature.

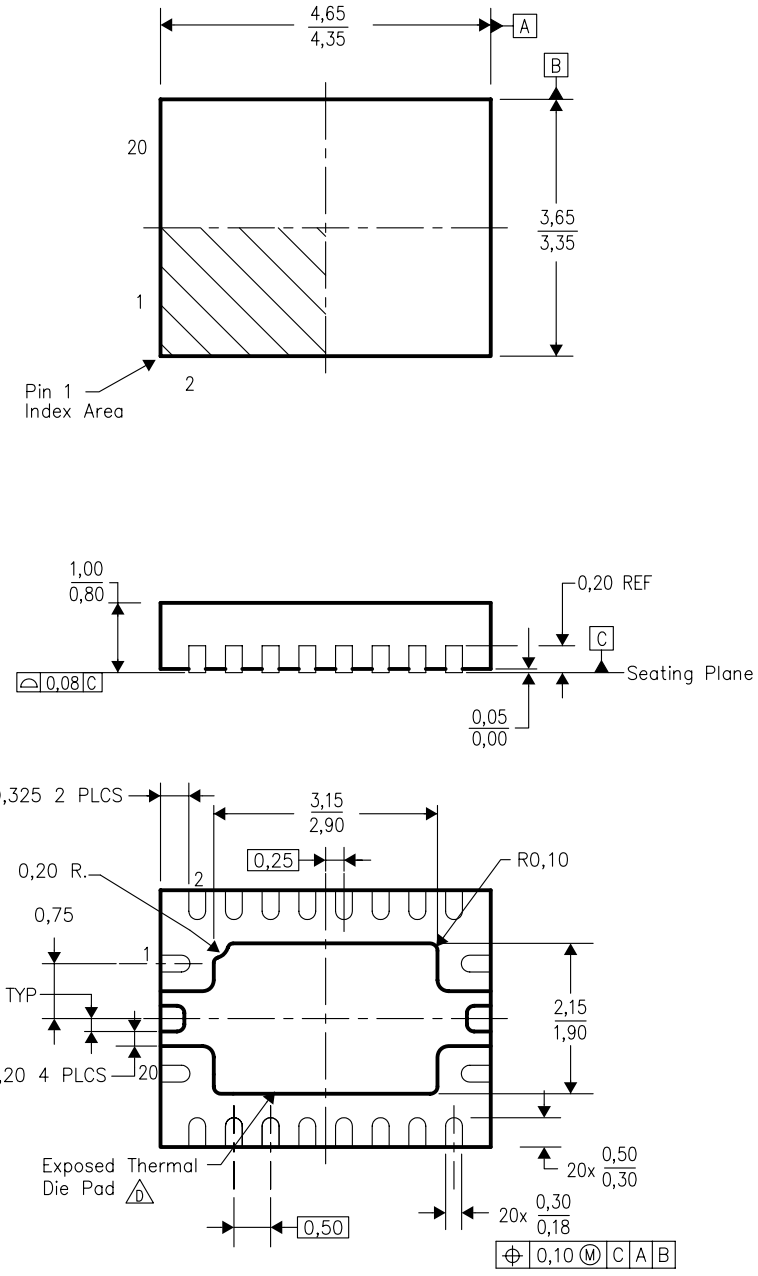
APPLICATION INFORMATION (continued)

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from input terminals to VSS and the output filter capacitors from OUT to VSS should be placed as close as possible to the bqTINY-II, with short trace runs to both signal and VSS pins.
- All low-current VSS connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into AC and USB, and from the BAT and OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY-III is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment* (SLUA271).

RHL (R–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

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