FAIRCHILD SEMICONDUCTOR®

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RMWB04001

RMWB04001

4 GHz Buffer Amplifier MMIC

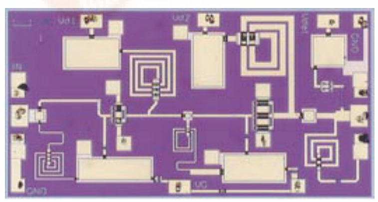
General Description

The RMWB04001 is a 2-stage GaAs MMIC amplifier designed as a 3.5 to 4 GHz Buffer Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other amplifiers, multipliers and mixers it forms part of a complete 23 and 26 GHz transmit/receive chipset. The RMWB04001 utilizes our 0.25µm power PHEMT process and can be used in a variety of applications requiring a high gain medium power amplifier.

Features

- 4 mil substrate
- Small-signal gain 27dB (typ.)
- Saturated Power Out 20dBm (typ.)
- Voltage Detector Included to Monitor Pout
- Chip size 2.4mm x 1.3mm x 100µm

Device



Absolute Ratings

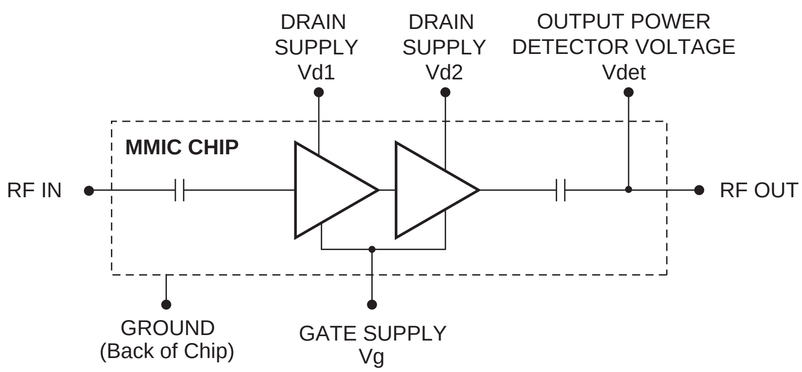
Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+4V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	8	V
I_D	Positive DC Current	168	mA
P_{IN}	RF Input Power (from 50Ω source)	+7	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{STG}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	140	°C/W

Electrical Characteristics (At 25°C), 50Ω system, Vd = +4V, Quiescent Current (Idq) = 36mA

Parameter	Min	Typ	Max	Units
Frequency Range	3.5		4.0	GHz
Gate Supply Voltage[1] (Vg)		-0.7		V
Gain (Small Signal at Pin = -12dBm)	24	27		dB
Gain Variation vs. Frequency		0.5		dB
Power Output Saturated: (Pin = -2dBm)	18	20		dBm
Input Return Loss (Pin = -12dBm)		14		dB
Output Return Loss (Pin = -12dBm)		12		dB
DC Detector Voltage at Pout = 20dBm		0.5		V

Note:
1: Typical range of gate voltage is -1 to -0.4V to set typical Idq of 36mA.

Functional Block Diagram[1]



Note:
1: Detector delivers > 0.1V DC into 3kΩ load resistor for > 20dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

Application Information

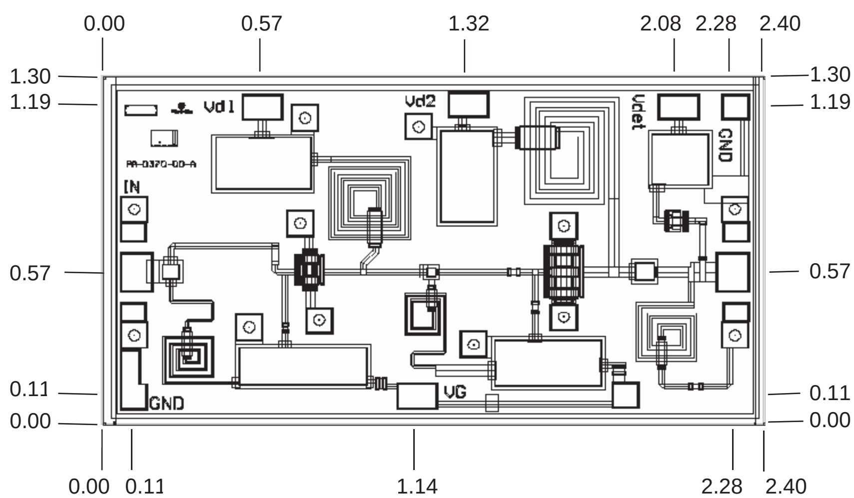
CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

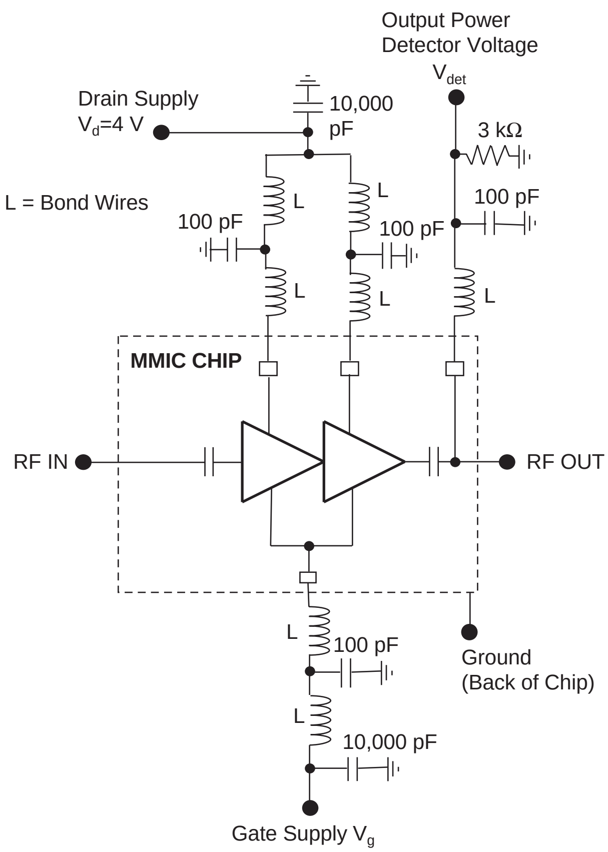
These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3mils wide and 0.5mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mils long corresponding to a typical 2 mil gap between the chip and the substrate material.



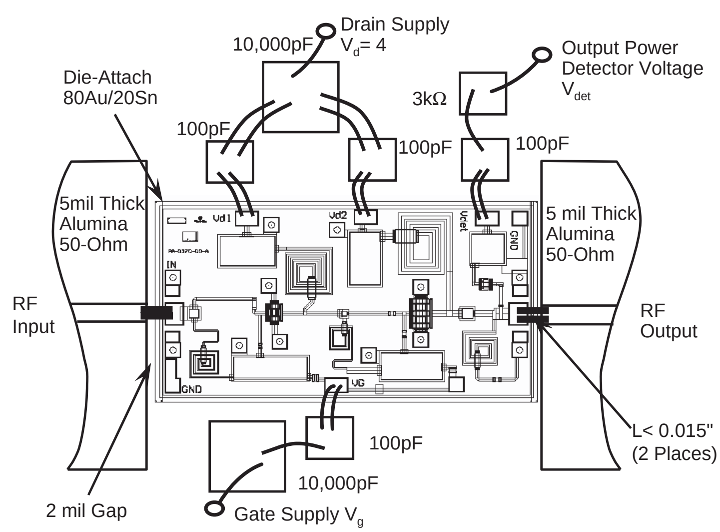
Dimensions in mm

Figure 1. Chip Layout and Bond Pad Locations
Chip Size is 2.40mm x 1.3mm X 100µm. Back of chip is RF and DC Ground.



Note:
Detector delivers > 0.1V DC into 3kΩ load resistor for >20 dBm output power. If output power level detection is not desired, do not connect to detector bond pad.

Figure 2. Recommended Application Schematic Circuit Diagram



Note: Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Figure 3. Recommended Assembly Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +4V to Vd.

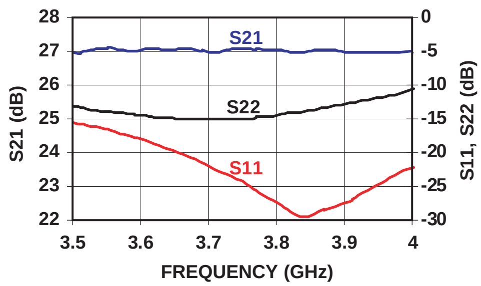
Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 36mA.

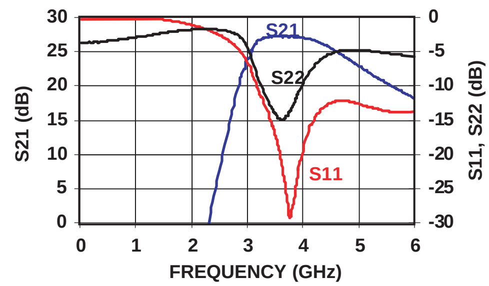
Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:
(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

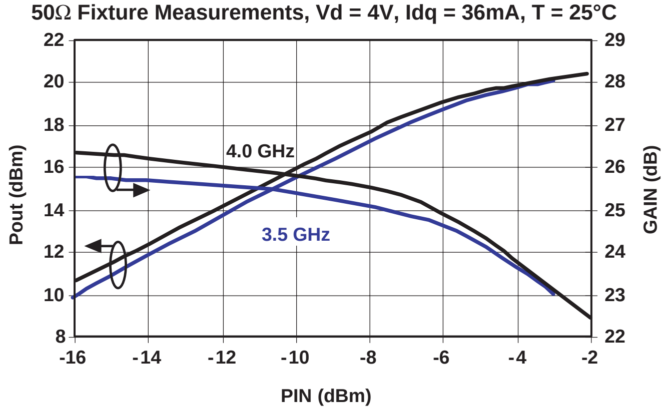
Performance Data

Typical Small Signal Performance
On-Wafer measurements, Vd = 4V, Idq = 36mA, T = 25°C

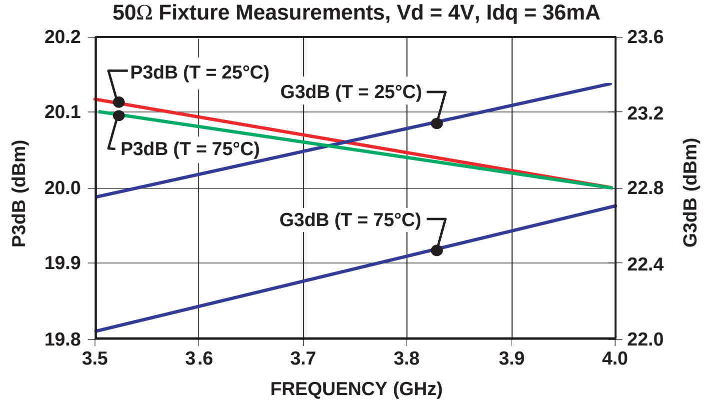




Power Output and Gain vs. Power In
50Ω Fixture Measurements, Vd = 4V, Idq = 36mA, T = 25°C



Power Output and Gain at 3dB vs. Frequency and Temperature
50Ω Fixture Measurements, Vd = 4V, Idq = 36mA



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