

64-bit THERMAL HEAD DRIVER

S-4601A

The S-4601A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. The 75 μm driver output pad pitch allows for high density mounting up to 300dpi. It can be used for general purpose because "H" or "L" can be selected for the latch and the driver enable.

Features

- Low current consumption : 0.3 mA typ.
($f_{\text{CLK}} = 2 \text{ MHz}$, SI : fixed)
- High speed operation : 7 MHz (chip)
5MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 15 mA typ.
($V_{\text{OL}} = 1.5 \text{ V}$, $T_a = -10 \text{ to } 80^\circ\text{C}$)
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

Block Diagram

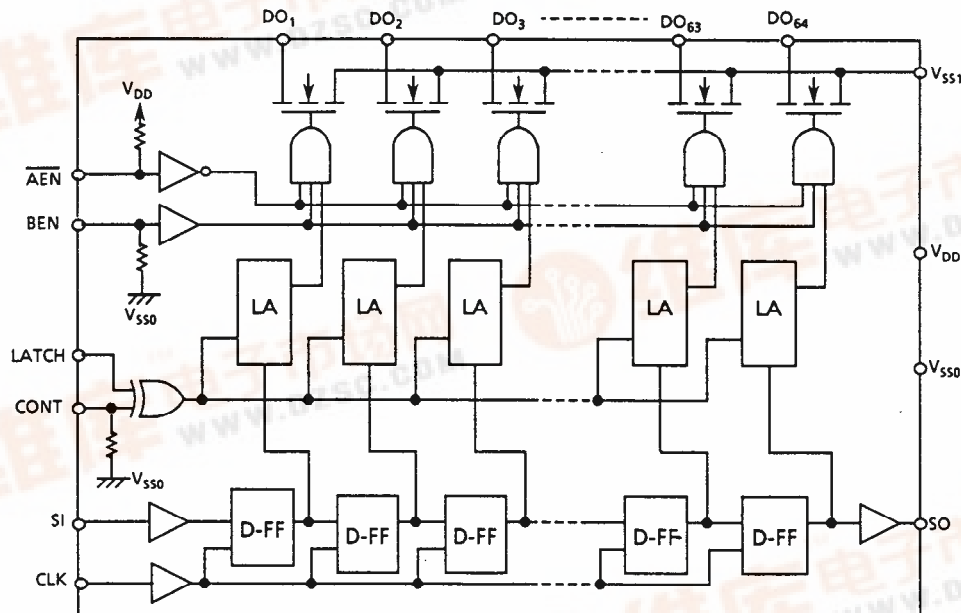


Figure 1

64-bit THERMAL HEAD DRIVER S-4601A

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data are output to the respective drivers when $\overline{\text{AEN}}$ is low and BEN is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{\text{AEN}}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO ₁ to DO ₆₄ (DO _n)	Driver output terminals (Nch open-drain)
65, 66, 73, 74, 80, 81	V _{SS1}	GND for driver (0 V)
71, 78	V _{DD}	Positive power supply for logic (+ 5 V)
67, 75	V _{SS0}	GND for logic (0 V)
77	CLK	Clock input terminal for 64-bit shift register
79	SI	Serial data input terminal for 64-bit shift register
68	SO	Serial data output terminal for 64-bit shift register
69	LATCH	Data latch signal input terminal When CONT = "L" or open LATCH = "L": reads the data of the shift register LATCH = "H": holds the preceding data When CONT = "H" LATCH = "L": holds the preceding data LATCH = "H": reads the data of the shift register
72	CONT	Data latch signal control terminal : selects "H" or "L" for LATCH (pull-down resistor is built in)
76	$\overline{\text{AEN}}$	Driver enable terminal : outputs the latch data to the driver when "L" (pull-up resistor is built in)
70	BEN	Driver enable terminal : outputs the latch data to the driver when "H" (pull-down resistor is built in)

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{SS0,1} - V _{DD}	-0.4 to + 7.0	V
Driver output voltage	V _{DOH}	36	V
Driver output current	I _{DOL}	30	mA
Input voltage	V _{IN}	V _{SS0} -0.5 to V _{DD} + 0.5	V
Output voltage	V _{OUT}	V _{SS0} -0.5 to V _{DD} + 0.5	V
Max. junction temperature	T _{JMAX}	125	°C
Operating temperature	T _{opr}	-10 to + 80	°C
Storage temperature	T _{stg}	-40 to + 125	°C

DC Electrical Characteristics

Table 3
(Unless otherwise specified : $V_{DD} = 5.0 \text{ V} \pm 10\%$, $T_a = -10^\circ\text{C}$ to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		$0.7 \times V_{DD}$	—	V_{DD}	V
Low level input voltage	V_{IL}		V_{SS}	—	$0.3 \times V_{DD}$	V
High level input current	I_{IH}	$V_{DD} = 5.0 \text{ V}$ $V_{IH} = 5.0 \text{ V}$ $T_a = 25^\circ\text{C}$	—	—	35	μA
		BEN, CONT	—	—	0.5	μA
Low level input current	I_{IL}	$V_{DD} = 5.0 \text{ V}$ $V_{IL} = 0 \text{ V}$ $T_a = 25^\circ\text{C}$	—	—	—	μA
		AEN	-35	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load	4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load	—	—	0.05	V
High level output current	I_{OH}	SO terminal, $V_{OH} = V_{DD} - 0.4 \text{ V}$	—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, $V_{OL} = 0.4 \text{ V}$	0.5	—	—	mA
High level driver output voltage	V_{DOH}		—	24	26	V
Low level driver output voltage	V_{DOL}	$I_{DOL} = 15 \text{ mA}$	—	0.7	1.5	V
Driver leakage current	I_{LEAK}	$V_{DOH} = 26 \text{ V}$ Per 1-bit of driver output	—	—	1.0	μA
Current consumption	I_{DD}	$f_{CLK} = 2 \text{ MHz}$, $T_a = 25^\circ\text{C}$ SI : fixed	—	0.3	1.0	mA
Lower V_{DD} detection voltage	V_{DET}		2.0	—	4.0	V

AC Electrical Characteristics

Table 4
($V_{DD} = 5.0 \text{ V} \pm 10\%$, $T_a = -10^\circ\text{C}$ to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS0}$	50	—	—	ns
Data hold time	t_{HD}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS0}$	10	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	$C_L = 3 \text{ pF}$	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	$R_L = 3 \text{ k}\Omega$, $V_{DOH} = 24 \text{ V}$	—	—	2.0	μs
DOn rise time	t_{rDO}	$R_L = 3 \text{ k}\Omega$, $V_{DOH} = 24 \text{ V}$	—	1.0	2.0	μs
DOn fall time	t_{fDO}	$R_L = 3 \text{ k}\Omega$, $V_{DOH} = 24 \text{ V}$	—	0.4	1.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

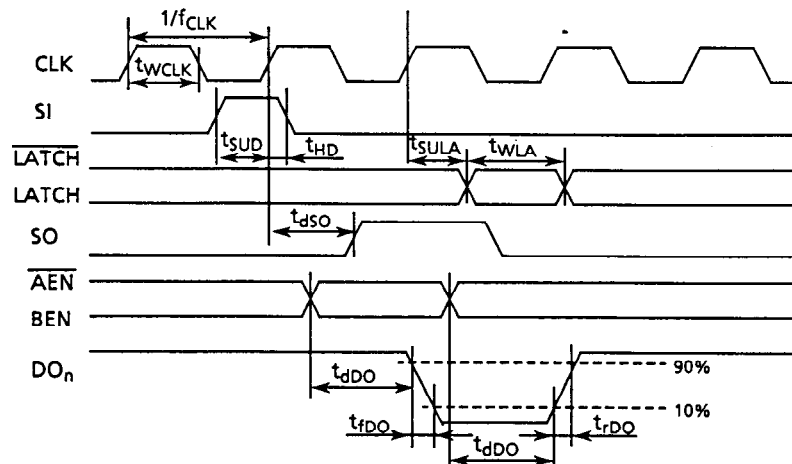


Figure 2

64-bit THERMAL HEAD DRIVER S-4601A

■ Dimensions

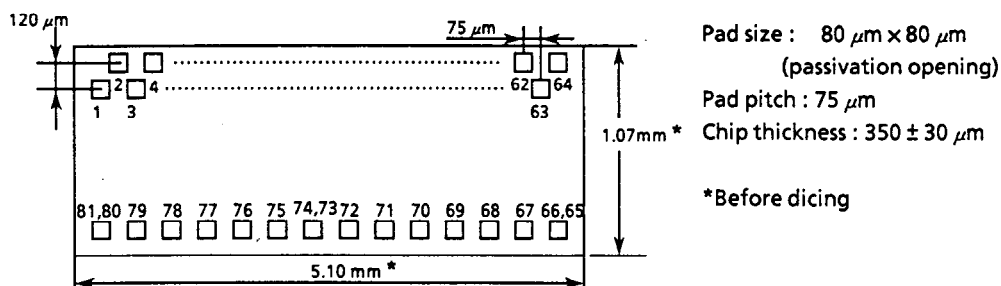


Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit : μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO ₁	-2362.5	310	28	DO ₂₈	-337.5	430	55	DO ₅₅	1687.5	310
2	DO ₂	-2287.5	430	29	DO ₂₉	-262.5	310	56	DO ₅₆	1762.5	430
3	DO ₃	-2212.5	310	30	DO ₃₀	-187.5	430	57	DO ₅₇	1837.5	310
4	DO ₄	-2137.5	430	31	DO ₃₁	-112.5	310	58	DO ₅₈	1912.5	430
5	DO ₅	-2062.5	310	32	DO ₃₂	-37.5	430	59	DO ₅₉	1987.5	310
6	DO ₆	-1987.5	430	33	DO ₃₃	37.5	310	60	DO ₆₀	2062.5	430
7	DO ₇	-1912.5	310	34	DO ₃₄	112.5	430	61	DO ₆₁	2137.5	310
8	DO ₈	-1837.5	430	35	DO ₃₅	187.5	310	62	DO ₆₂	2212.5	430
9	DO ₉	-1762.5	310	36	DO ₃₆	262.5	430	63	DO ₆₃	2287.5	310
10	DO ₁₀	-1687.5	430	37	DO ₃₇	337.5	310	64	DO ₆₄	2362.5	430
11	DO ₁₁	-1612.5	310	38	DO ₃₈	412.5	430	65	V _{SS1}	2395.0	-430
12	DO ₁₂	-1537.5	430	39	DO ₃₉	487.5	310	66	V _{SS1}	2275.0	-430
13	DO ₁₃	-1462.5	310	40	DO ₄₀	562.5	430	67	V _{SS0}	2112.5	-430
14	DO ₁₄	-1387.5	430	41	DO ₄₁	637.5	310	68	SO	1788.5	-430
15	DO ₁₅	-1312.5	310	42	DO ₄₂	712.5	430	69	LATCH	1268.5	-430
16	DO ₁₆	-1237.5	430	43	DO ₄₃	787.5	310	70	BEN	1012.5	-430
17	DO ₁₇	-1162.5	310	44	DO ₄₄	862.5	430	71	V _{DD}	640.5	-430
18	DO ₁₈	-1087.5	430	45	DO ₄₅	937.5	310	72	CONT	292.5	-430
19	DO ₁₉	-1012.5	310	46	DO ₄₆	1012.5	430	73	V _{SS1}	16.5	-430
20	DO ₂₀	-937.5	430	47	DO ₄₇	1087.5	310	74	V _{SS1}	-103.5	-430
21	DO ₂₁	-862.5	310	48	DO ₄₈	1162.5	430	75	V _{SS0}	-273.5	-430
22	DO ₂₂	-787.5	430	49	DO ₄₉	1237.5	310	76	AEN	-545.5	-430
23	DO ₂₃	-712.5	310	50	DO ₅₀	1312.5	430	77	CLK	-981.5	-430
24	DO ₂₄	-637.5	430	51	DO ₅₁	1387.5	310	78	V _{DD}	-1819.5	-430
25	DO ₂₅	-562.5	310	52	DO ₅₂	1462.5	430	79	SI	-2041.5	-430
26	DO ₂₆	-487.5	430	53	DO ₅₃	1537.5	310	80	V _{SS1}	-2275.0	-430
27	DO ₂₇	-412.5	310	54	DO ₅₄	1612.5	430	81	V _{SS1}	-2395.0	-430