

64-bit THERMAL HEAD DRIVER

S-4610A

The S-4610A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It easily drives small heads separately because its driver enable is 32-bit×2. It is ideal for the video printer and the low-voltage-drive thermal print head because of large driver output current and small ON-state resistance.

■ Features

- Low current consumption : 0.4 mA typ.
($f_{CLK} = 5 \text{ MHz}$, SI : fixed)
- High speed operation : 7 MHz (chip)
5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 70 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

■ Block Diagram

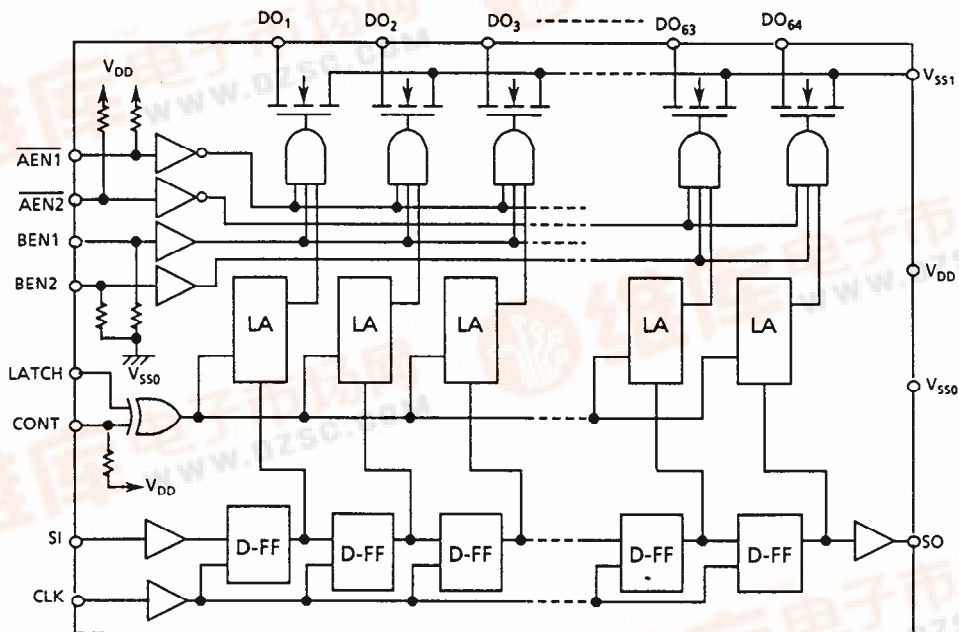


Figure 1

64-bit THERMAL HEAD DRIVER S-4610A

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data are output to the respective drivers when $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ are low and BEN1 and BEN2 are high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ high or BEN1 and BEN2 low makes all driver output transistors go off. $\overline{\text{AEN1}}$ and BEN1 control 1-bit to 32-bit of driver output and $\overline{\text{AEN2}}$ and BEN2 control 33-bit to 64-bit.

-- All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO ₁ to DO ₆₄ (DO _n)	Driver output terminals(Nch open-drain)
65, 68, 71, 74, 77, 80, 83, 86	V _{SS1}	GND for driver (0 V)
67	V _{DD}	Positive power supply for logic (+ 5 V)
75, 81	V _{SS0}	GND for logic (0 V)
82	CLK	Clock input terminal for 64-bit shift register
85	SI	Serial data input terminal for 64-bit shift register
66	SO	Serial data output terminal for 64-bit shift register
84	LATCH	Data latch signal input terminal When CONT = "L" LATCH = "L": reads the data of the shift register LATCH = "H": holds the preceding data When CONT = "H" or open LATCH = "L": holds the preceding data LATCH = "H": reads the data of the shift register
76	CONT	Data latch signal control terminal : selects "H" or "L" for LATCH(pull-up resistor is built in)
73	$\overline{\text{AEN1}}$	Driver enable terminal : $\overline{\text{AEN1}}$ outputs the latch data of DO ₁ to DO ₃₂ and $\overline{\text{AEN2}}$ DO ₃₃ to DO ₆₄ when low(pull-up resistor is built in)
72	$\overline{\text{AEN2}}$	
70	BEN1	Driver enable terminal : BEN1 outputs the latch data of DO ₁ to DO ₃₂ and BEN2 DO ₃₃ to DO ₆₄ when high(pull-down resistor is built in)
69	BEN2	
78, 79	NC	Dummy terminals

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{SS0,1} - V _{DD}	-0.4 to +7.0	V
Driver output voltage	V _{DOH}	36	V
Driver output current	I _{DOL}	70	mA
Input voltage	V _{IN}	V _{SS0} -0.5 to V _{DD} + 0.5	V
Output voltage	V _{OUT}	V _{SS0} -0.5 to V _{DD} + 0.5	V
Max. junction temperature	T _{JMAX}	125	°C
Operating temperature	T _{opr}	-10 to +80	°C
Storage temperature	T _{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3
(Unless otherwise specified : $V_{DD} = 5.0\text{ V} \pm 10\%$, $T_a = -10^\circ\text{C}$ to 80°C)

Parameter	Sybl	Conditions	Min.	Typ.	Max.	Unit	
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
High level input voltage	V_{IH}		$0.7 \times V_{DD}$	—	V_{DD}	V	
Low level input voltage	V_{IL}		V_{SS}	—	$0.3 \times V_{DD}$	V	
High level input current	I_{IH}	$V_{DD} = 5.0\text{ V}$ $V_{IH} = 5.0\text{ V}$ $T_a = 25^\circ\text{C}$	BEN1, 2	—	—	35	μA
				—	—	0.5	μA
Low level input current	I_{IL}	$V_{DD} = 5.0\text{ V}$ $V_{IL} = 0\text{ V}$ $T_a = 25^\circ\text{C}$	AEN1, 2, CONT	-35	—	—	μA
				-0.5	—	—	μA
High level output voltage	V_{OH}	SO terminal, no load	4.45	—	—	V	
Low level output voltage	V_{OL}	SO terminal, no load	—	—	0.05	V	
High level output current	I_{OH}	SO terminal, $V_{OH} = V_{DD} - 0.4\text{ V}$	—	—	-0.5	mA	
Low level output current	I_{OL}	SO terminal, $V_{OL} = 0.4\text{ V}$	0.5	—	—	mA	
High level driver output voltage	V_{DOH}		—	24	26	V	
Low level driver output voltage	V_{DOL}	$I_{DOL} = 50\text{ mA}$, $V_{DD} = 5.0\text{ V}$	—	0.5	1.1	V	
Driver leakage current	I_{LEAK}	$V_{DOH} = 26\text{ V}$ Per 1-bit of driver output	—	—	1.0	μA	
Current consumption	I_{DD}	$T_a = 25^\circ\text{C}$	$f_{CLK} = 2\text{ MHz}$, SI : fixed	—	0.2	0.6	mA
			$f_{CLK} = 5\text{ MHz}$, SI : fixed	—	0.4	1.2	mA
			$f_{CLK} = 5\text{ MHz}$, SI = $1/2f_{CLK}$	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}		2.0	—	4.0	V	

■ AC Electrical Characteristics

Table 4
($V_{DD} = 5.0\text{ V} \pm 10\%$, $T_a = -10^\circ\text{C}$ to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS0}$	50	—	—	ns
Data hold time	t_{HD}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS0}$	10	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	$C_L = 3\text{ pF}$	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	$R_L = 1\text{ k}\Omega$, $V_{DOH} = 24\text{ V}$	—	—	6.5	μs
DOn rise time	t_{rDO}	$R_L = 1\text{ k}\Omega$, $V_{DOH} = 24\text{ V}$	—	1.7	4.5	μs
DOn fall time	t_{fDO}	$R_L = 1\text{ k}\Omega$, $V_{DOH} = 24\text{ V}$	—	2.0	5.0	μs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

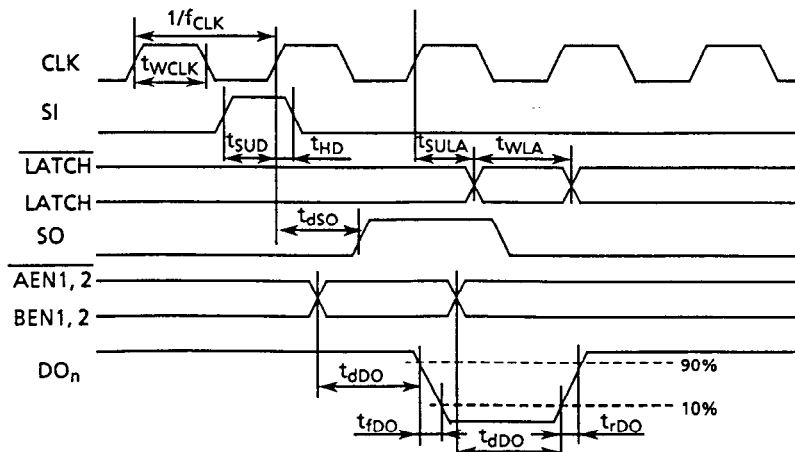
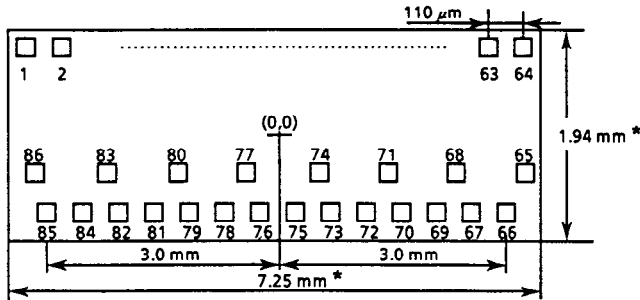


Figure 2

64-bit THERMAL HEAD DRIVER S-4610A

■ Dimensions



Pad size : $80\ \mu\text{m} \times 80\ \mu\text{m}$
(passivation opening)
Pad pitch :
Driver output pad : $110\ \mu\text{m}$
Control pad : $200\ \mu\text{m}$ min.
Chip thickness : $350 \pm 30\ \mu\text{m}$

*Before dicing

Figure 3

■ Pad Coordinates (The origin of the coordinates axes is the center of the chip)

Table 5

Unit : μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO ₁	-3465	865	30	DO ₃₀	-275	865	59	DO ₅₉	2915	865
2	DO ₂	-3355	865	31	DO ₃₁	-165	865	60	DO ₆₀	3025	865
3	DO ₃	-3245	865	32	DO ₃₂	-55	865	61	DO ₆₁	3135	865
4	DO ₄	-3135	865	33	DO ₃₃	55	865	62	DO ₆₂	3245	865
5	DO ₅	-3025	865	34	DO ₃₄	165	865	63	DO ₆₃	3355	865
6	DO ₆	-2915	865	35	DO ₃₅	275	865	64	DO ₆₄	3465	865
7	DO ₇	-2805	865	36	DO ₃₆	385	865	65	V _{SS1}	3070	-455
8	DO ₈	-2695	865	37	DO ₃₇	495	865	66	SO	2870	-865
9	DO ₉	-2585	865	38	DO ₃₈	605	865	67	V _{DD}	2455	-865
10	DO ₁₀	-2475	865	39	DO ₃₉	715	865	68	V _{SS1}	2190	-455
11	DO ₁₁	-2365	865	40	DO ₄₀	825	865	69	BEN2	1985	-865
12	DO ₁₂	-2255	865	41	DO ₄₁	935	865	70	BEN1	1785	-865
13	DO ₁₃	-2145	865	42	DO ₄₂	1045	865	71	V _{SS1}	1310	-455
14	DO ₁₄	-2035	865	43	DO ₄₃	1155	865	72	AEN2	985	-865
15	DO ₁₅	-1925	865	44	DO ₄₄	1265	865	73	AEN1	785	-865
16	DO ₁₆	-1815	865	45	DO ₄₅	1375	865	74	V _{SS1}	430	-455
17	DO ₁₇	-1705	865	46	DO ₄₆	1485	865	75	V _{SS0}	230	-865
18	DO ₁₈	-1595	865	47	DO ₄₇	1595	865	76	CONT	30	-865
19	DO ₁₉	-1485	865	48	DO ₄₈	1705	865	77	V _{SS1}	-450	-455
20	DO ₂₀	-1375	865	49	DO ₄₉	1815	865	78	NC	-870	-865
21	DO ₂₁	-1265	865	50	DO ₅₀	1925	865	79	NC	-1130	-865
22	DO ₂₂	-1155	865	51	DO ₅₁	2035	865	80	V _{SS1}	-1330	-455
23	DO ₂₃	-1045	865	52	DO ₅₂	2145	865	81	V _{SS0}	-1535	-865
24	DO ₂₄	-935	865	53	DO ₅₃	2255	865	82	CLK	-1965	-865
25	DO ₂₅	-825	865	54	DO ₅₄	2365	865	83	V _{SS1}	-2210	-455
26	DO ₂₆	-715	865	55	DO ₅₅	2475	865	84	LATCH	-2420	-865
27	DO ₂₇	-605	865	56	DO ₅₆	2585	865	85	SI	-2890	-865
28	DO ₂₈	-495	865	57	DO ₅₇	2695	865	86	V _{SS1}	-3090	-455
29	DO ₂₉	-385	865	58	DO ₅₈	2805	865				