AUK Semiconductor

S3882P

Current Mode PWM Controller

Descriptions

The S3882 is fixed PWM controller for Off-line and DC-DC converter applications. The internal circuits include UVLO, low start up current circuit, temperature compensated reference, high gain error amplifier, current sensing comparator, and high current totempole output for driving a power MOSFET.
Also S3882 provide low start up current below 0.3mA and short shutdown delay Time typical 100nsec.
S3882 have UVLO threshold of 16V(on) and 10V(off).
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Features

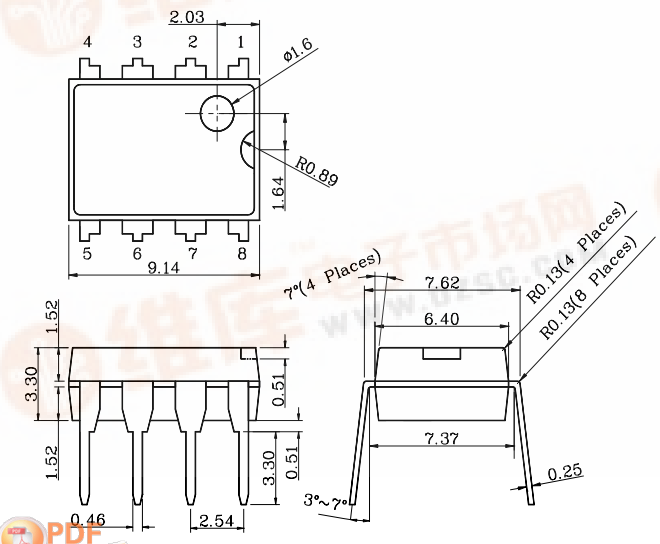
- Low start up current < 0.3mA
- Operating range up to 500KHz
- Cycle by cycle current limiting
- Under Voltage Lock Out with hysteresis
- Short shutdown delay time ; typical 100nsec
- High current totempole output
- Output swing limiting : 22V

Ordering Information

Type NO.	Marking	Package Code
S3882P	S3882P	DIP-8

Outline Dimensions

unit : mm



PIN Connections

1. Output / Compensation
2. Voltage feedback. Input
3. Current sense Input
4. Rt/Ct
5. GND
6. Output
7. Vcc
8. Vref

Absolute Maximum Ratings

Ta=25°C

Characteristic	Symbol	Ratings	Unit
Supply Voltage	Vcc	28	V
Output Current	Io	1	A
Analog Inputs	Vi(ana)	-0.3 to 6.3	V
Error Amp. Output Sink current	Isink(EA)	10	mA
Power Dissipation	Pd	1	W

Electrical Characteristics

(Vcc=15V, Rt=10Kohm,Ct=3.3nF, Ta=0℃ to 70℃, Unless otherwise specified)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
1. Reference Section						
Output Voltage	Vref	Tj=25℃, Io=1mA	4.91	5.00	5.09	V
Line Regulation	Δ Vref	12V ≤ V_{CC} ≤ 25V	-	6	20	mV
Load Regulation	Δ Vref	1mA ≤ I_O ≤ 20mA	-	6	25	mV
Output Short Current	Isc	Ta=25°C	-180	-100	-	mA
2. Oscillator Section						
Initial Accuracy	f_{OSC}	Tj=25℃	47	52	57	KHz
Voltage Stability	△f /△V	12V ≤ V_{CC} ≤ 25V	-	0.2	1.0	%
Oscillator Voltage	V_{OSC}	V_{pin4}, peak to peak	1.4	1.7	1.8	V
Discharge Current	$I_{discharge}$	Tj=25°C, Pin4=2V	7.8	8.3	8.8	mA
3. Error Amp Section						
Input Voltage	V_2	V_{PIN1}=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_b	-	-2.0	-0.3	-	μA
Open Loop Voltage Gain	A_{VO1}	2V ≤ V_O ≤ 4V	65	90	-	dB
Unity Gain Bandwidth	GBW	Tj=25°C	0.7	1	-	MHz
PSRR	PSRR1	V_{CC}=12V to 25V	60	70	-	dB
Output Sink Current	I_{SINK}	V_{PIN2}=2.7V, V_{PIN1}=1.1V	2	6	-	mA
Output Source Current	I_{SOURCE}	V_{PIN2}=2.3V, V_{PIN1}=5V		-0.8	-0.5	mA
Output High Voltage	V_{OH}	V_{pin2}=2.3V, R_1=15 kΩ to GN	5	6	-	V
Output Low Voltage	V_{OL}	V_{PIN2}=2.3V, R_1=15 kΩ to PIN8	-	0.8	1.1	V
4. Current Sense Section						
Gain	G_V	-	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{i(MaX)}$	$V_{PIN\ 1}$=5V	0.9	1.0	1.1	V
PSRR	PSRR2	12V ≤ V_{CC} ≤ 25V	-	70	-	dB
Input Bias Current	$I_{\ bias}$	-	-10	-2	-	μA
Delay to Output	T_d	$V_{PIN\ 3}$=0V to 2V	-	100	200	nS

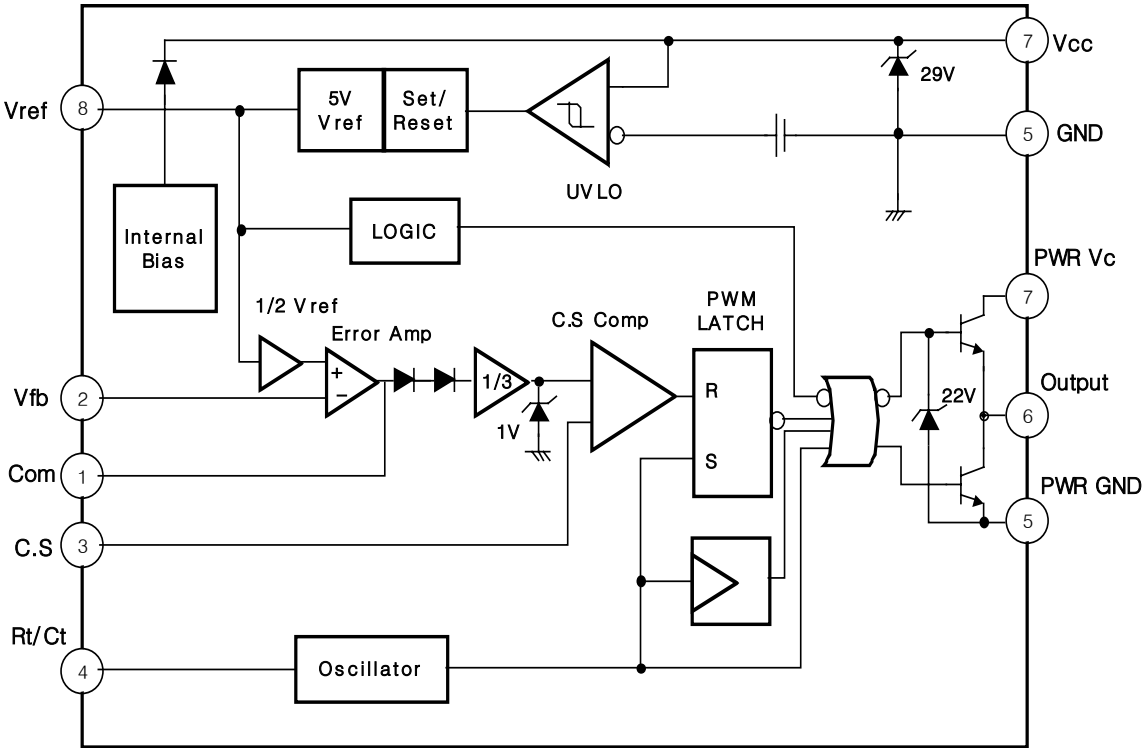
Electrical Characteristics(continued)

(Vcc=15V, Rt=10Kohm, Ct=3.3nF, Ta=0℃to 70℃, Unless otherwise specified)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
5. Output Section						
Output Low Level1	V_{OL1}	Isink=20mA	-	0.1	0.4	V
Output Low Level2	V_{OL2}	Isink=200mA	-	1.5	2.0	V
Output High Level1	V_{OH1}	Isource=20mA	13.0	13.5	-	V
Output High Level2	V_{OH2}	Isource=200mA	12.0	13.5	-	V
Rise Time	t_r	Tj=25℃, C_1=1nF	-	40	100	nS
Fall Time	t_f	Tj=25℃, C_1=1nF	-	40	100	nS
Out Volt. Swing Limit	V_{olim}	Vcc=27V, C_1=1nF	-	22	-	V
6. Under Voltage Lockout Section						
Start Threshold	V_{th}	-	15	16	17	V
Min. Operating Voltage	V_{tL}	After turn on	9	10	11	V
7.PWM Section						
Maximum Duty Cycle	D_{max}	-	94	96	100	%
Minimum Duty Cycle	D_{min}	-	-	-	0	%
8.Total Standby Section						
Start-Up Current	I_{st}	-	-	0.2	0.4	mA
Operating Supply Current	I_{CC}	V_{pin2}=V_{pin3}=0V	-	11	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC}=25mA	-	29	-	V

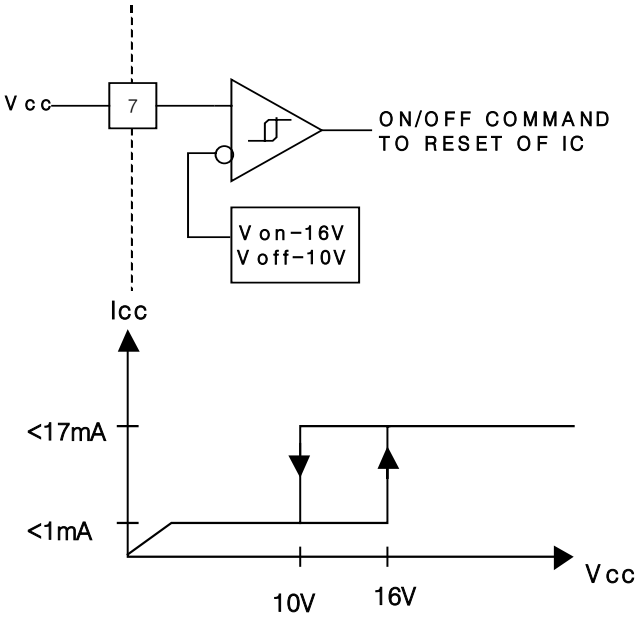
NOTE: Adjust Vcc above the the start threshold before setting at 15V

Block Diagram



Information in Using IC

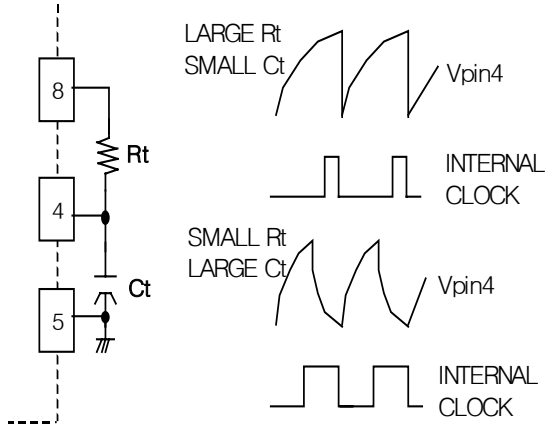
1. Under voltage Lockout



To prevent erratic output behavior which activating the power switch with extraneous leakage currents, during under voltage lockout. Output(pin6) should be shunted to ground with a bleeder resister.

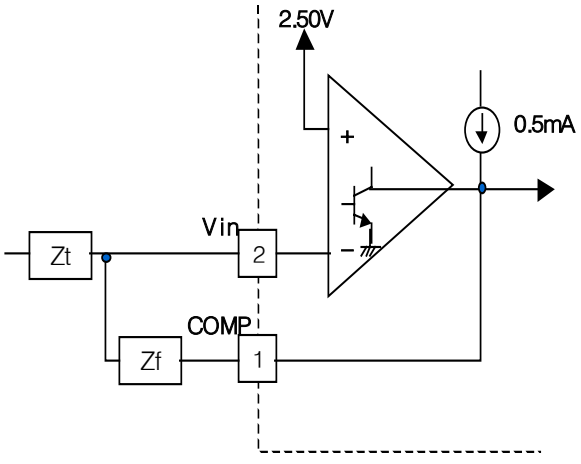
The Vcc comparator upper and lower threshold are 16V/10V. The large hysteresis and low start up currents makes it ideally suited in off-line converter application where efficient bootstrap start-up techniques are required.

2. Oscillator Waveforms and Maximum Duty Cycle



The oscillator frequency is programmed by the values selected for the timing components Rt and Ct. Ct is charged from 5V, Vref, through resistor Rt to approximately 2.8V and discharged to 1.2V by an internal current sink.
During the discharge of Ct, the oscillator generates an internal blanking pulse and the center input NOR gate high. This makes output to be in a low state and control the amount of output dead time.

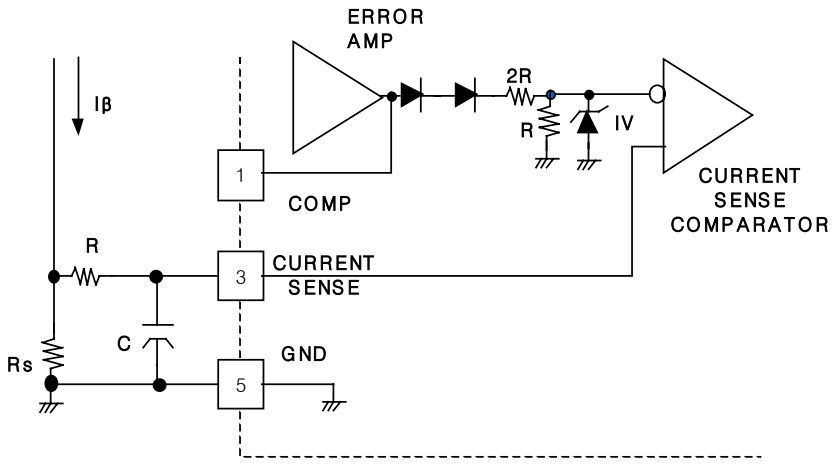
3. Error AMP Configuration



Error amp output(Pin1) is provided for external loop compensation and error amp can source or sink up to 0.5mA. The non-inverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input(pin2).

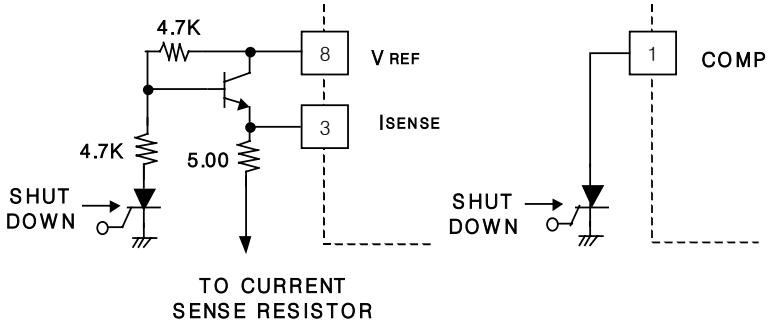
4. Current Sense Circuit

$$Ipeak = \frac{R(V_{pin1} - 2V_{be})}{3R \times Rs}$$



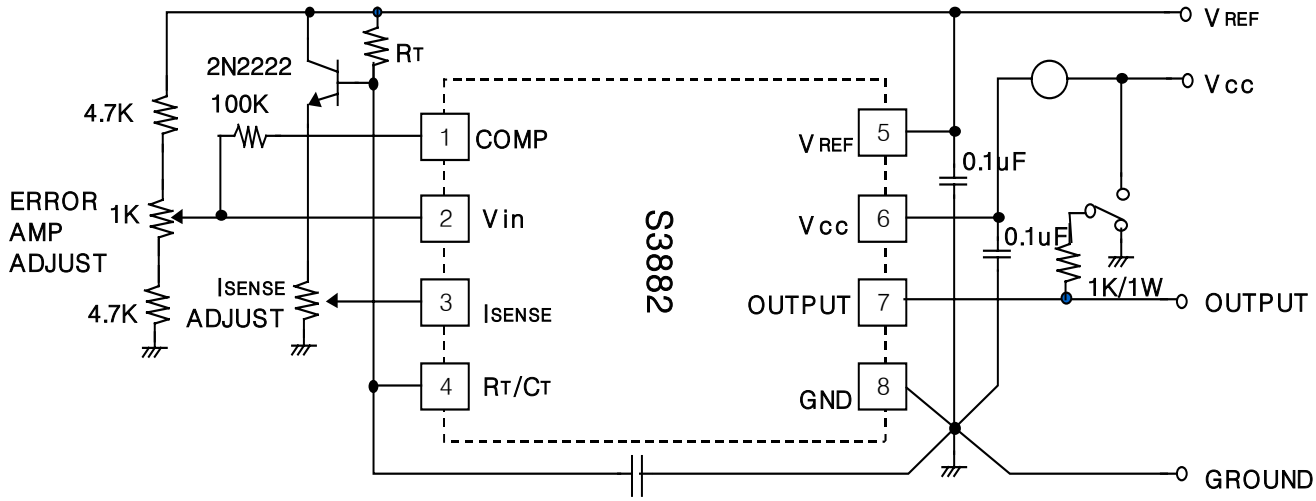
A normal operating conditions occurs when the power supply output is overloaded or if output voltage to 1.0V Therefore the maximum peak switch current is lpk(max)=1.0V/Rs, and under the normal operating conditions the peak inductor current controlled by the voltage at pin1.

5. Shutdown Techniques



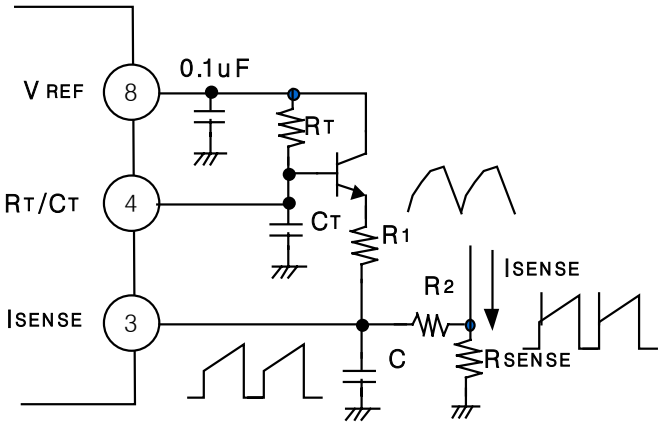
Shutdown of the S3882 can be accomplished by two methods; either raise pin3 above 1V or pull pin1 below a voltage two diodes drops above ground. Either causes the output of the PWM method comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which turn off, allowing the SCR to reset.

6. Open Loop Test



High peak currents associated with capacitive leads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

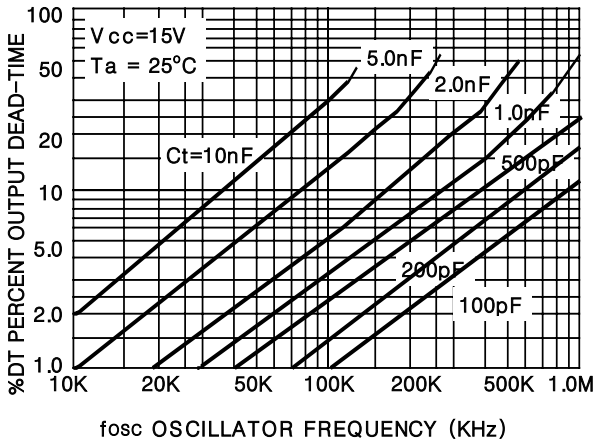
7.Slope Compensation



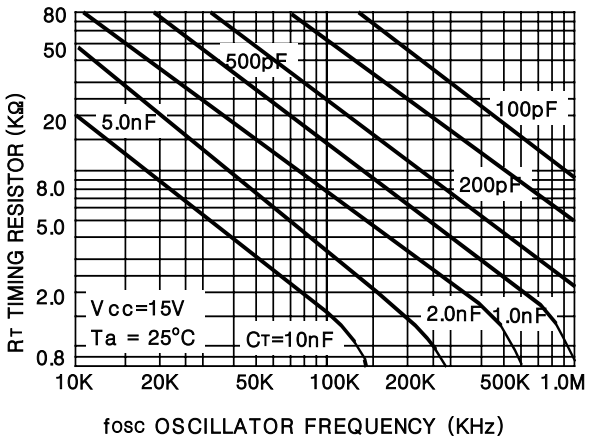
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycle over 50%. Note that capacitor C, forms a filter with R_2 to suppress the leading edge switch spikes.

Electrical Characteristic Curves

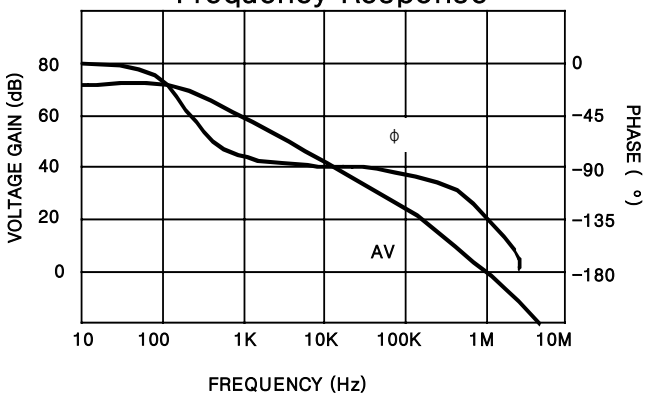
OUTPUT DEAD-TIME vs.
OSCILLATOR FREQUENCY



TIMING RESISTOR vs.
OSCILLATOR FREQUENCY



Error Amplifier Open-Loop
Frequency Response



Output Saturation Characteristics