◇ STRUCTURE Silicon Monolithic Integrated Circuit
◇ PRODUCT SPI BUS Serial EEPROMs
◇ SERIES SIGNATURE SERIES
◇ FAMILY BR95□□0 family
◇ TYPE Supply voltage 1.8V～5.5V/Opreating temperature -40℃～+85℃type
◇ PART NUMBER BR95□□0-R□□6TP

PART NUMBER	PACKAGE	DENSITY
BR95010-RMN6TP	SO8 narrow	1Kbit
BR95020-RMN6TP		2Kbit
BR95040-RMN6TP		4Kbit
BR95080-RMN6TP		8Kbit
BR95160-RMN6TP		16Kbit
BR95010-RDW6TP	TSSOP8	1Kbit
BR95020-RDW6TP		2Kbit
BR95040-RDW6TP		4Kbit
BR95080-RDW6TP		8Kbit
BR95160-RDW6TP		16Kbit
BR95010-RDS6TP	TSSOP8 3×3mm^2	1Kbit
BR95020-RDS6TP		2Kbit
BR95040-RDS6TP		4Kbit

◇ FEATURES

SPI BUS interface
Endurance : 1,000,000 erase/write cycles
Data retention : 40 years
Intial Data: Memory array FFh

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	-65	125	℃
V_I	Input Voltage	-0.3	Vcc+0.3	V
Vcc	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (Ta=25℃)

PACKAGE	Rating	Unit
SO8 narrow	450 *1	mW
TSSOP8	330 *2	mW
TSSOP8 3×3mm^2	310 *3	mW

* Degradation is done at 4.5mW/℃(*1), 3.3mW/℃(*2), 3.1mW/℃(*3) for operation above 25℃

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=−40～85°C, Vcc=1.8～5.5V)

Parameter	Symbol	Min.	Max.	Unit	Test condition
Input Leakage Current	I_{LI}	−	±2	μA	$V_{IN}=V_{SS}$ or V_{CC}
Output Leakage Current	I_{LO}	−	±2	μA	$\overline{S}=V_{CC}$, $V_{OUT}=V_{SS}$ or V_{CC}
Supply Current	I_{CC}	−	1	mA	V_{CC}=1.8V, f_C=2MHz, t_W=10ms
Supply Current (Standby Power mode)	I_{CCI}	−	0.5	μA	$\overline{S}=V_{CC}$, V_{CC}=1.8V, $V_{IN}=V_{SS}$ or V_{CC}
Input Low Voltage (BR95010/020/040)	V_{IL}	−0.3	$0.25V_{CC}$	V	
Input Low Voltage (BR95080/160)		−0.3	0.3Vcc	V	
Input High Voltage	V_{IH}	$0.7V_{CC}$	V_{CC}+0.3	V	
Output Low Voltage	V_{OL}	−	0.3	V	I_{OL}=0.15mA, V_{CC}=1.8V
Output High Voltage	V_{OH}	0.8 V_{CC}	−	V	I_{OH}=−0.1mA, V_{CC}=1.8V

○This product is not designed for protection against radioactive rays.

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=−40～85°C, Vcc=1.8～5.5V, C_L=100pF)

Parameter	Symbol	Min.	Max.	Unit
Clock Frequency	f_c	−	2	MHz
$\overline{S}$ Active Setup Time	t_{SLCH}	200	−	ns
$\overline{S}$ Not Active Setup Time	t_{SHCH}	200	−	ns
$\overline{S}$ Deselect Time	t_{SHSL}	200	−	ns
$\overline{S}$ Active Hold Time	t_{CHSH}	200	−	ns
$\overline{S}$ Not Active Hold Time	t_{CHSL}	200	−	ns
Clock High Time	t_{CH} *1	200	−	ns
Clock Low Time	t_{CL} *1	200	−	ns
Clock Rise Time	t_{CLCH} *2	−	1	μs
Clock Fall Time	t_{CHCL} *2	−	1	μs
Data In Setup Time	t_{DVCH}	40	−	ns
Data In Hold Time	t_{CHDX}	50	−	ns
Clock Low Hold Time after $\overline{HOLD}$ not Active	t_{HHCH}	140	−	ns
Clock Low Hold Time after $\overline{HOLD}$ Active	t_{HLCH}	90	−	ns
Clock High Set-up Time before $\overline{HOLD}$ Active (BR95010/020/040)	t_{CHHL}	120	−	ns
Clock Low Set-up Time before $\overline{HOLD}$ Active (BR95080/160)	t_{CLHL}	0	−	ns
Clock High Set-up Time before $\overline{HOLD}$ not Active (BR95010/020/040)	t_{CHHH}	120	−	ns
Clock Low Set-up Time before $\overline{HOLD}$ not Active (BR95080/160)	t_{CLHH}	0	−	ns
Output Disable Time	t_{SHQZ} *2	−	250	ns
Clock Low to Output Valid (BR95010/020/040)	t_{CLQV}	−	180	ns
Clock Low to Output Valid (BR95080/160)		−	150	
Output Hold Time	t_{CLQX}	0	−	ns
Output Rise Time	t_{QLQH} *2	−	100	ns
Output Fall Time	t_{QHQL} *2	−	100	ns
$\overline{HOLD}$ High to Output Valid	t_{HHQV}	−	150	ns
$\overline{HOLD}$ Low to Output High-Z	t_{HLQZ} *2	−	250	ns
Write Time	t_W	−	10	ms

*1 $t_{CH}+t_{CL}\geqq 1/f_C$

*2 This parameter is not 100% tested.

◇ BLOCK DIAGRAM

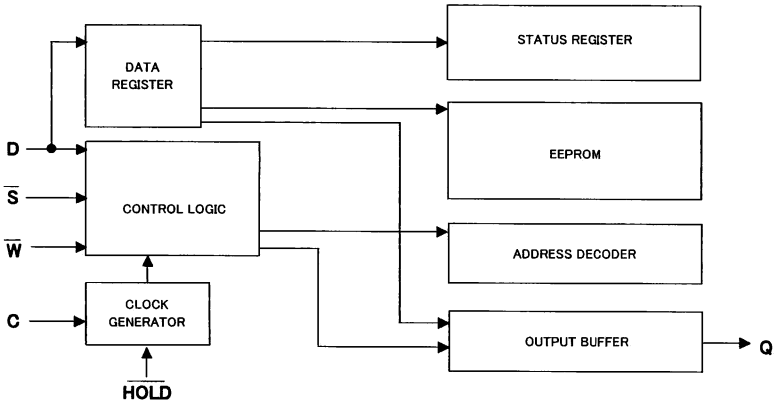


Fig.−1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	$\overline{S}$
2	Q
3	$\overline{W}$
4	Vss
5	D
6	C
7	$\overline{HOLD}$
8	Vcc

◇NOTES FOR POWER SUPPLY

In order to prevent an inadvertent write, the device has the feature of P.O.R.
After the power is on, the device is in the write disable mode. P.O.R. works only during power up. The noise may force the device write enable mode with $\overline{S}$="H"during power ON/OFF. In the case of power up, keep the following conditions to ensure to make the function of P.O.R.

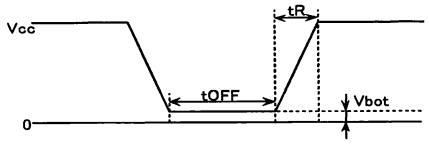


Fig.-2 Vcc waveform

◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

Please keep $\overline{S}$ "H" during power ON/OFF.
The device is an active state during $\overline{S}$ is low. The extraordinary function or data collaption may occur because of noise etc., if power-up is done with $\overline{S}$ "L". In order to prevent above errors from happening, keep $\overline{S}$ "H" (=Vcc) during power ON. (The device does not receive any command during $\overline{S}$ is high.)
It may continue at low Vcc by capacitance of Vcc line during power off.
Please keep $\overline{S}$ "H" during power off because of the device may make malfunction and inadvertent write.

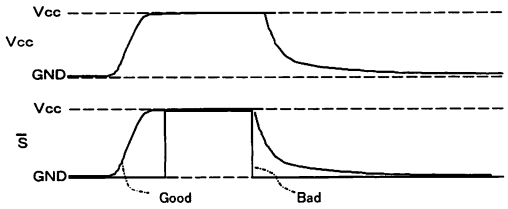


Fig.-3 $\overline{S}$ TIMING DURING POWER ON/OFF

(Good example)
$\overline{S}$ follows Vcc. ($\overline{S}$ is pull up to Vcc)

(Bad example)
$\overline{S}$ is low during power ON/OFF.
Please take more than 10ms between power ON and power OFF, or the internal circuit is not always reset.

◇CAUTIONS ON USE

(1) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

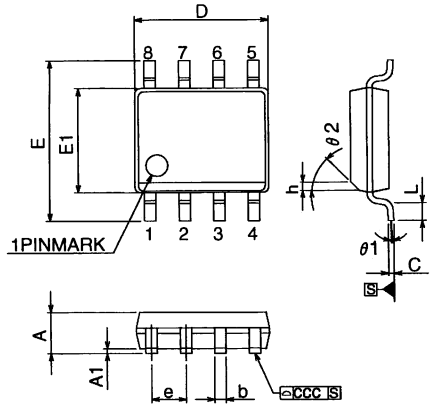
(2) Vss electric potential
Set the voltage of Vss terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of Vss terminal.

(3) Thermal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and Vss owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION

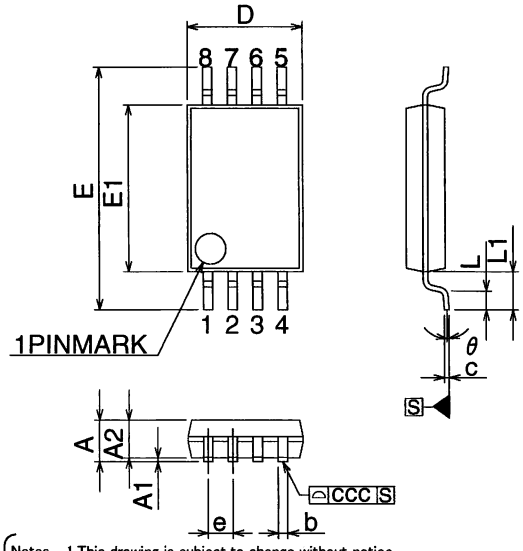


Notes 1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MS-012 variation AA.

Fig.-4 SO8 narrow Package Outline

◇ SO8 narrow Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
b	-	0.33	0.51	-	0.013	0.020
c	-	0.19	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
e	1.27	-	-	0.050	-	-
E	-	5.80	6.20	-	0.228	0.244
E1	-	3.80	4.00	-	0.150	0.157
L	-	0.40	1.27	0.050	0.016	0.050
θ1	-	0°	8°	-	0°	8°
ccc	-	-	0.10	-	-	0.004
h	-	0.25	0.50	-	0.010	0.020
θ2	45°	-	-	45°	-	-

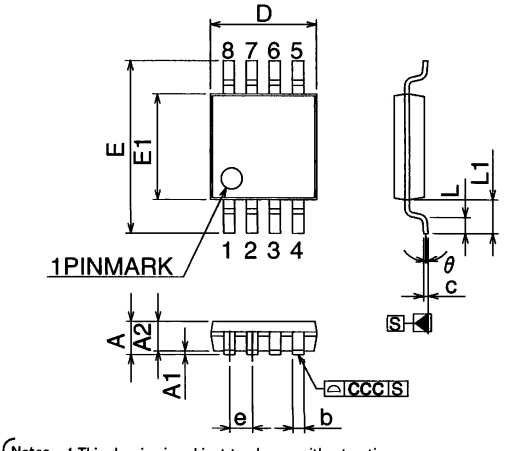


Notes 1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MO-153.

Fig.-5 TSSOP8 Package Outline

◇ TSSOP8 Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
ccc	-	-	0.100	-	-	0.0039
θ	-	0°	8°	-	0°	8°



Notes 1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MO-187 variation AA.

Fig.-6 TSSOP8 3×3mm^2 Package Outline

◇ TSSOP8 3×3mm^2 Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.100	-	-	0.0433
A1	-	0.050	0.150	-	0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b	-	0.250	0.400	-	0.0098	0.0157
c	-	0.120	0.230	-	0.0047	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950	-	-	0.0374	-	-
ccc	-	-	0.100	-	-	0.0039
θ	-	0°	6°	-	0°	6°

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