

VISHAY

Si7463DP

Vishay Siliconix

P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-40	0.0092 @ $V_{GS} = -10$ V	-18.6
	0.014 @ $V_{GS} = -4.5$ V	-15

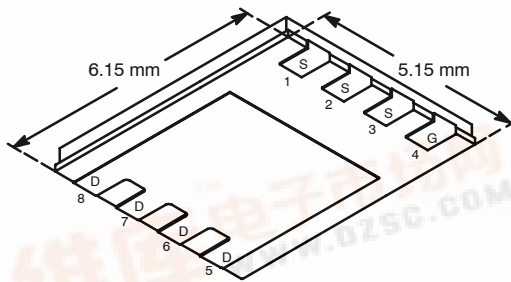
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

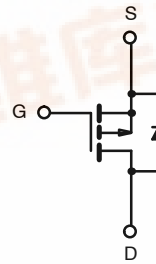
- Automotive
 - 12-V Boardnet
 - High-Side Switches
 - Motor Drives

PowerPAK SO-8



Bottom View

Ordering Information: Si7463DP-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-40		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^{\circ}\text{C}$) ^a	$T_A = 25^{\circ}\text{C}$	I_D	-18.6	-11	A
	$T_A = 70^{\circ}\text{C}$		-15	-8.9	
Pulsed Drain Current		I_{DM}	-60		
continuous Source Current (Diode Conduction) ^a		I_S	-4.5	-1.6	
Maximum Power Dissipation ^a	$T_A = 25^{\circ}\text{C}$	P_D	5.4	1.9	W
	$T_A = 70^{\circ}\text{C}$		3.4	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	18	23	$^\circ\text{C/W}$
		52	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.3	

Notes:
 a. Surface Mounted on 1" x 1" FR4 Board.

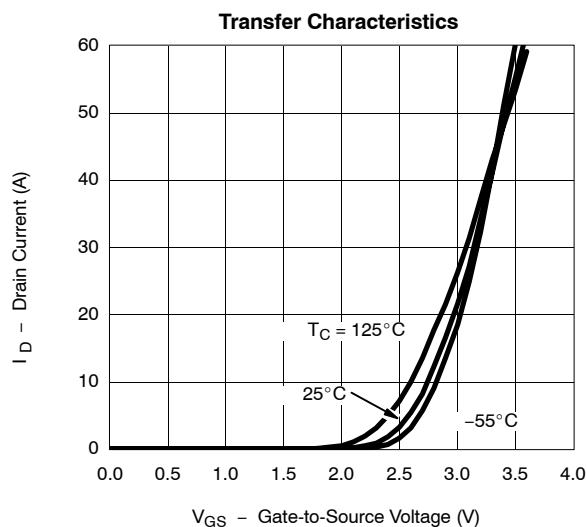
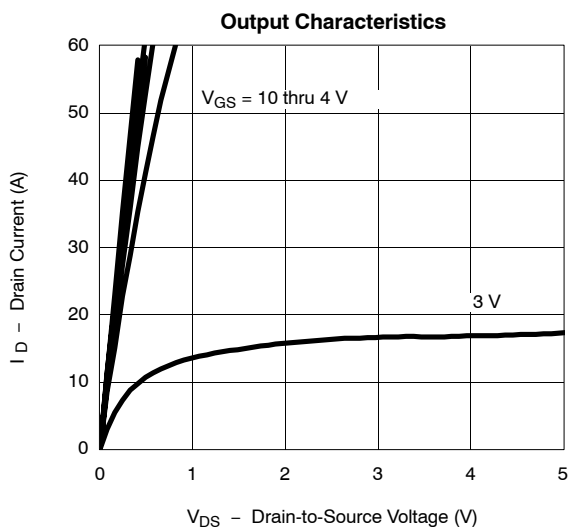
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1		-3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -40\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -18.6\ \text{A}$		0.0075	0.0092	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -15\ \text{A}$		0.011	0.014	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -18.6\ \text{A}$		50		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -4.5\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -20\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -18.6\ \text{A}$		121	140	nC
Gate-Source Charge	Q_{gs}			19.2		
Gate-Drain Charge	Q_{gd}			30.3		
Gate-Resistance	R_g			2.7		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\ \text{V}, R_L = 20\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		20	30	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			200	300	
Fall Time	t_f			100	150	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -4.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		45	70	

Notes

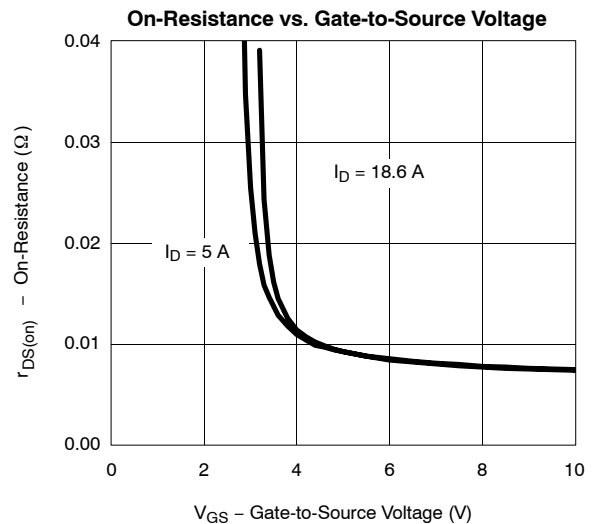
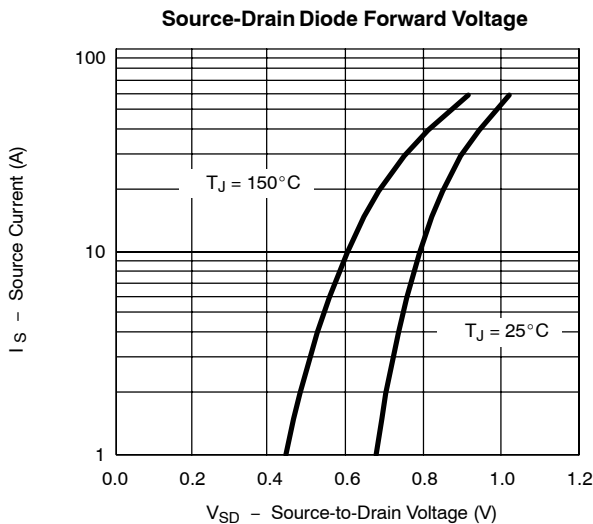
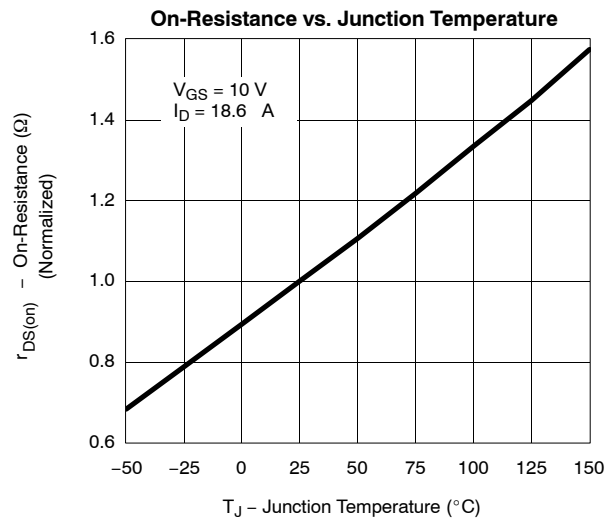
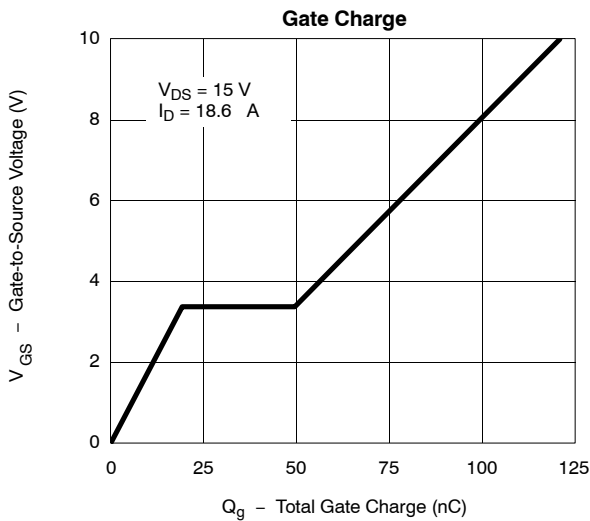
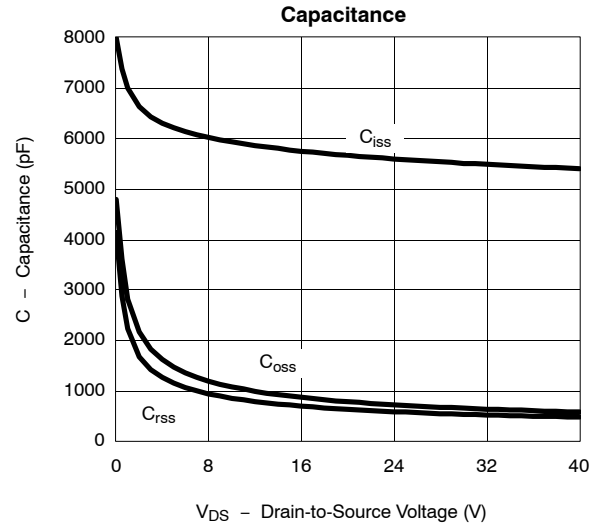
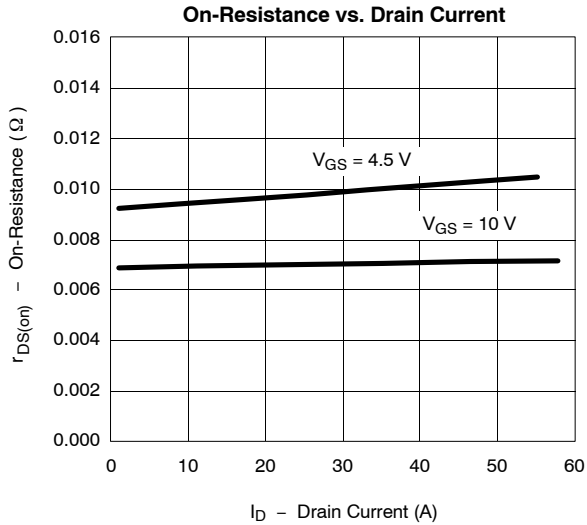
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

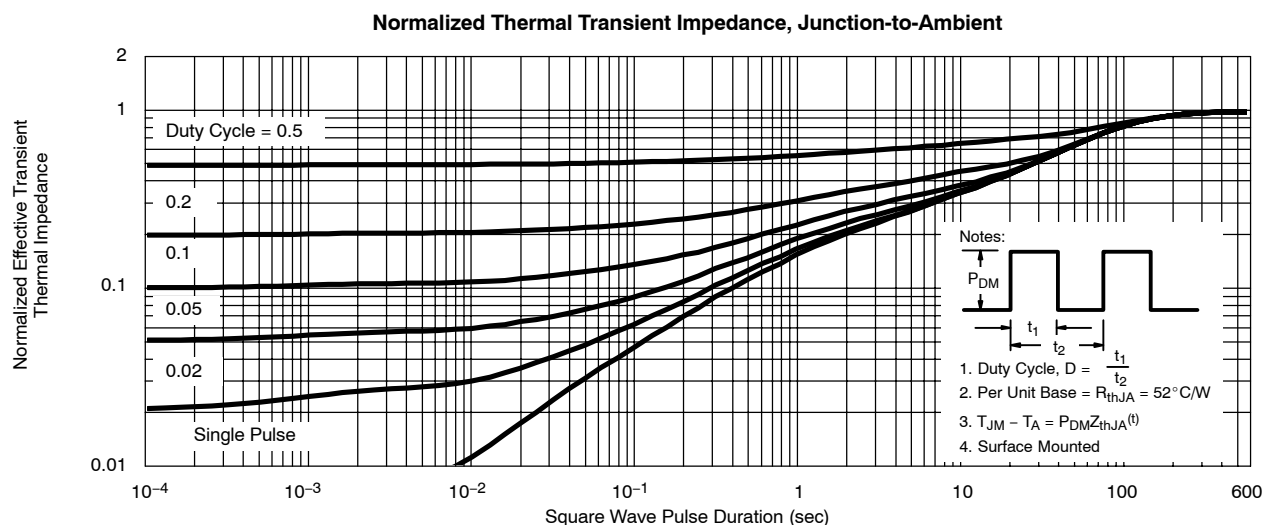
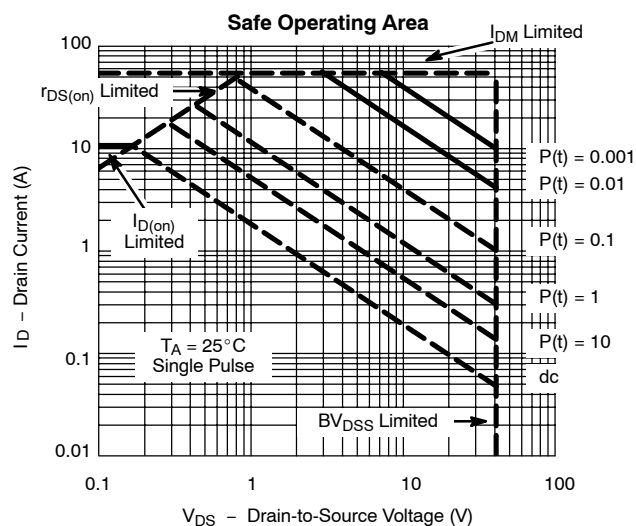
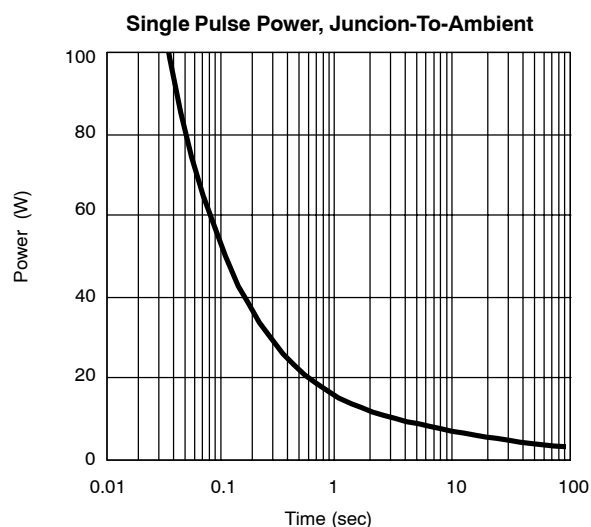
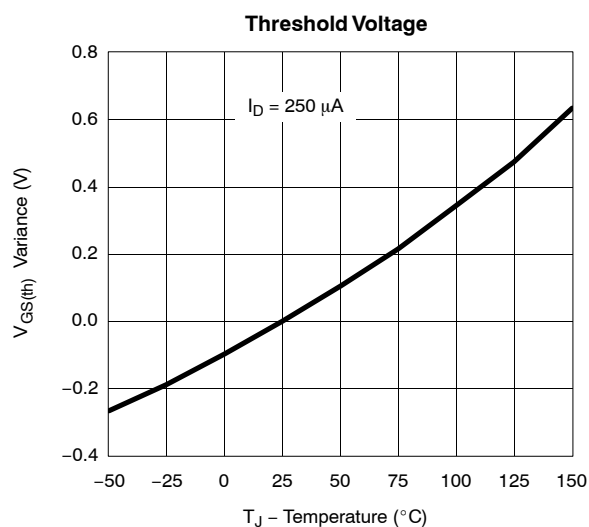




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