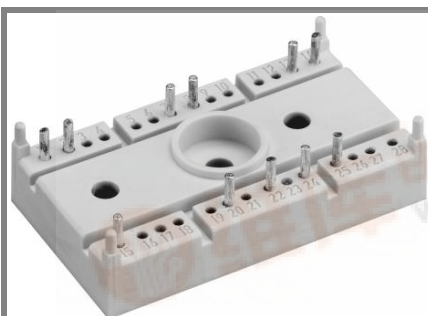


SK 40 DT



SEMITOP® 3

Controllable Bridge Rectifier

SK 40 DT

Preliminary Data

Features

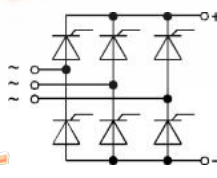
- Compact design
- One screw mounting
- Heat transfer and insulation through direct copper bonded aluminium oxide ceramic (DBC)
- Glass passivated thyristor chips
- Up to 1600V reverse voltage
- UL recognized, file no. E 63 532

Typical Applications

- Soft starters
- Light control
- Temperature control
- Motor control

V_{RSM} V	V_{RRM}, V_{DRM} V	$I_D = 42$ A (full conduction) ($T_s = 80$ °C)
900	800	SK 40 DT 08
1300	1200	SK 40 DT 12
1700	1600	SK 40 DT 16

Symbol	Conditions	Values	Units
I_D	$T_s = 80$ °C	42	A
I_{FSM}	$T_{vj} = 25$ °C; 10 ms	320	A
i^2t	$T_{vj} = 125$ °C; 10 ms	280	A
	$T_{vj} = 25$ °C; 8,3 ... 10 ms	510	A²s
	$T_{vj} = 125$ °C; 8,3...10 ms	390	A²s
V_T	$T_{vj} = 25$ °C; 75A	max. 2,45	V
$V_{T(TO)}$	$T_{vj} = 125$ °C;	max. 1,1	V
r_T	$T_{vj} = 125$ °C	max. 20	mΩ
I_{DD}, I_{RD}	$T_{vj} = 125$ °C; $V_{DD} = V_{DRM}, V_{RD} = V_{RRM}$	max. 8	mA
t_{gd}	$T_{vj} =$ °C; $I_G =$ A; $di_G/dt =$ A/μs		μs
t_{gr}	$V_D = \cdot V_{DRM}$		μs
$(dv/dt)_{cr}$	$T_{vj} = 125$ °C	max. 1000	V/μs
$(di/dt)_{cr}$	$T_{vj} = 125$ °C; $f = 50...60$ Hz	max. 100	A/μs
t_q	$T_{vj} = 125$ °C; typ.	80	μs
I_H	$T_{vj} = 25$ °C; typ. / max.	80 / 150	mA
I_L	$T_{vj} = 25$ °C; $R_G = 33$ Ω	150 / 300	mA
V_{GT}	$T_{vj} = 25$ °C; d.c.	min. 2	V
I_{GT}	$T_{vj} = 25$ °C; d.c.	min. 100	mA
V_{GD}	$T_{vj} = 125$ °C; d.c.	max. 0,25	V
I_{GD}	$T_{vj} = 125$ °C; d.c.	max. 3	mA
$R_{th(j-s)}$	Per thyristor	1,7	K/W
T_{solder}	Terminals, 10s	260	°C
T_{vj}		-40...+125	°C
T_{stg}		-40...+125	°C
V_{isol}	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3000 (2500)	V
M_s	Mounting torque to heatsink	2,5	Nm
m	weight	30	g
Case	SEMITOP® 3	T 15	



DT



SK 40 DT

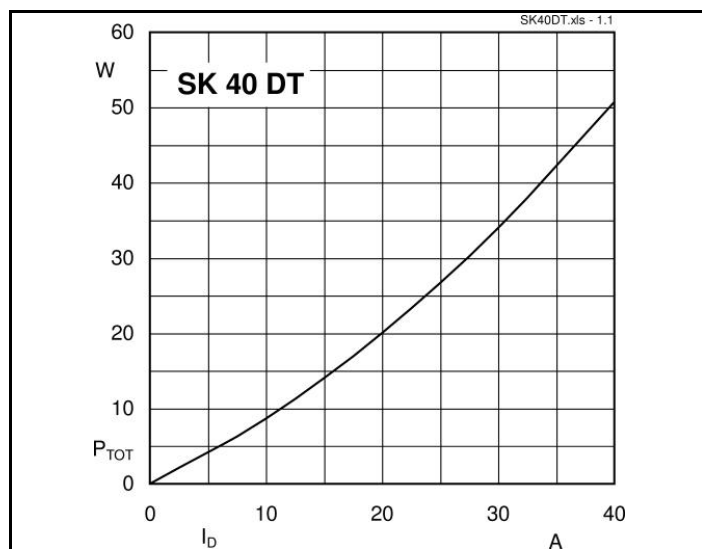


Fig. 1 Power dissipation vs. output current

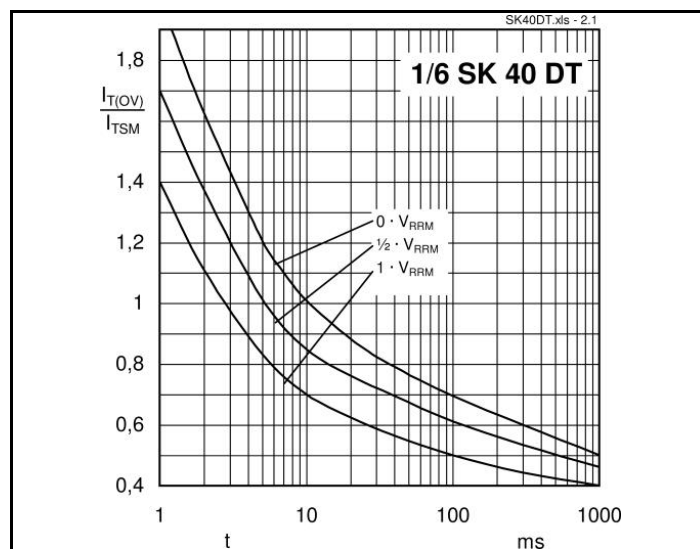


Fig. 2 Surge overload current vs. time

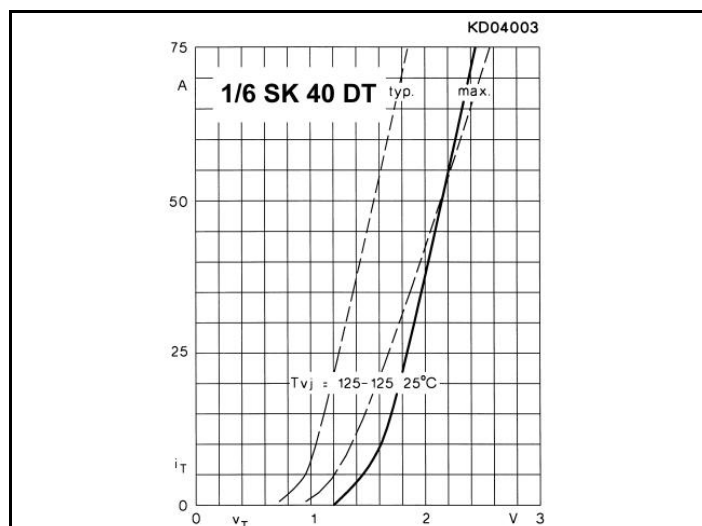


Fig. 3 Forward characteristics of single thyristor

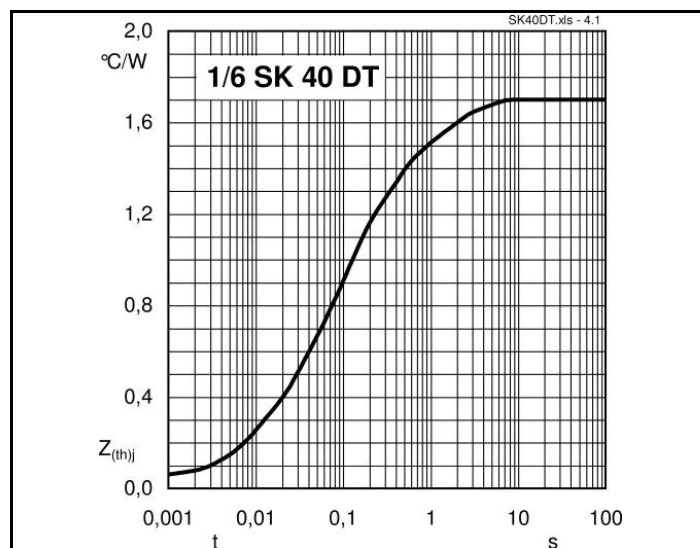


Fig. 4 Transient thermal impedance vs. time for single thyristor

SK 40 DT

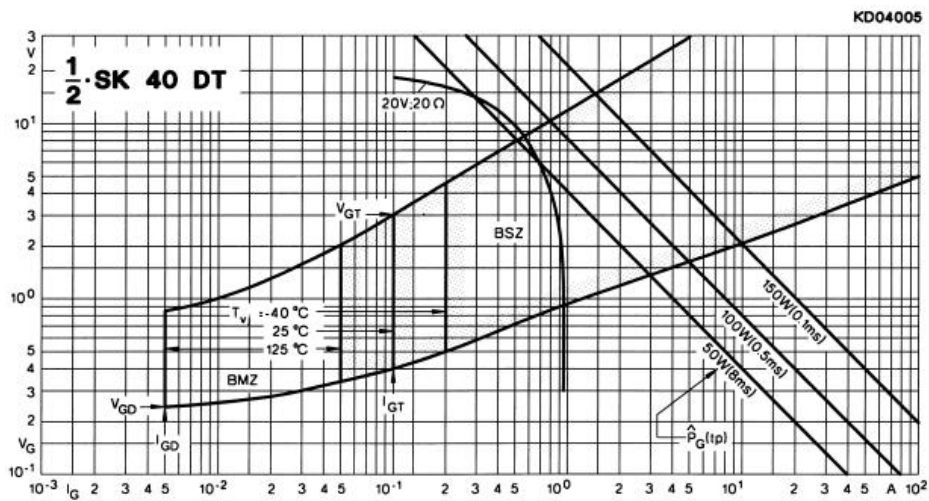
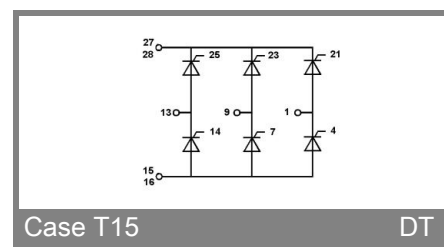
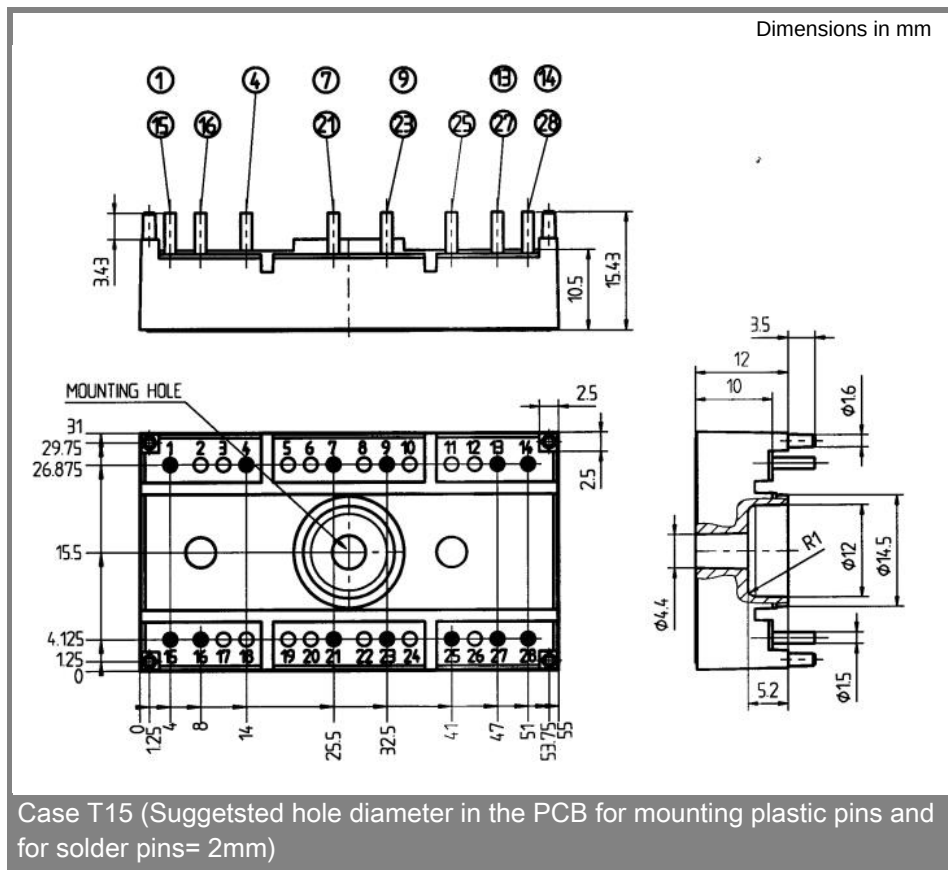


Fig. 5 Gate trigger characteristics



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