SN65220, SN65240, SN75240
SINGLE AND DUAL UNIVERSAL SERIAL BUS PORT TRANSIENT SUPPRESSORS

SLLS266C – FEBRUARY 1997 – REVISED MARCH 2000

- **Design to Protect Submicron 3-V or 5-V Silicon from Noise Transients**
- **Applicable to Two High- or Low-Speed Universal Serial Bus (USB) Host, Hub, or Peripheral Ports**
- **Port ESD Protection Capability Exceeds:**
  - **15-kV Human Body Model**
  - **2-kV Machine Model**
- **Low Current Leakage . . . 1 μA Max**
- **Stand-Off Voltage . . . 6.0 V Min**
- **Low Capacitance . . . 35 pF Typ**

description

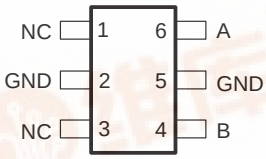
The SN65220 is a single transient voltage suppressor and the SN75240 and SN65240 are dual transient voltage suppressors designed to provide additional electrical noise transient protection to two USB ports. Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver and/or the USB ASIC if they are of sufficient magnitude and duration. The USB ports are typically implemented in 3-V or 5-V digital CMOS with very limited ESD protection. The SN65220, SN75240, and SN65240 can significantly increase the port ESD protection level and reduce the risk of damage to the large and expensive circuits of the USB port.

The SN75240 is characterized for operation from 0°C to 70°C. The SN65220 and SN65240 are characterized for operation from –40°C to 85°C. IEC1000-4-2 ESD performance is measured at the system level and system design influences the results of these tests. A high compliance level may be attained with proper system design.

IEC1000-4-2 Compliance Test Levels

IEC1000-4-2 COMPLIANCE LEVEL	MAXIMUM TEST VOLTAGE	
	CONTACT DISCHARGE (kV)	AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

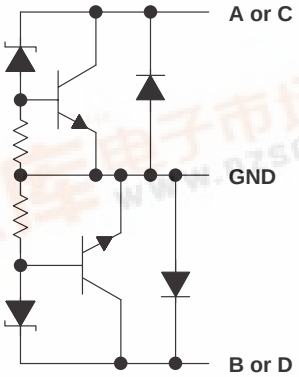
SN65220
(Marked as SADI)
DBV PACKAGE
(TOP VIEW)



SN65240, SN75240
(Marked as A65240 or A75240)
P OR PW PACKAGE
(TOP VIEW)

NC – No internal connection

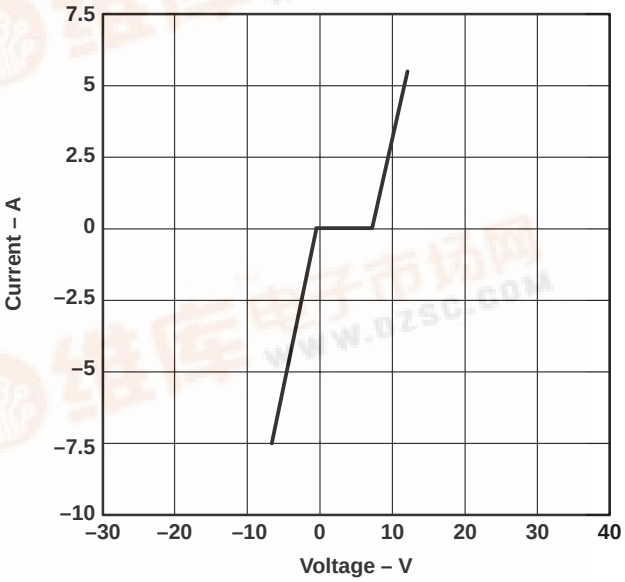
schematic



(One Suppressor Shown)

NOTE A: All four GND terminals should be connected to ground.

CURRENT vs VOLTAGE



NOTE A: Typical current versus voltage curve was derived using the IEC 1.2/50-μs surge waveform.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Continuous total power dissipation . . . . . See Dissipation Rating Table
Electrostatic discharge . . . . . Class 3, A:15 kV, B: 2 kV
Peak power dissipation, $P_{D(peak)}$ . . . . . 60 W
Peak forward surge current, I_{FSM} . . . . . 3 A
Peak reverse surge current, I_{RSM} . . . . . –9 A
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	246 mW	200 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW
PW	520 mW	4.2 mW/°C	331 mW	268 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	MAX	UNIT
Operating free-air temperature, T_A	SN65240, SN65220	–40	85	°C
	SN75240	0	70	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	µA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals		7		V

APPLICATION INFORMATION

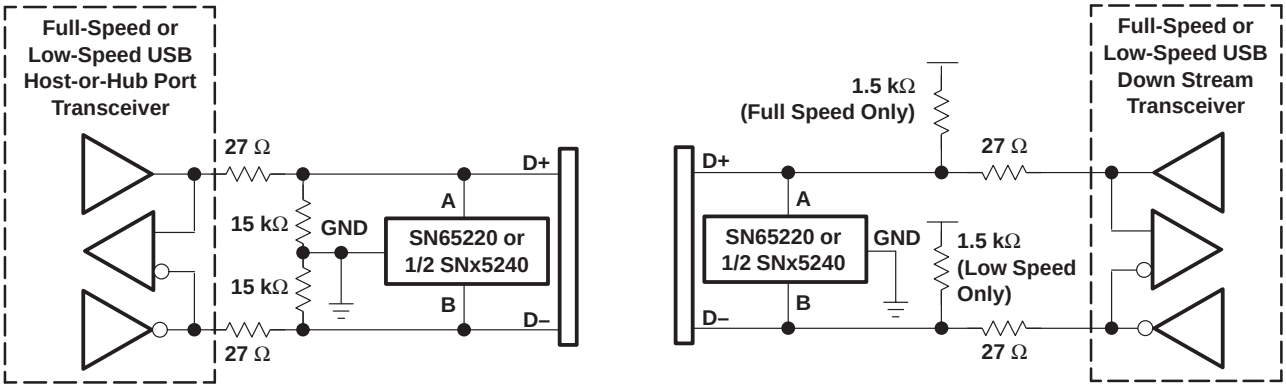
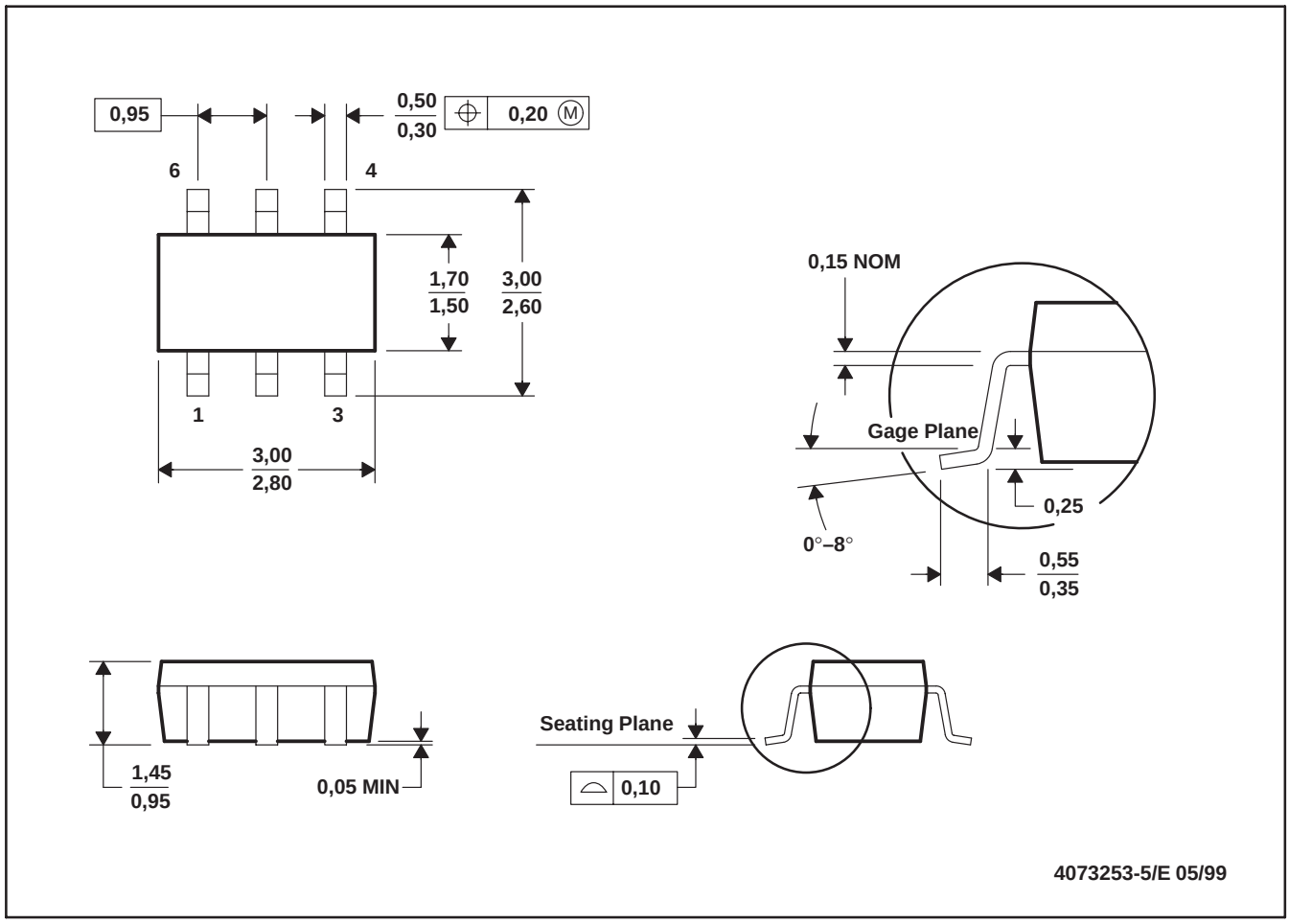


Figure 1. Typical USB Application

MECHANICAL INFORMATION

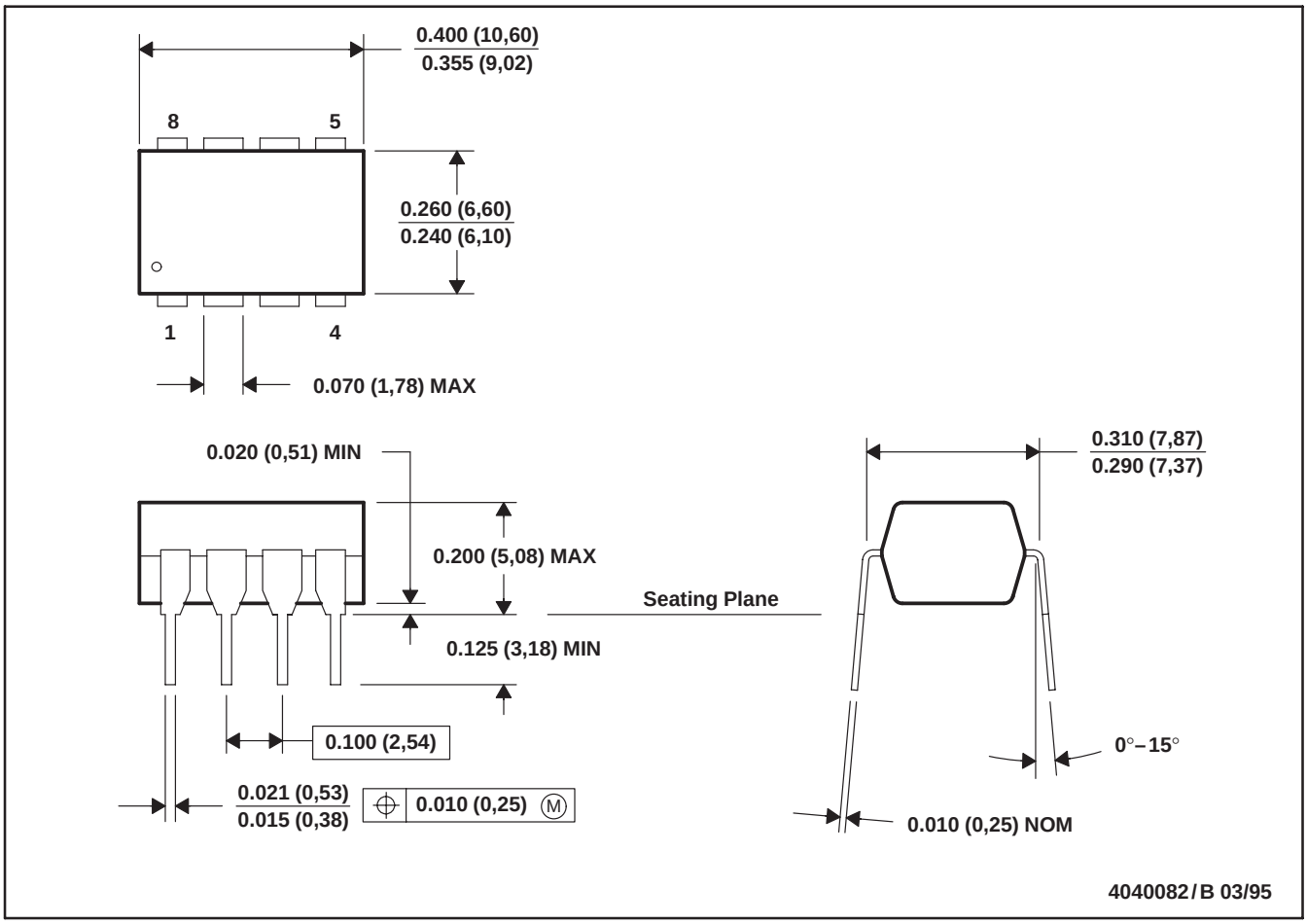
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

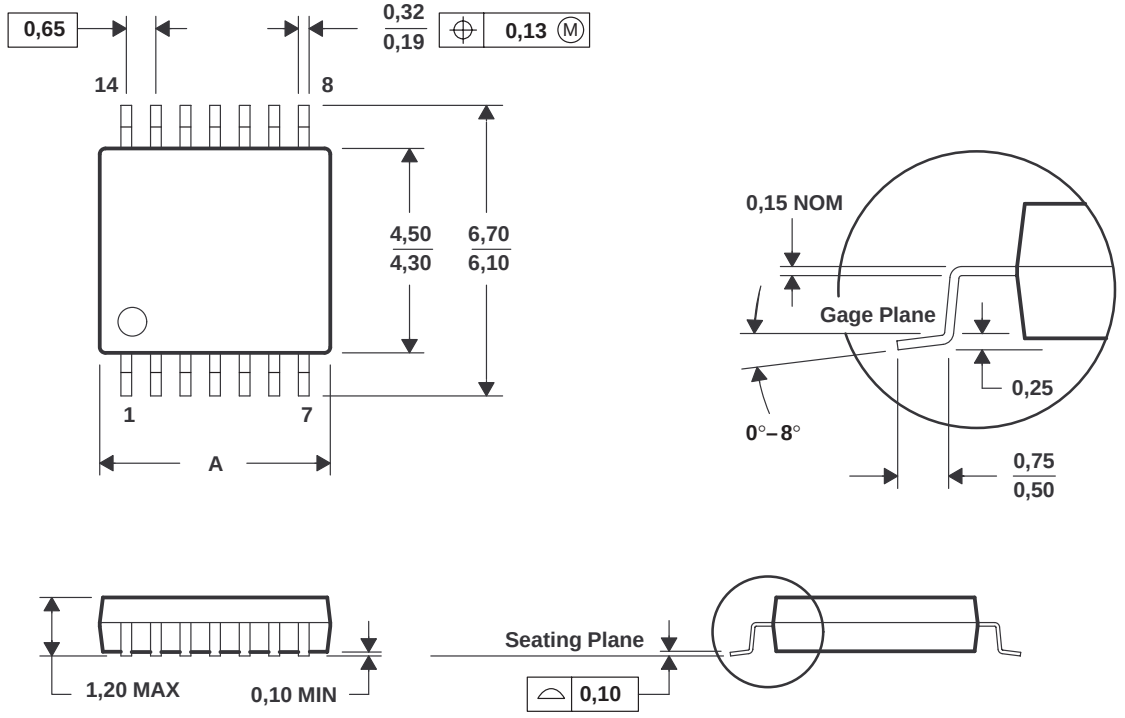


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.