

SN74AHC244Q OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SGDS017 – FEBRUARY 2002

- Q Devices Meet Automotive Performance Requirements
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

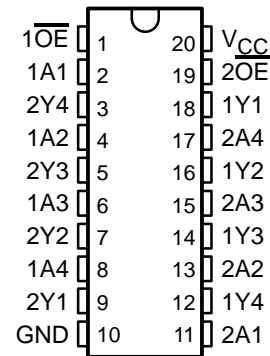
description

This octal buffer/driver is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHC244Q is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DW OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 125°C | SOIC – D | Tape and reel | SN74AHC244QDWR | AHC244Q |
| | TSSOP – PW | Tape and reel | SN74AHC244QPWR | HA244Q |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 4-bit buffer/driver)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |



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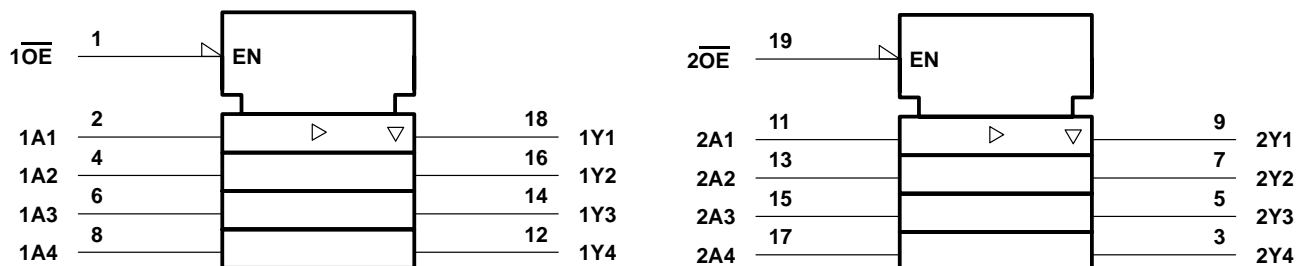
SN74AHC244Q

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

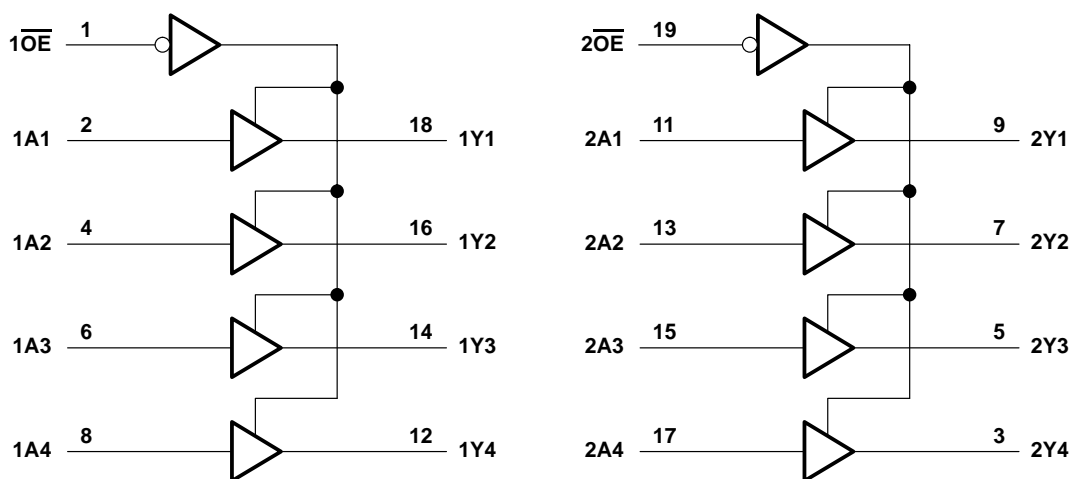
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DW package | 58°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---------------------------------|------|-----------------|------|
| V _{CC} | Supply voltage | | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | V |
| | | V _{CC} = 3 V | 2.1 | | |
| | | V _{CC} = 5.5 V | 3.85 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | V |
| | | V _{CC} = 3 V | | 0.9 | |
| | | V _{CC} = 5.5 V | | 1.65 | |
| V _I | Input voltage | | 0 | 5.5 | V |
| V _O | Output voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | –50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | –4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | | –8 | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | 4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | | 8 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | | 20 | |
| T _A | Operating free-air temperature | | –40 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|-----------------|-----------------------|-----|-------|------|------|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = –50 μA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | I _{OH} = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | I _{OH} = –8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | | 0.5 | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | | 0.5 | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | μA |
| I _{OZ} | V _O = V _{CC} or GND, V _I ($\overline{\text{OE}}$) = V _{IL} or V _{IH} | 5.5 V | | | ±0.25 | | ±2.5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 40 | μA |
| C _i | V _I = V _{CC} or GND | 5 V | | 2 | 10 | | | pF |
| C _o | V _O = V _{CC} or GND | 5 V | | 3.5 | | | | pF |

SN74AHC244Q

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|------|-----|------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 5.8 | 8.4 | 1 | 10 | ns | |
| t_{PHL} | | | | 5.8 | 8.4 | 1 | 10 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 6.6 | 10.6 | 1 | 12.5 | ns | |
| t_{PZL} | | | | 6.6 | 10.6 | 1 | 12.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 5 | 9.7 | 1 | 11 | ns | |
| t_{PLZ} | | | | 5 | 9.7 | 1 | 11 | | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 8.3 | 11.9 | 1 | 13.5 | ns | |
| t_{PHL} | | | | 8.3 | 11.9 | 1 | 13.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 9.1 | 14.1 | 1 | 16 | ns | |
| t_{PZL} | | | | 9.1 | 14.1 | 1 | 16 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 10.3 | 14 | 1 | 16 | ns | |
| t_{PLZ} | | | | 10.3 | 14 | 1 | 16 | | |

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|-----|-----|------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 3.9 | 5.5 | 1 | 6.5 | ns | |
| t_{PHL} | | | | 3.9 | 5.5 | 1 | 6.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 4.7 | 7.3 | 1 | 8.5 | ns | |
| t_{PZL} | | | | 4.7 | 7.3 | 1 | 8.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 15\text{ pF}$ | 5 | 7.2 | 1 | 8.5 | ns | |
| t_{PLZ} | | | | 5 | 7.2 | 1 | 8.5 | | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 5.4 | 7.5 | 1 | 8.5 | ns | |
| t_{PHL} | | | | 5.4 | 7.5 | 1 | 8.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 6.2 | 9.3 | 1 | 10.5 | ns | |
| t_{PZL} | | | | 6.2 | 9.3 | 1 | 10.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 50\text{ pF}$ | 6.7 | 9.2 | 1 | 10.5 | ns | |
| t_{PLZ} | | | | 6.7 | 9.2 | 1 | 10.5 | | |

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | MIN | TYP | MAX | UNIT |
|--|-----|------|-----|------|
| $V_{OL(P)}$ Quiet output, maximum dynamic V_{OL} | | 0.5 | | V |
| $V_{OL(V)}$ Quiet output, minimum dynamic V_{OL} | | -0.2 | | V |
| $V_{OH(V)}$ Quiet output, minimum dynamic V_{OH} | | 4.8 | | V |
| $V_{IH(D)}$ High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

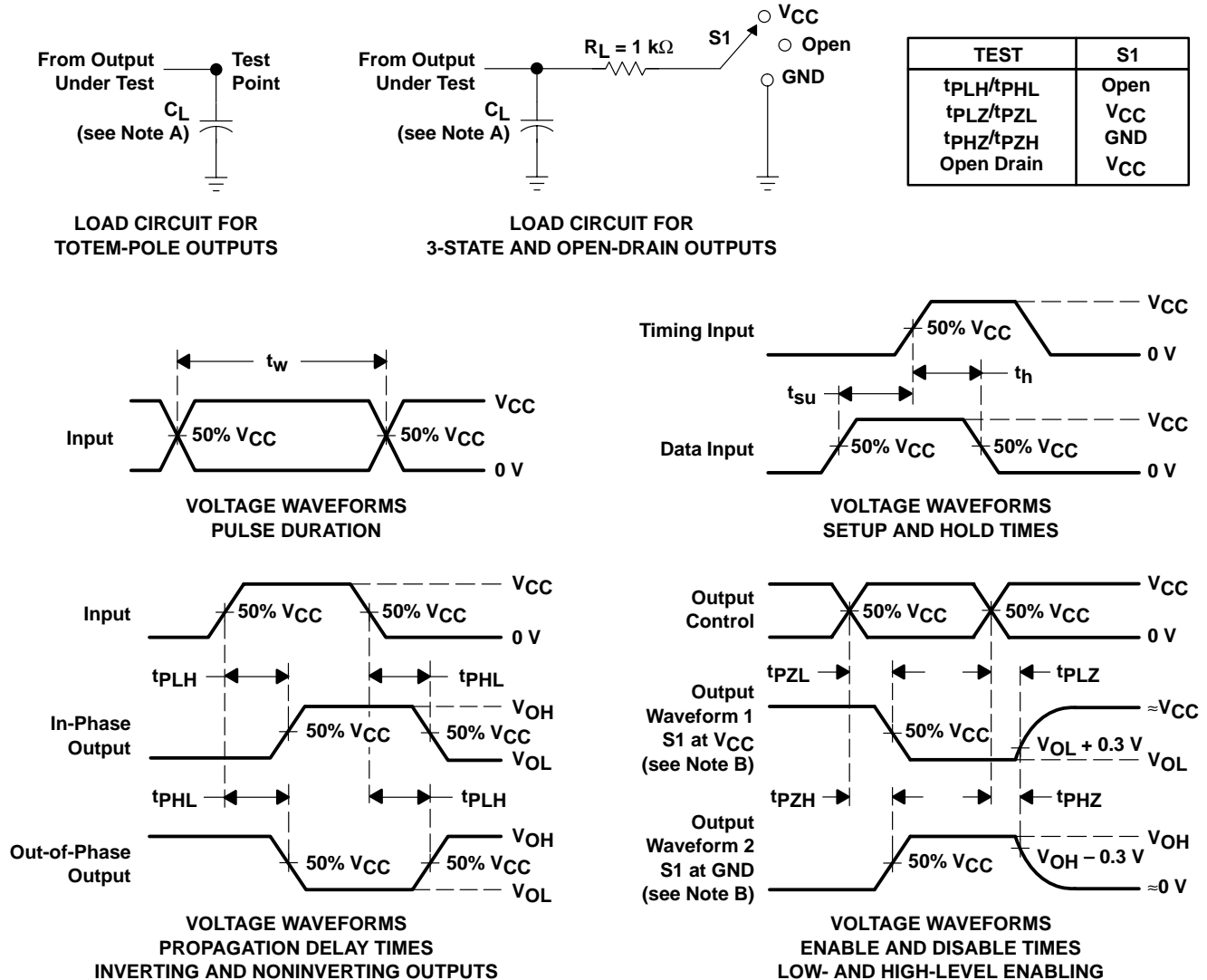
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 8.6 | pF |



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74AHC244QDWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74AHC244QDWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC244QPWR | ACTIVE | TSSOP | PW | 20 | 2000 | TBD | CU NIPDAU | Level-1-235C-UNLIM |
| SN74AHC244QPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

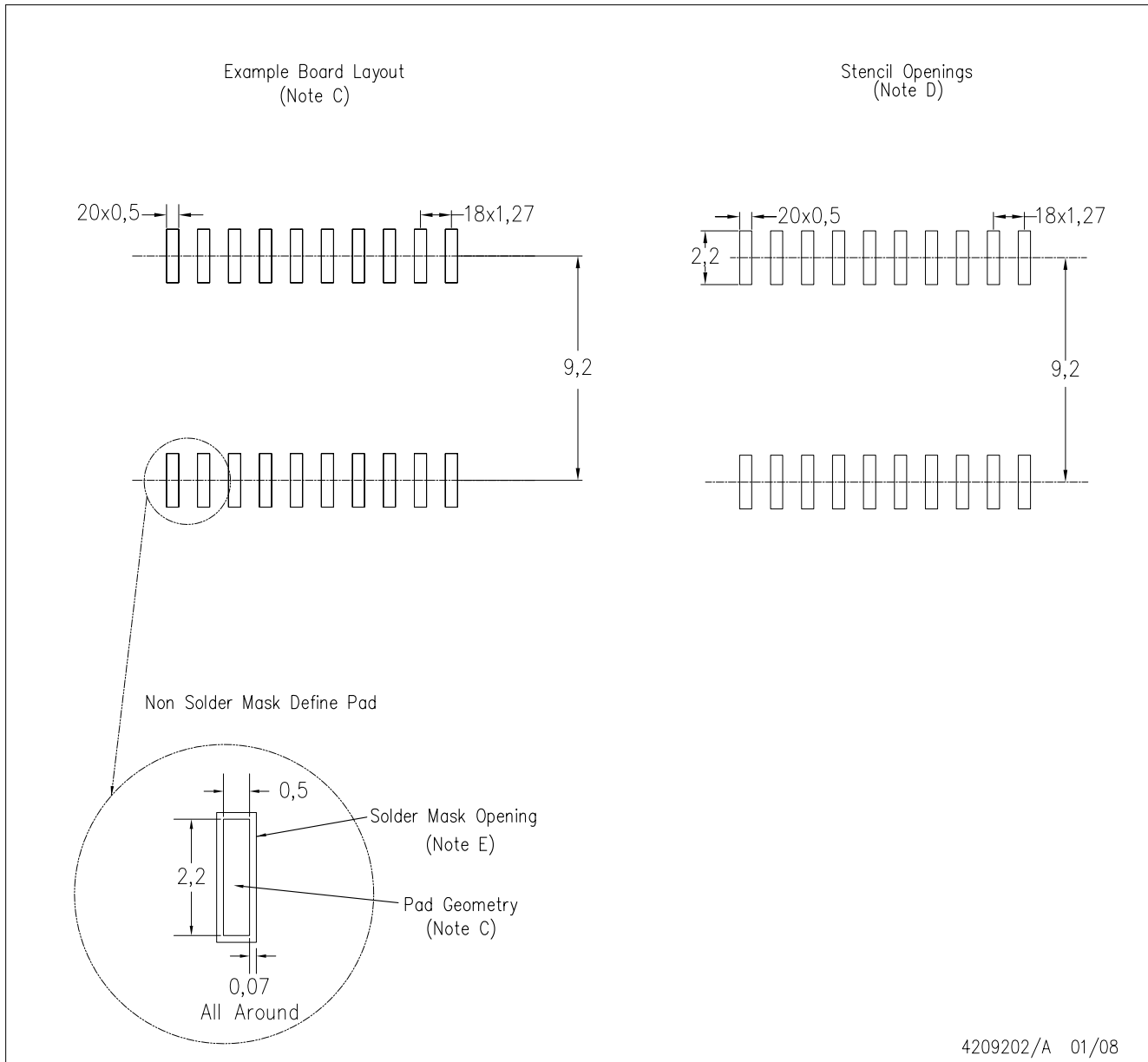
PLASTIC SMALL-OUTLINE PACKAGE



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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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