

SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30 8-INPUT POSITIVE-NAND GATES

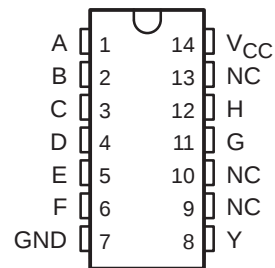
SDAS010C – MARCH 1984 – REVISED NOVEMBER 2000

description

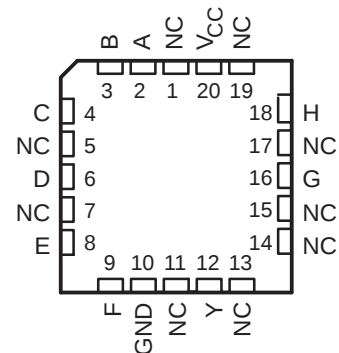
These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ or } Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . D OR N PACKAGE
SN74AS30 . . . DB PACKAGE
(TOP VIEW)



SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS30AN	SN74ALS30AN
			SN74AS30N	SN74AS30N
	SOIC – D	Tube	SN74ALS30AD	ALS30A
		Tape and reel	SN74ALS30AD	
		Tube	SN74AS30D	AS30
		Tape and reel	SN74AS30D	
–55°C to 125°C	SSOP – DB	Tape and reel	SN74AS30DBR	AS30
	CDIP – J	Tube	SNJ54ALS30AJ	SNJ54ALS30AJ
			SNJ54AS30J	SNJ54AS30J
	LCCC – FK	Tube	SNJ54ALS30AFK	SNJ54ALS30AFK
			SNJ54AS30FK	SNJ54AS30FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

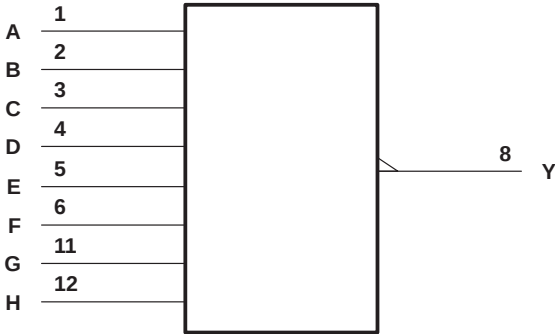
SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30
8-INPUT POSITIVE-NAND GATES

SDAS010C – MARCH 1984 – REVISED NOVEMBER 2000

FUNCTION TABLE

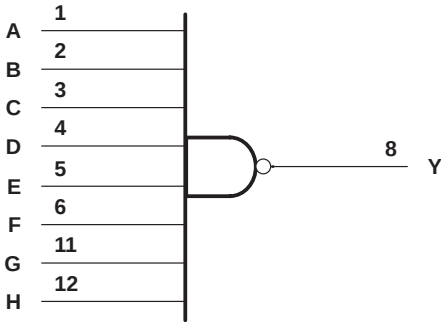
INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I	–0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	86°C/W
DB package	96°C/W
N package	80°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30

8-INPUT POSITIVE-NAND GATES

SDAS010C – MARCH 1984 – REVISED NOVEMBER 2000

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8 [†]	V
				0.7 [‡]	
I _{OH}	High-level output current			–0.4	mA
				–2	
I _{OL}	Low-level output current			4	mA
				8	
				20	
T _A	Operating free-air temperature			–55	°C
				125	
				–55	
				125	
				0	
				70	

[†] Applies to the 'AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of –55°C to 70°C.

[‡] Applies to the SN54ALS30A over the temperature range of 70°C to 125°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP [§]	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = –18 mA	'ALS30A			–1.5	V
			'AS30			–1.2	
V _{OH}	V _{CC} = 4.5 V to 5.5 V	I _{OH} = –0.4 mA	'ALS30A	V _{CC} –2			V
		I _{OH} = –2 mA	'AS30	V _{CC} –2			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	'ALS30A		0.25	0.4	V
		I _{OL} = 8 mA	SN74ALS30A		0.35	0.5	
		I _{OL} = 20 mA	'AS30		0.35	0.5	
I _I	V _{CC} = 5.5 V,	V _I = 7 V				0.1	mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V				20	μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V	'ALS30A			–0.1	mA
			'AS30			–0.5	
I _O [¶]	V _{CC} = 5.5 V,	V _O = 2.25 V	SN54ALS30A	–20		–112	mA
			SN74ALS30A	–30		–112	
			'AS30	–30		–112	
I _{CCH}	V _{CC} = 5.5 V,	V _I = 0	'ALS30A		0.22	0.36	mA
			'AS30		0.9	1.5	
I _{CCL}	V _{CC} = 5.5 V,	V _I = 4.5 V	'ALS30A		0.54	0.9	mA
			'AS30		3	4.9	

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[¶] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30
8-INPUT POSITIVE-NAND GATES

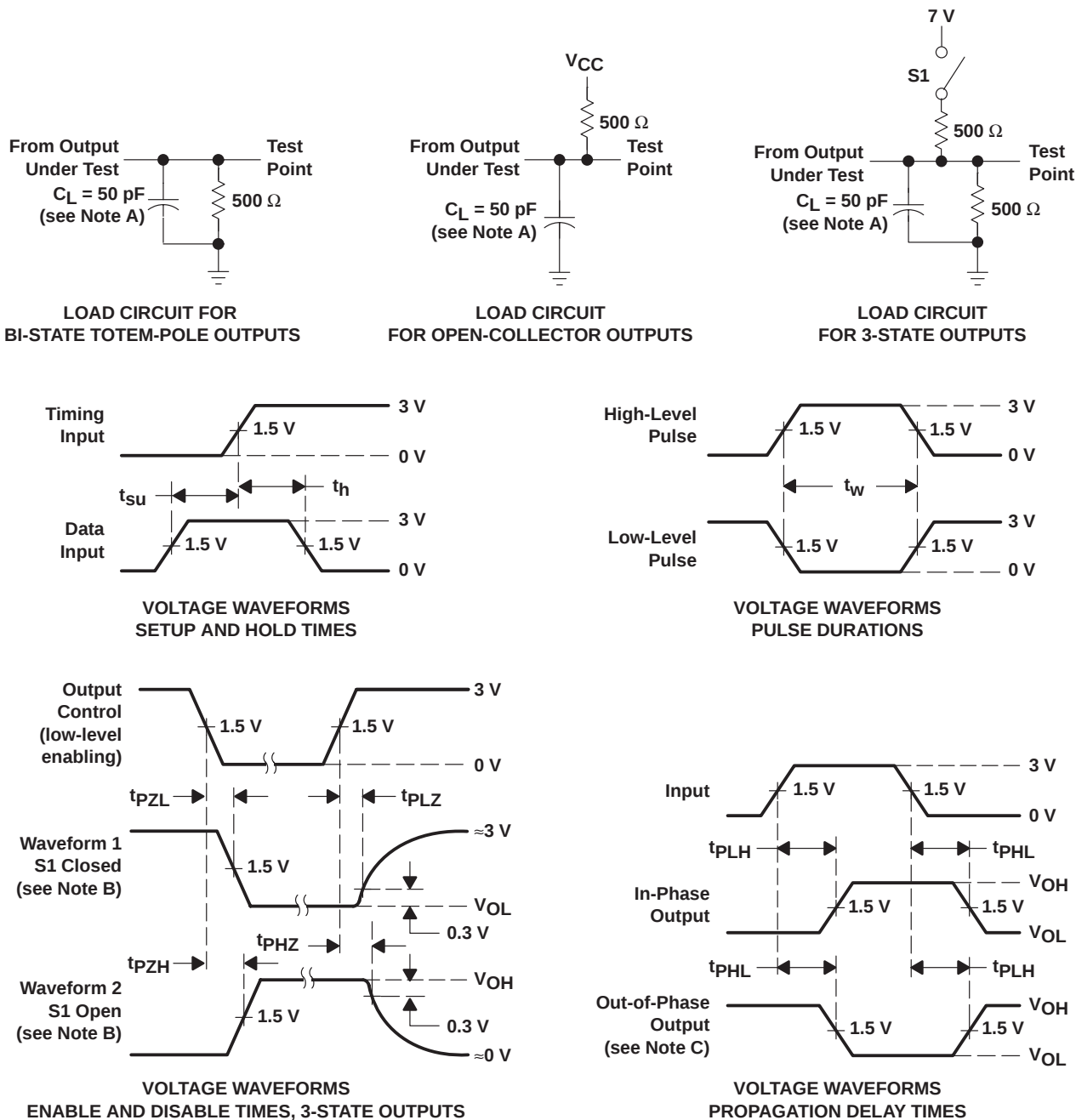
SDAS010C – MARCH 1984 – REVISED NOVEMBER 2000

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t _{PLH}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	10	
			SN54AS30	1	5.5	
			SN74AS30	1	5	
t _{PHL}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	12	
			SN54AS30	1	5	
			SN74AS30	1	4.5	



PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.