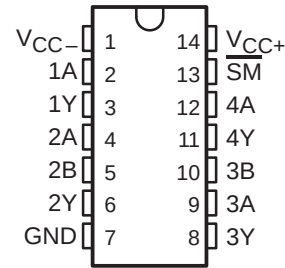


SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

- Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Supply Current
- Sleep Mode:
3-State Outputs in High-Impedance State
Ultra-Low Supply Current . . . 17 μ A Typ
- Improved Functional Replacement for:
SN75188,
Motorola MC1488,
National Semiconductor DS14C88, and
DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/ μ s
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ± 4.5 V to ± 15 V

D OR N PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGNS

description

The SN75C198 is a monolithic low-power BI-MOS device containing four low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/ μ s. This feature eliminates the need for external components.

The sleep-mode input, $\overline{SM}$, can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

$\overline{SM}$	INPUTS		OUTPUT Y
	A	B	
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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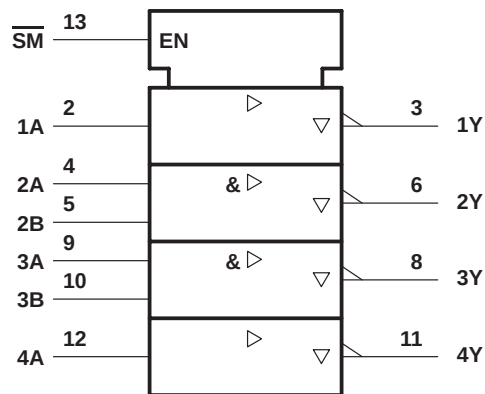
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SN75C198

QUADRUPLE LOW-POWER LINE DRIVERS

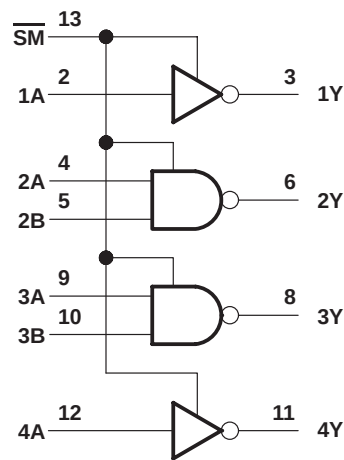
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logic symbol†

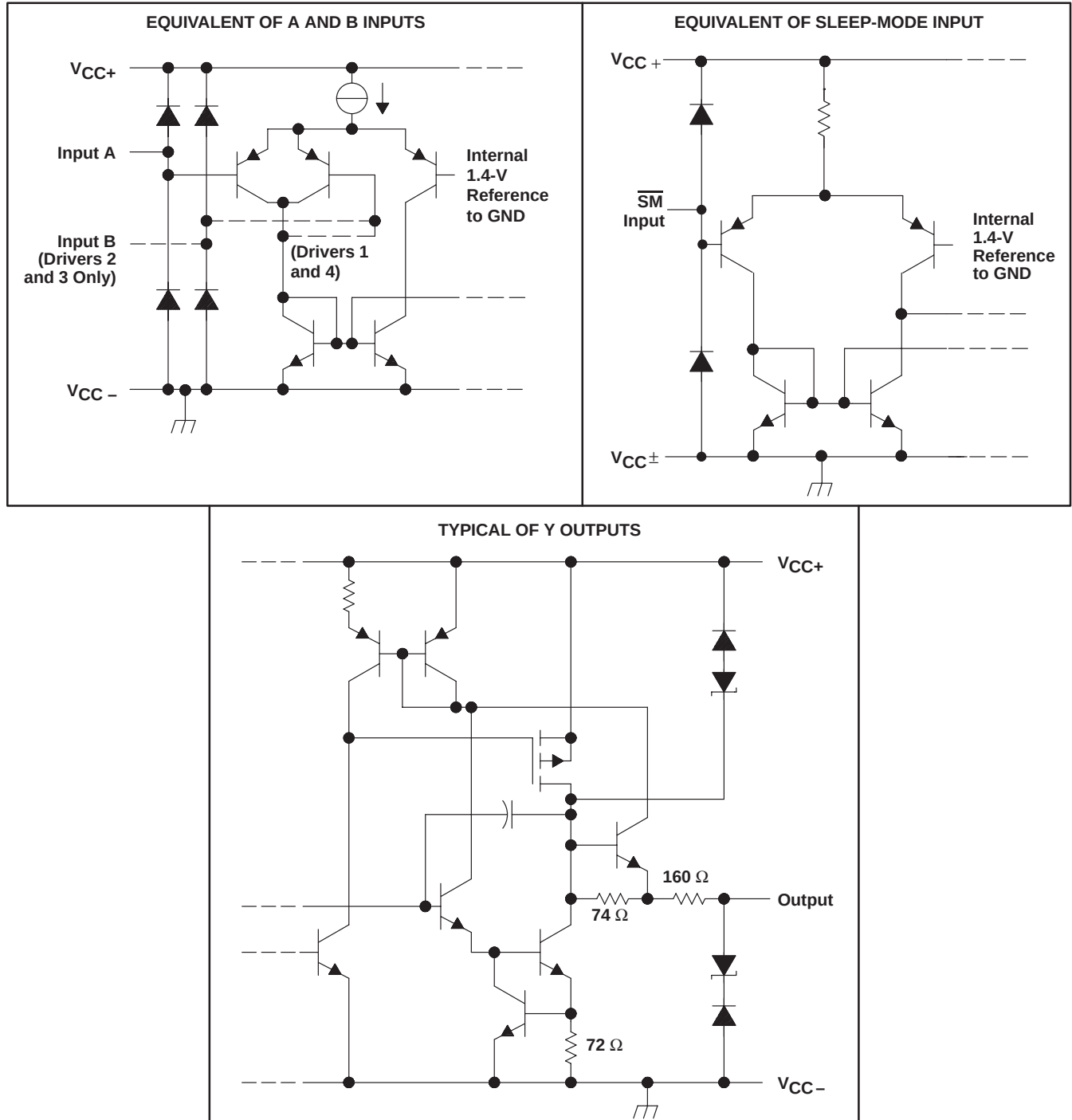


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

SN75C198

QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	15 V
Supply voltage, V_{CC-}	-15 V
Input voltage range, V_I	-15 V to 15 V
Output voltage range, V_O	$V_{CC-} - 6$ V to $V_{CC+} + 6$ V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN75C198	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	730 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	-4.5	-12	-15	V
Input voltage, V_I (see Figure 2)	$V_{CC-} + 2$		V_{CC+}	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}	A and B inputs			0.8
	SM input			0.6
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12$ V, $\overline{SM}$ at 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IH} = 0.8$ V, $R_L = 3$ k Ω	$V_{CC\pm} = \pm 5$ V	4			V
			$V_{CC\pm} = \pm 12$ V	10			
V_{OL}	Low-level output voltage (see Note 2)	$V_{IH} = 2$ V, $R_L = 3$ k Ω	$V_{CC\pm} = \pm 5$ V			–4	V
			$V_{CC\pm} = \pm 12$ V			–10	
I_{IH}	High-level input current	$V_I = 5$ V				10	μ A
I_{IL}	Low-level input current	$V_I = 0$ V				–10	μ A
I_{OZ}	High-impedance-state output current	$\overline{SM}$ at 0.6 V	$V_O = 12$ V, $V_{CC\pm} = \pm 12$ V			100	μ A
			$V_O = -12$ V, $V_{CC\pm} = \pm 12$ V			–100	
$I_{OS(H)}$	High-level short-circuit output current [‡]	$V_I = 0.8$ V, $V_O = 0$ or V_{CC-}		–4.5	–10	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current [‡]	$V_I = 2$ V, $V_O = 0$ or V_{CC+}		4.5	10	19.5	mA
r_o	Output resistance	$V_{CC\pm} = 0$, $V_O = -2$ V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	A and B inputs at 0.8 V or 2 V, No load	$V_{CC\pm} = \pm 5$ V		90	160	μ A
			$V_{CC\pm} = \pm 12$ V		95	160	
		A and B inputs at 0.8 V or 2 V, $R_L = 3$ k Ω , $\overline{SM}$ at 0.6 V	$V_{CC\pm} = \pm 5$ V		40		
			$V_{CC\pm} = \pm 12$ V		40		
I_{CC-}	Supply current from V_{CC-}	A and B inputs at 0.8 V or 2 V, No load	$V_{CC\pm} = \pm 5$ V		–90	–160	μ A
			$V_{CC\pm} = \pm 12$ V		–95	–160	
		A and B inputs at 0.8 V or 2 V, $R_L = 3$ k Ω , $\overline{SM}$ at 0.6 V	$V_{CC\pm} = \pm 5$ V		–40		
			$V_{CC\pm} = \pm 12$ V		–40		

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output [§]	$R_L = 3$ k Ω to 7 k Ω , See Figure 1	$C_L = 15$ pF,			3	μ s
t_{PHL}	Propagation delay time, high- to low-level output [§]					3.5	μ s
t_{TLH}	Transition time, low- to high-level output [¶]			0.53	1	3.2	μ s
t_{THL}	Transition time, high- to low-level output [¶]			0.53	1	3.2	μ s
t_{TLH}	Transition time, low- to high-level output [#]	$R_L = 3$ k Ω to 7 k Ω , See Figure 2	$C_L = 2500$ pF,		1.5		μ s
t_{THL}	Transition time, high- to low-level output [#]				1.5		μ s
t_{PZH}	Output enable time to high level	$R_L = 3$ k Ω to 7 k Ω , See Figure 3	$C_L = 15$ pF,			50	μ s
t_{PHZ}	Output disable time from high level					10	μ s
t_{PZL}	Output enable time to low level	$R_L = 3$ k Ω to 7 k Ω , See Figure 4	$C_L = 15$ pF,			15	μ s
t_{PLZ}	Output disable time from low level					10	μ s
SR	Output slew rate [#]	$R_L = 3$ k Ω to 7 k Ω , $C_L = 15$ pF		6	15	30	V/ μ s

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[§] t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.

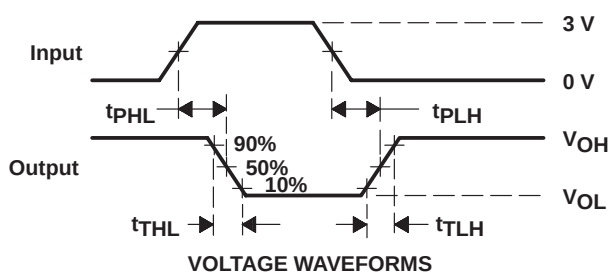
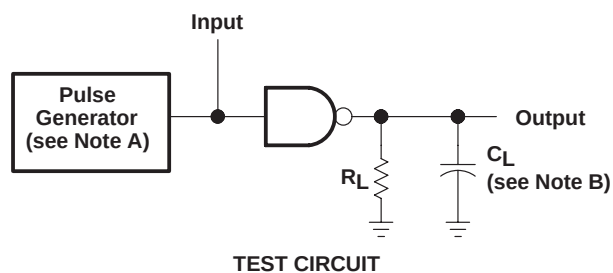
[¶] Measured between 10% and 90% points of output waveform

[#] Measured between 3-V and –3-V points of output waveform

SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

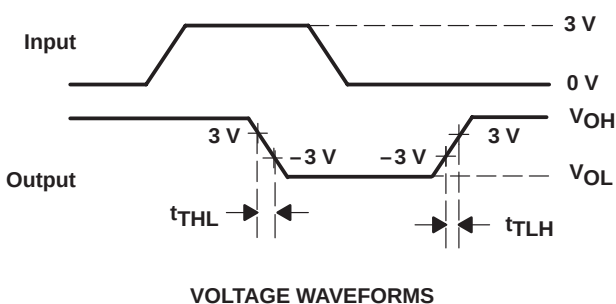
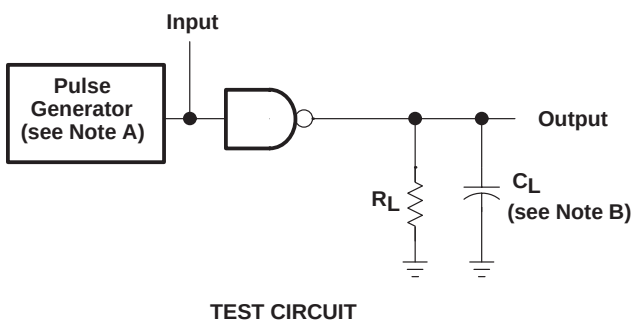
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PARAMETER MEASUREMENT INFORMATION



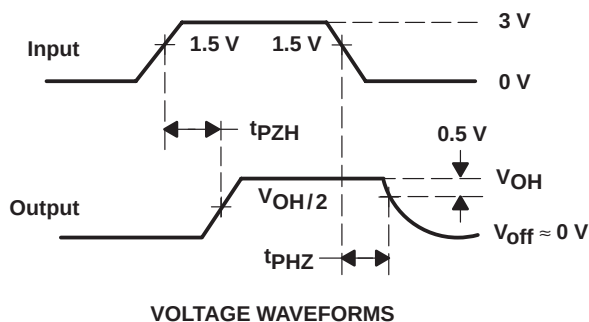
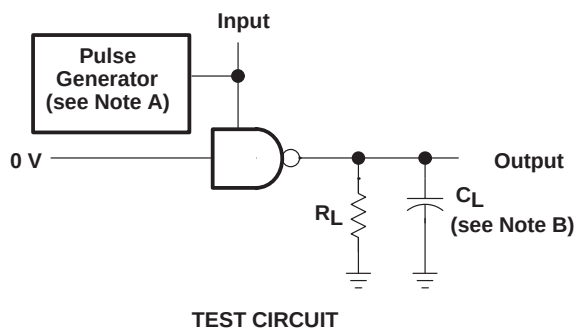
NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

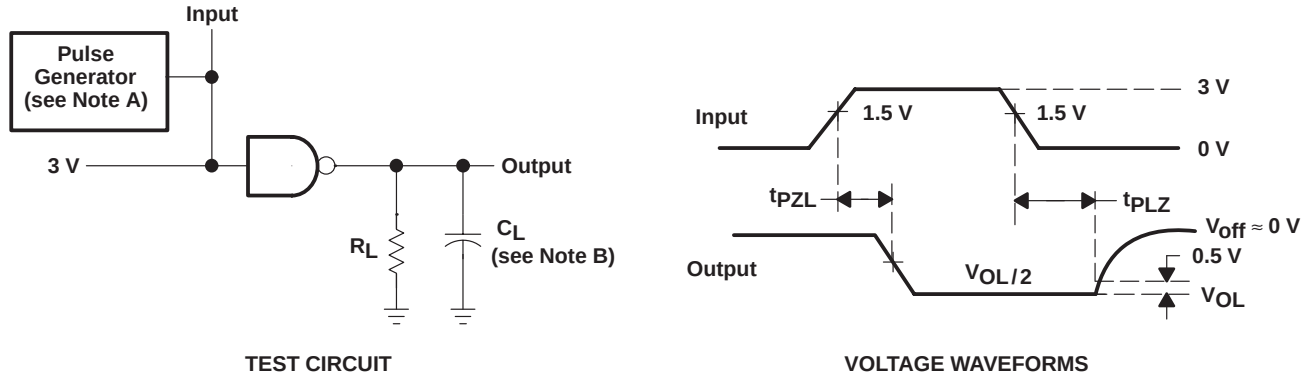
Figure 2. Test Circuit and Voltage Waveforms, Transition Times



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

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TYPICAL CHARACTERISTICS

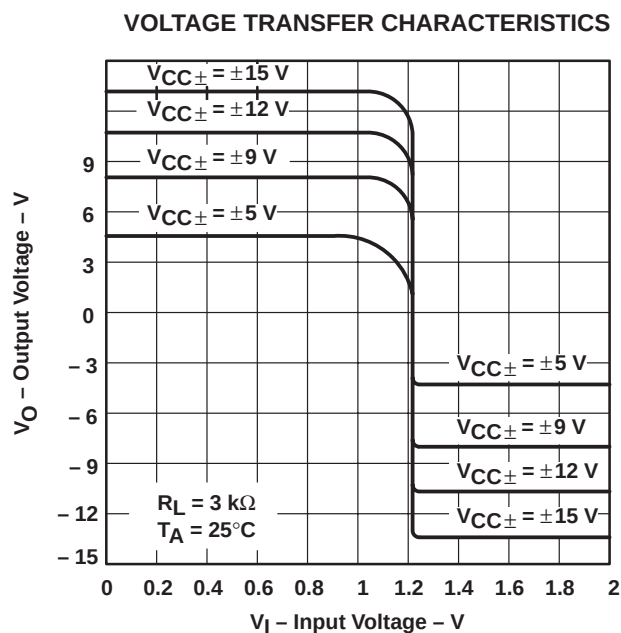


Figure 5

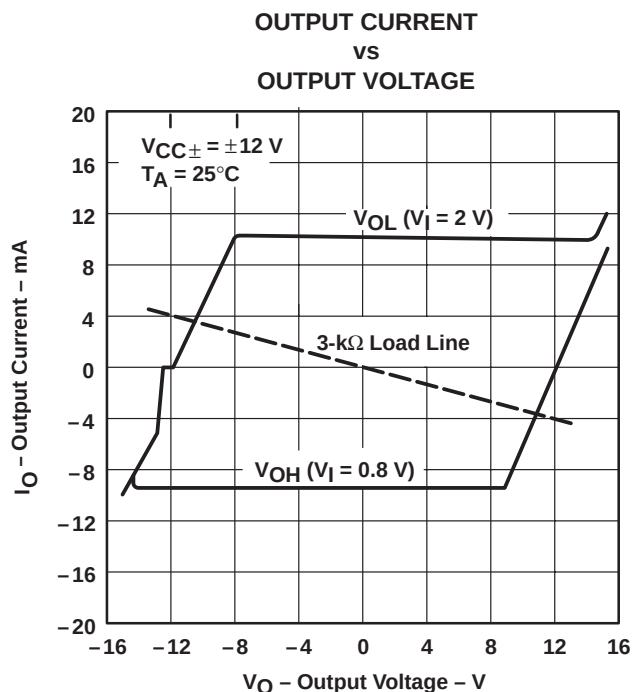


Figure 6

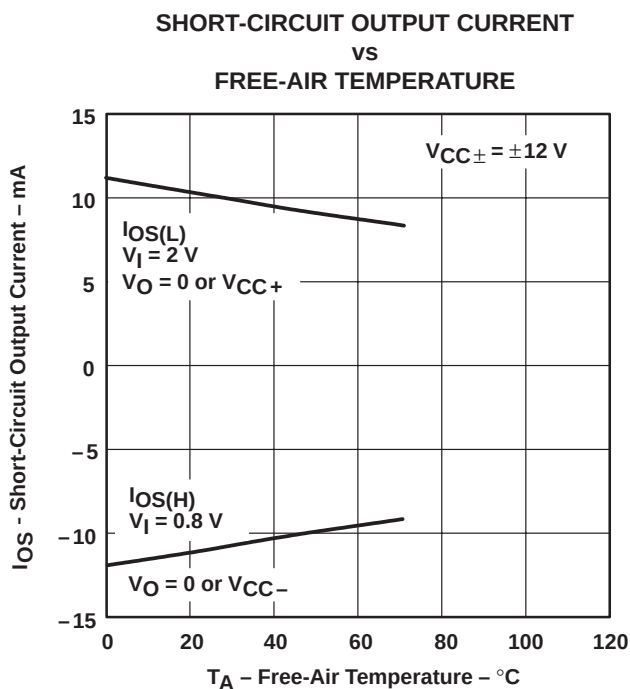


Figure 7

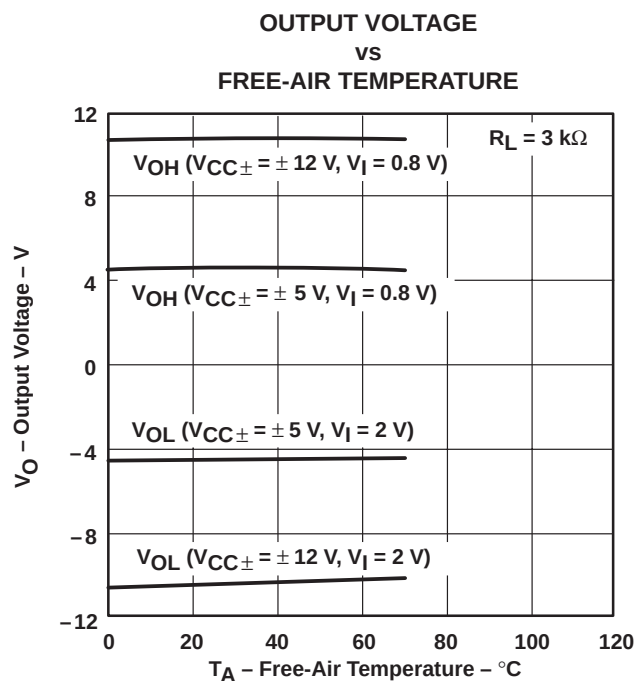
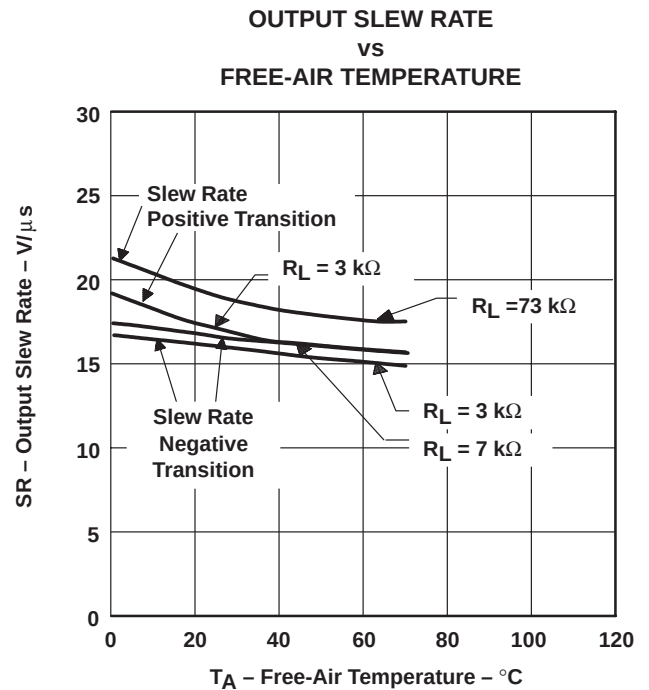
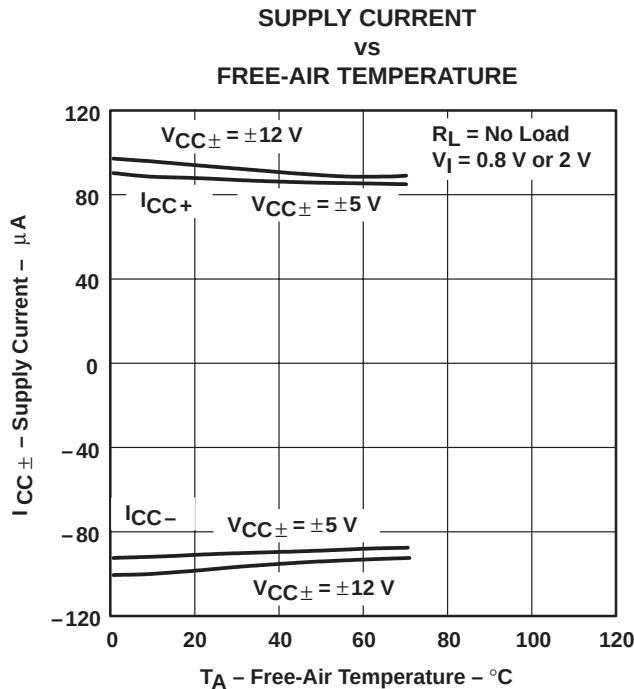
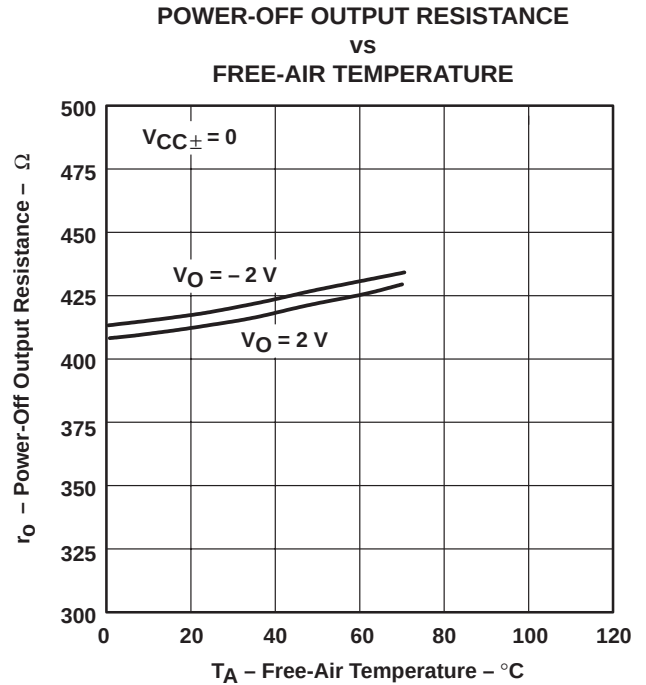
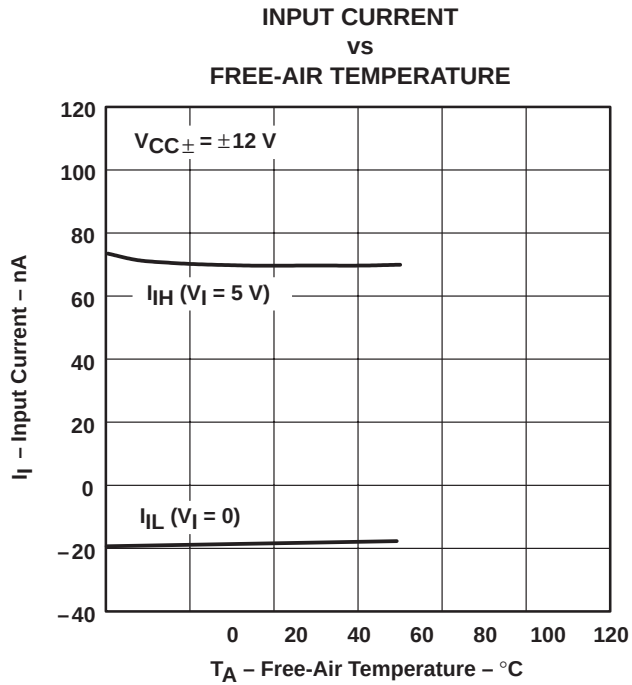


Figure 8

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

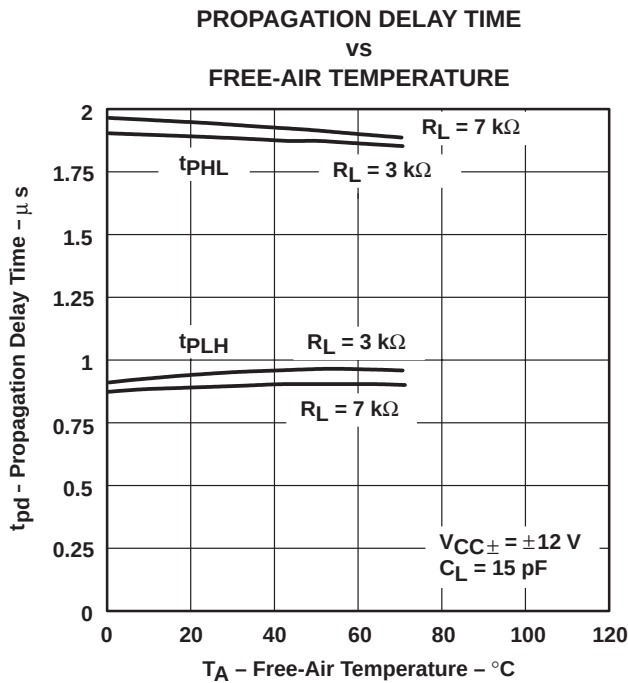


Figure 13

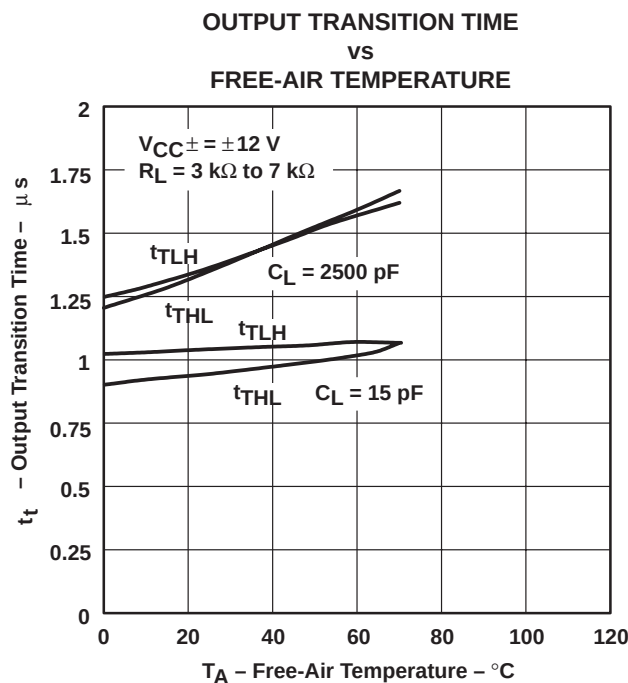


Figure 14

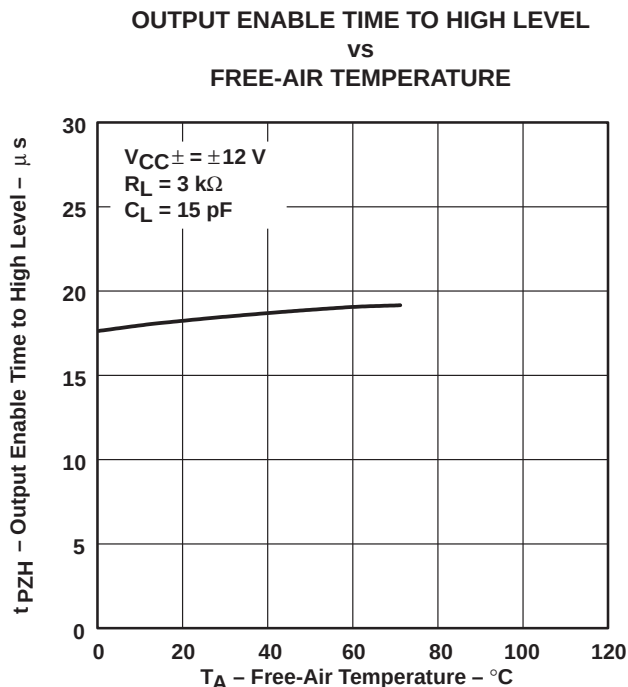


Figure 15

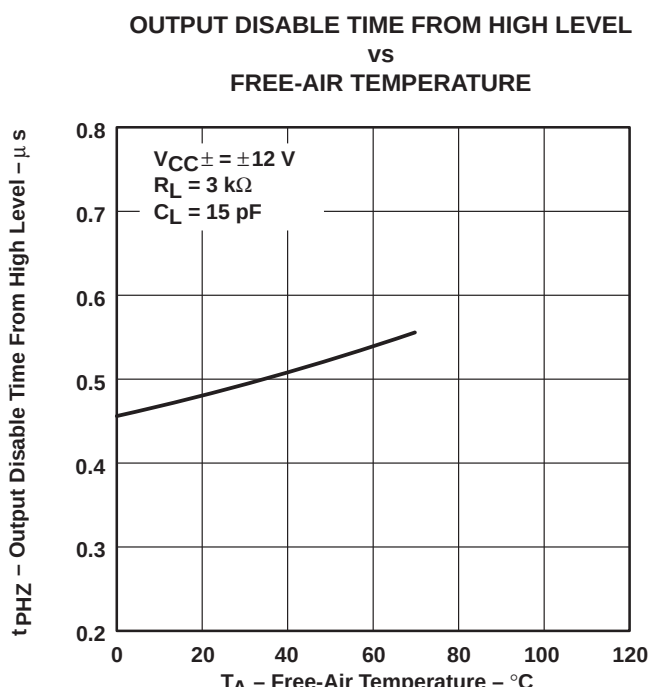


Figure 16

TYPICAL CHARACTERISTICS

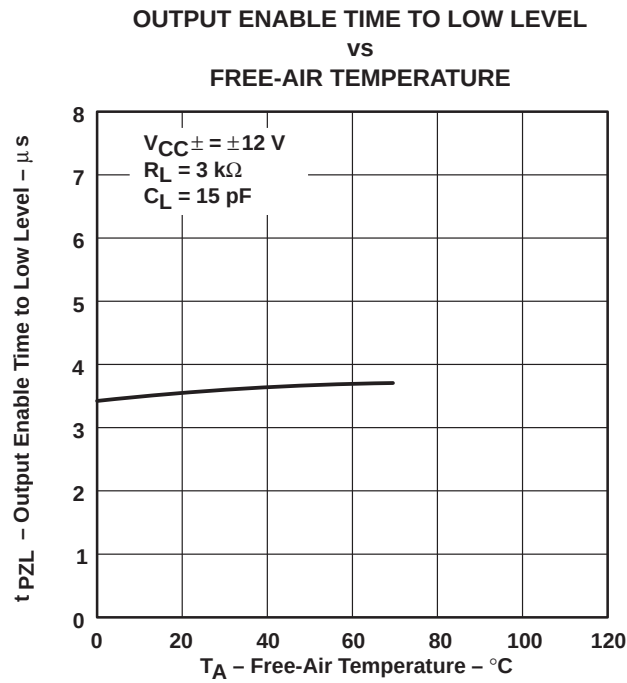


Figure 17

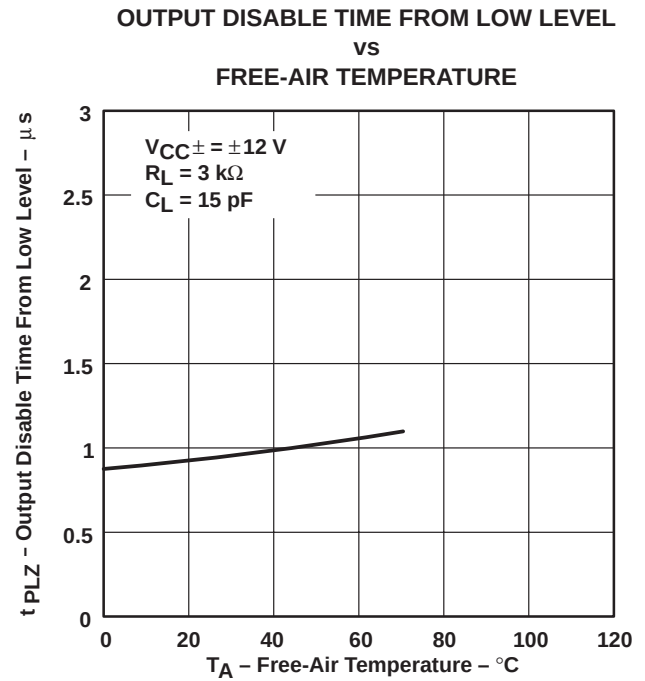


Figure 18

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75C198D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C198N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C198NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

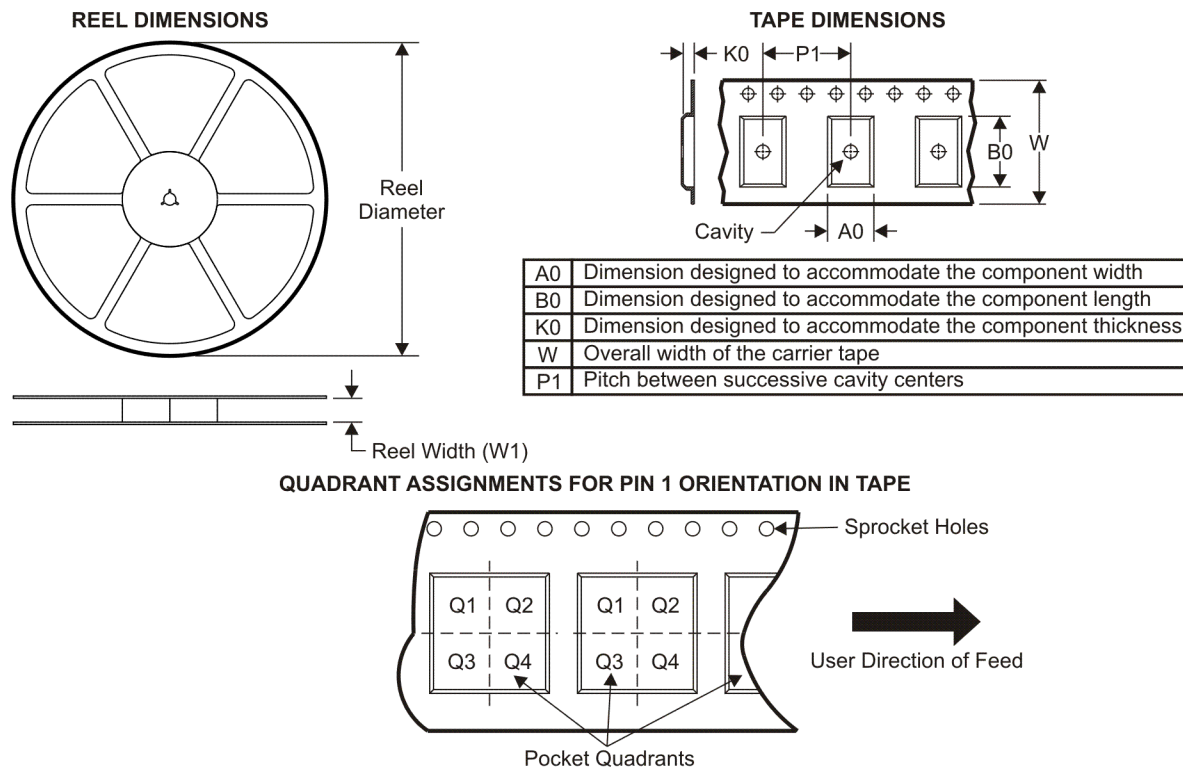
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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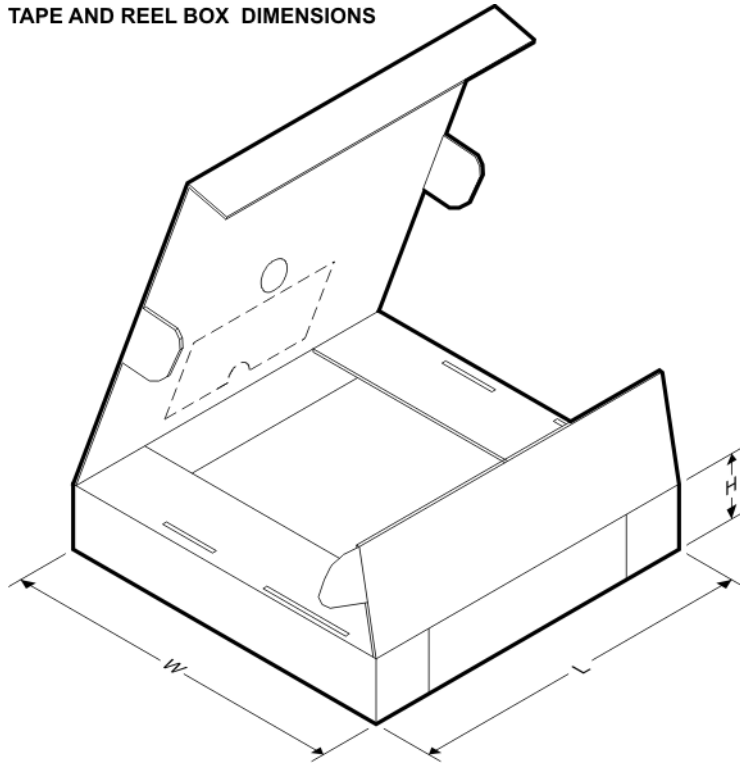
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C198DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

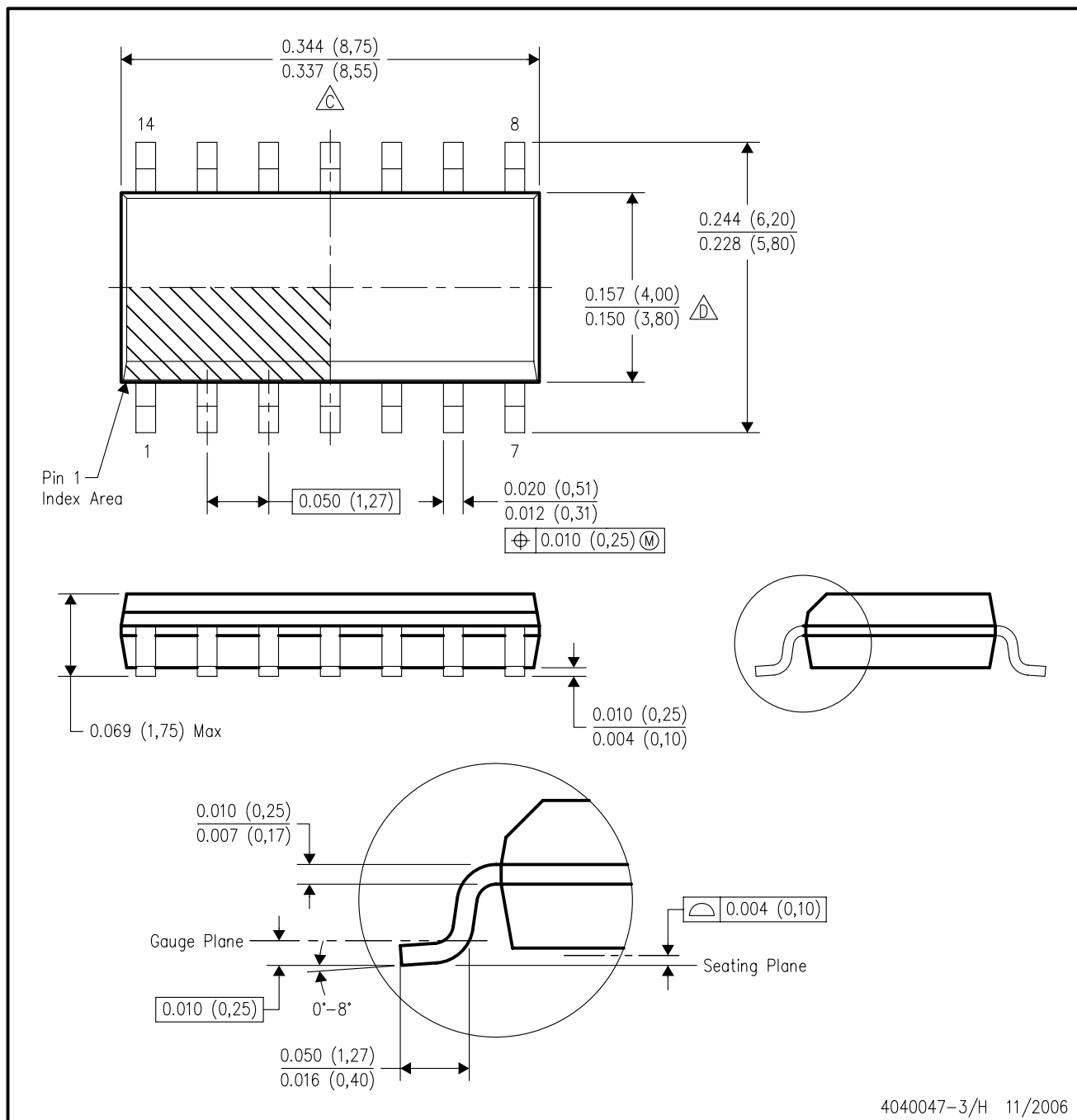


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C198DR	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/H 11/2006

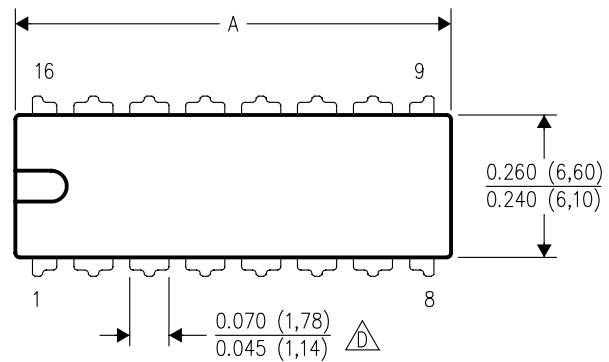
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

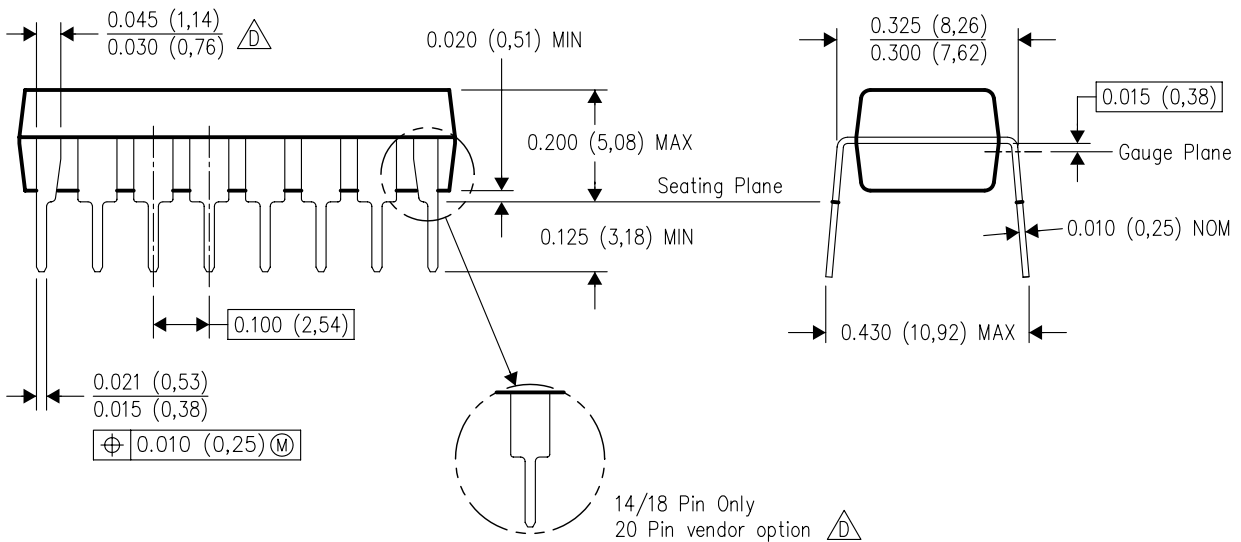
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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