



**SPI100N03S2-03  
SPP100N03S2-03,SPB100N03S2-03**

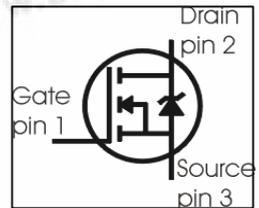
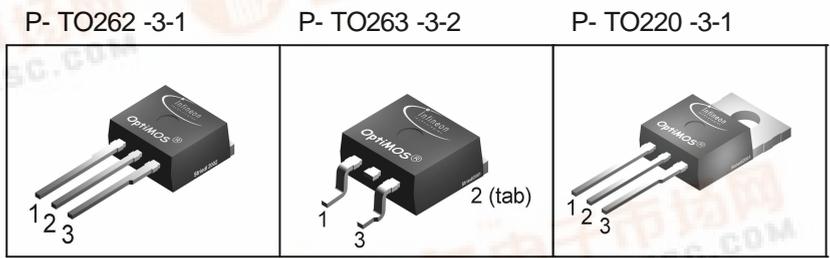
**OptiMOS® Power-Transistor**

**Feature**

- N-Channel
- Enhancement mode
- Excellent Gate Charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- 175°C operating temperature
- Avalanche rated
- $dv/dt$  rated

**Product Summary**

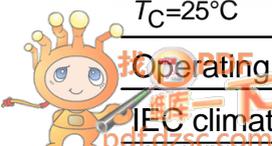
$V_{DS}$	30	V
$R_{DS(on)}$ max. SMD version	3	mΩ
$I_D$	100	A



Type	Package	Ordering Code	Marking
SPP100N03S2-03	P- TO220 -3-1	Q67042-S4058	PN0303
SPB100N03S2-03	P- TO263 -3-2	Q67042-S4057	PN0303
SPI100N03S2-03	P- TO262 -3-1	Q67042-S4116	PN0303

**Maximum Ratings, at  $T_j = 25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Value	Unit
Continuous drain current <sup>1)</sup> $T_C=25\text{ °C}$	$I_D$	100 100	A
Pulsed drain current $T_C=25\text{ °C}$	$I_{D\text{ puls}}$	400	
Avalanche energy, single pulse $I_D=80\text{ A}, V_{DD}=25\text{ V}, R_{GS}=25\text{ }\Omega$	$E_{AS}$	810	mJ
Repetitive avalanche energy, limited by $T_{jmax}^{2)}$	$E_{AR}$	30	
Reverse diode $dv/dt$ $I_S=100\text{ A}, V_{DS}=24\text{ V}, di/dt=200\text{ A}/\mu\text{s}, T_{jmax}=175\text{ °C}$	$dv/dt$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$	$\pm 20$	V
Power dissipation $T_C=25\text{ °C}$	$P_{tot}$	300	W
Operating and storage temperature	$T_j, T_{stg}$	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	



### Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	0.3	0.5	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	62 40	

### Electrical Characteristics, at $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	30	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 250\mu A$	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current $V_{DS}=30V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=30V, V_{GS}=0V, T_j=125^\circ C$	$I_{DSS}$	-	0.01 1	1 100	$\mu A$
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	1	100	
Drain-source on-state resistance $V_{GS}=10V, I_D=80A$ $V_{GS}=10V, I_D=80A, \text{SMD version}$	$R_{DS(on)}$	-	2.5 2.2	3.3 3	$m\Omega$

<sup>1</sup>Current limited by bondwire ; with an  $R_{thJC} = 0.5K/W$  the chip is able to carry  $I_D= 233A$  at  $25^\circ C$ , for detailed information see app.-note ANPS071E available at [www.infineon.com/optimos](http://www.infineon.com/optimos)

<sup>2</sup>Defined by design. Not subject to production test.

<sup>3</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu m$  thick) copper area for drain connection. PCB is vertical without blown air.

### Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Dynamic Characteristics

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 100A$	71	142	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 25V,$ $f = 1MHz$	-	5300	7020	pF
Output capacitance	$C_{oss}$		-	2450	3200	
Reverse transfer capacitance	$C_{rss}$		-	470	700	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 100A,$ $R_G = 2.2\Omega$	-	24	36	ns
Rise time	$t_r$		-	40	60	
Turn-off delay time	$t_{d(off)}$		-	44	66	
Fall time	$t_f$		-	39	59	

### Gate Charge Characteristics

Gate to source charge	$Q_{gs}$	$V_{DD} = 24V, I_D = 100A$	-	26	34	nC
Gate to drain charge	$Q_{gd}$		-	45	68	
Gate charge total	$Q_g$	$V_{DD} = 24V, I_D = 100A,$ $V_{GS} = 0 \text{ to } 10V$	-	113	150	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 24V, I_D = 100A$	-	5.6	-	V

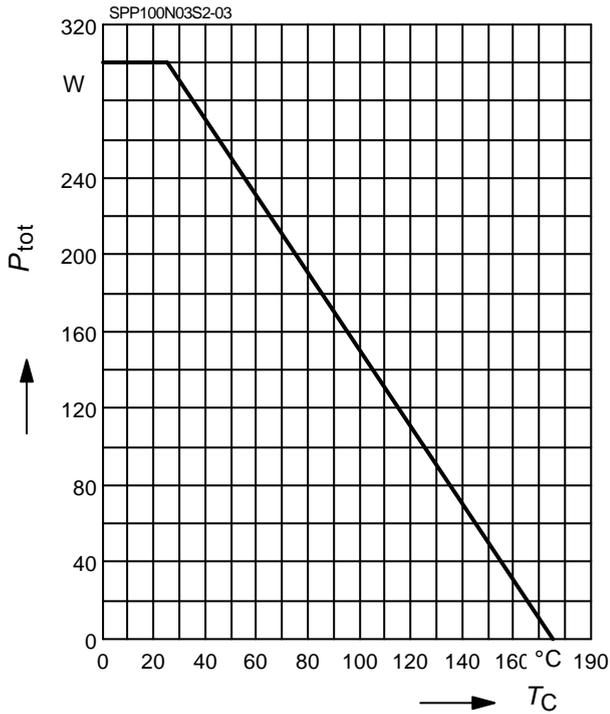
### Reverse Diode

Inverse diode continuous forward current	$I_S$	$T_C = 25^\circ C$	-	-	100	A
Inv. diode direct current, pulsed	$I_{SM}$		-	-	400	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0V, I_F = 100A$	-	0.9	1.3	V
Reverse recovery time	$t_{rr}$	$V_R = 15V, I_F = I_S,$ $di_F/dt = 100A/\mu s$	-	79	100	ns
Reverse recovery charge	$Q_{rr}$		-	109	136	nC

### 1 Power dissipation

$$P_{tot} = f(T_C)$$

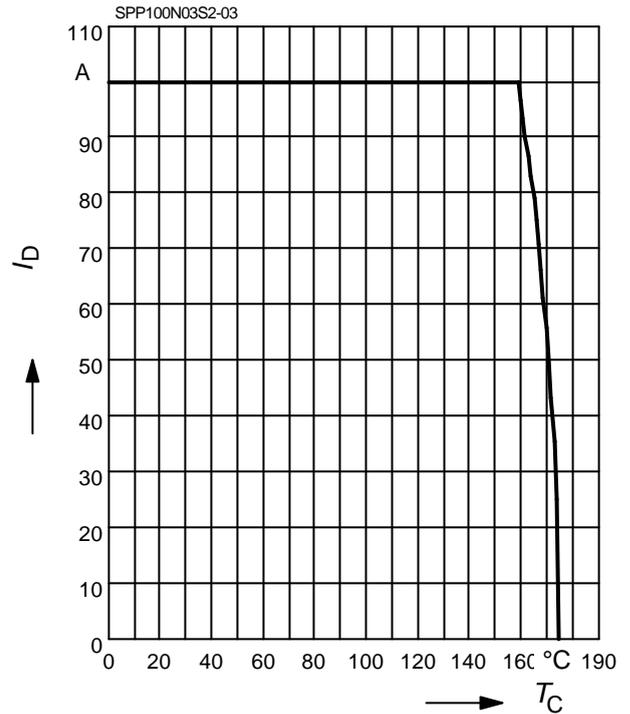
parameter:  $V_{GS} \geq 6 \text{ V}$



### 2 Drain current

$$I_D = f(T_C)$$

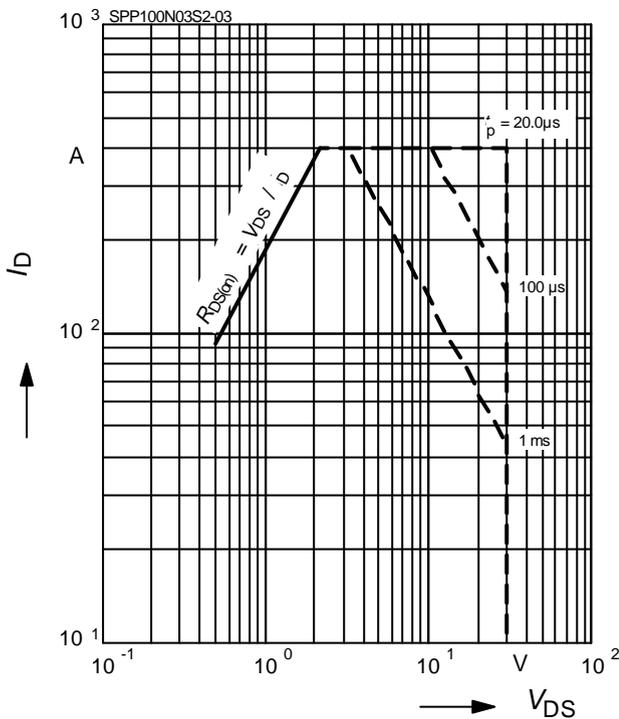
parameter:  $V_{GS} \geq 10 \text{ V}$



### 3 Safe operating area

$$I_D = f(V_{DS})$$

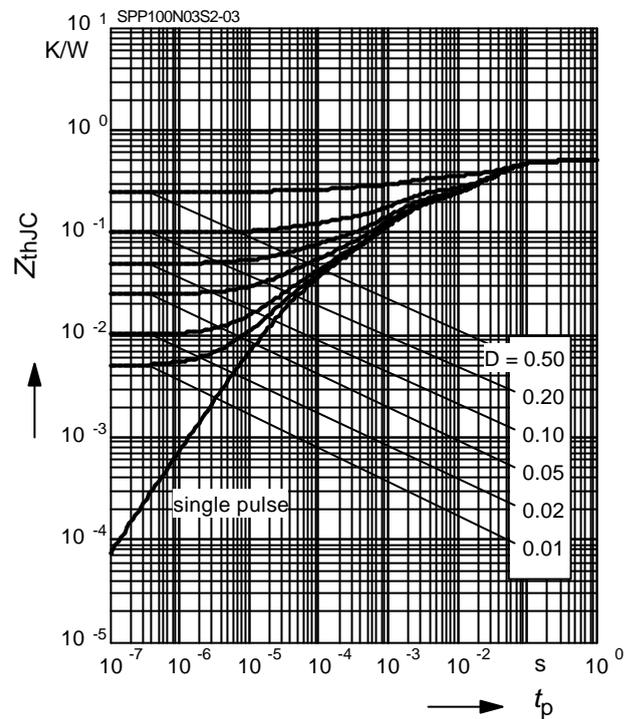
parameter:  $D = 0$ ,  $T_C = 25 \text{ °C}$



### 4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

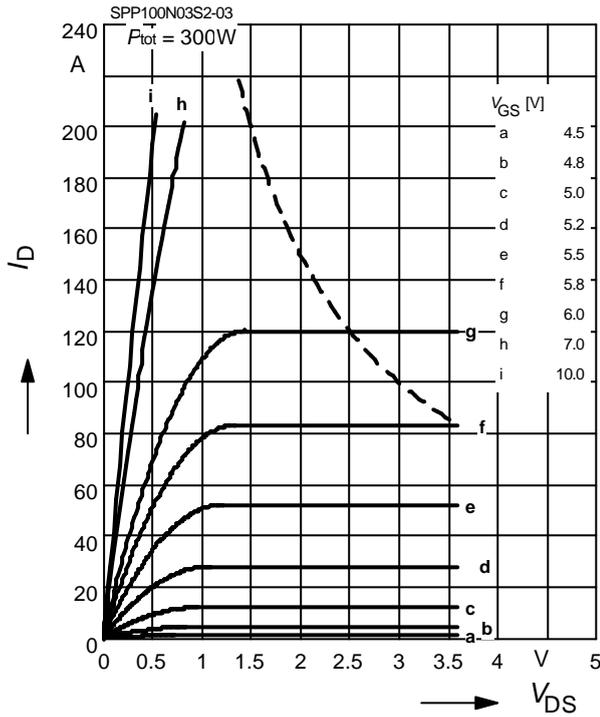
parameter:  $D = t_p/T$



### 5 Typ. output characteristic

$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

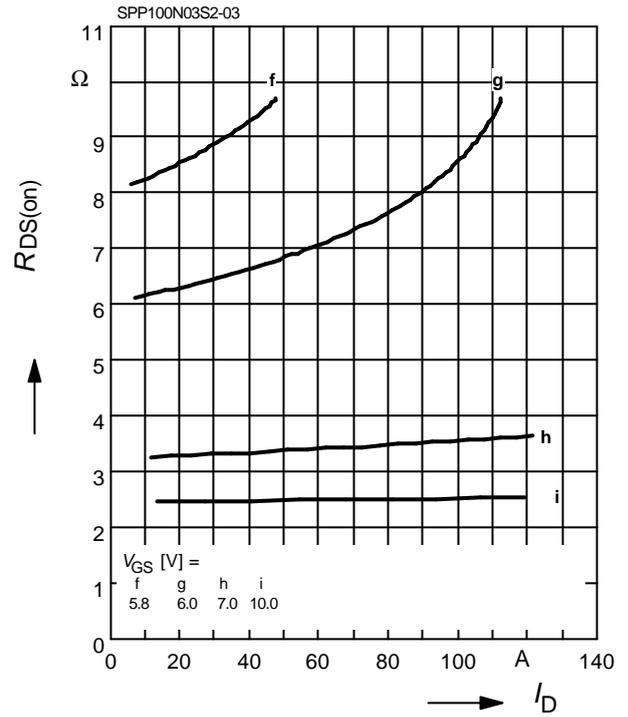
parameter:  $t_p = 80 \mu\text{s}$



### 6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

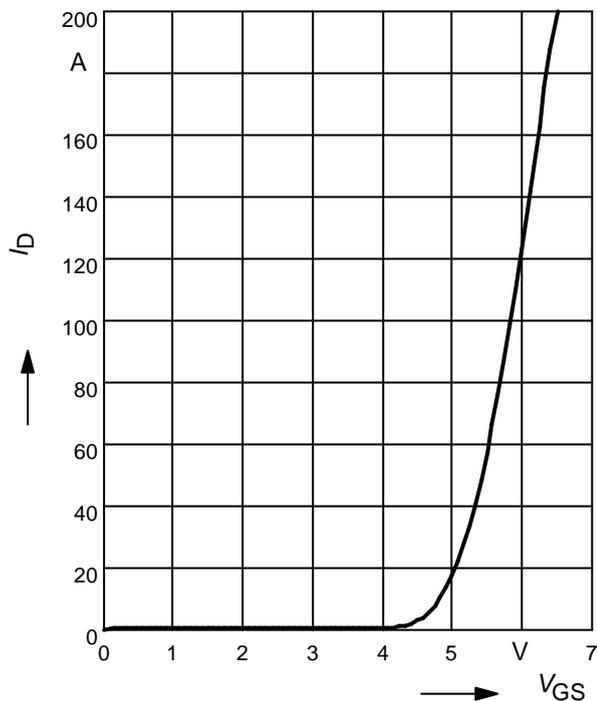
parameter:  $V_{GS}$



### 7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

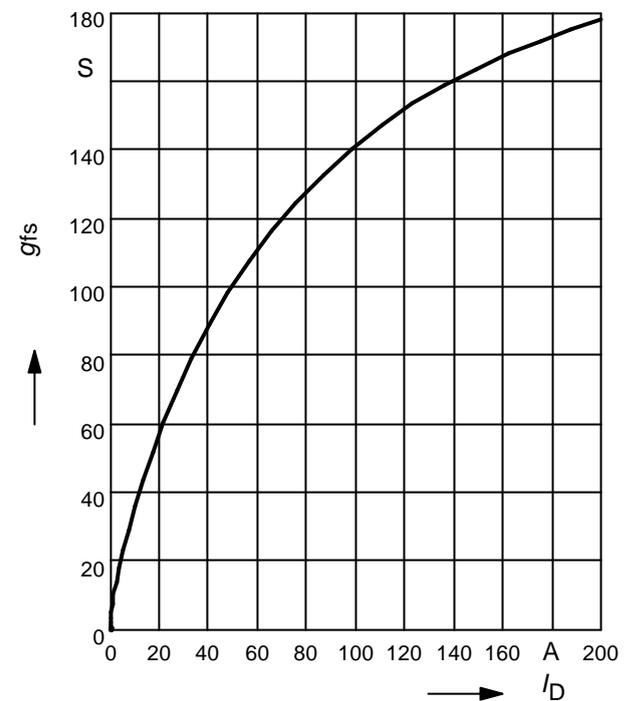
parameter:  $t_p = 80 \mu\text{s}$



### 8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_J = 25^\circ\text{C}$$

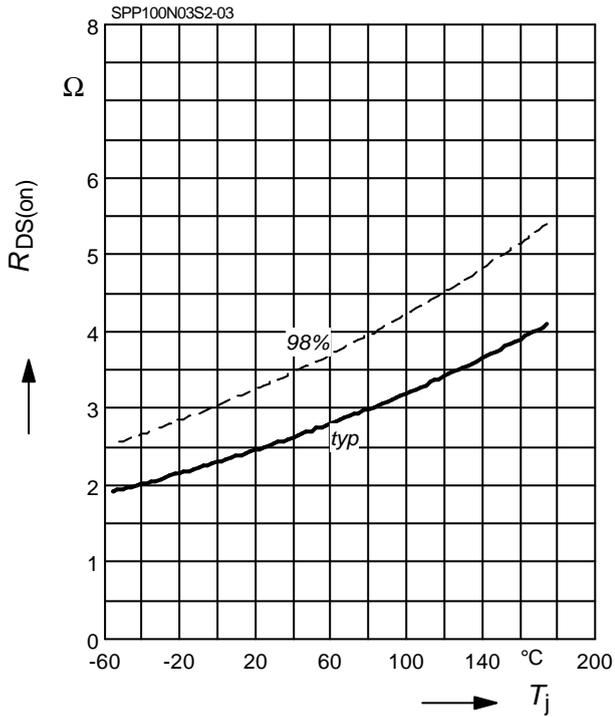
parameter:  $g_{fs}$



### 9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

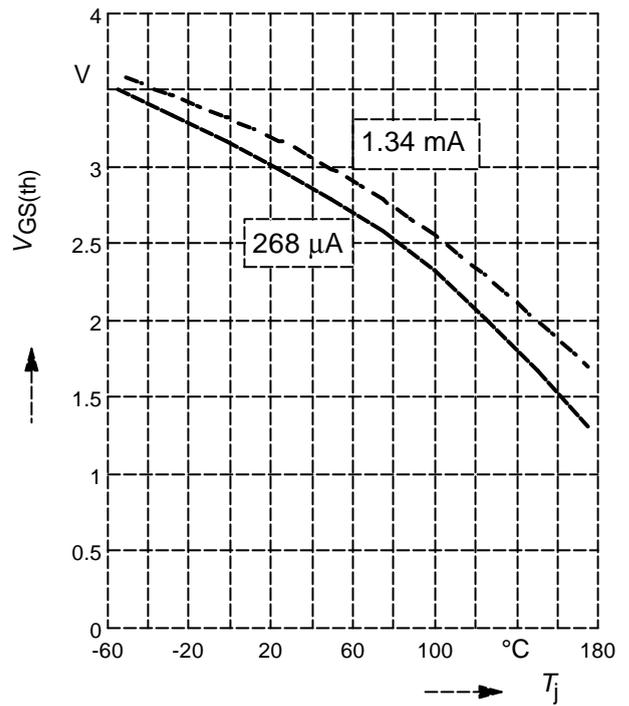
parameter:  $I_D = 80\text{ A}$ ,  $V_{GS} = 10\text{ V}$



### 10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

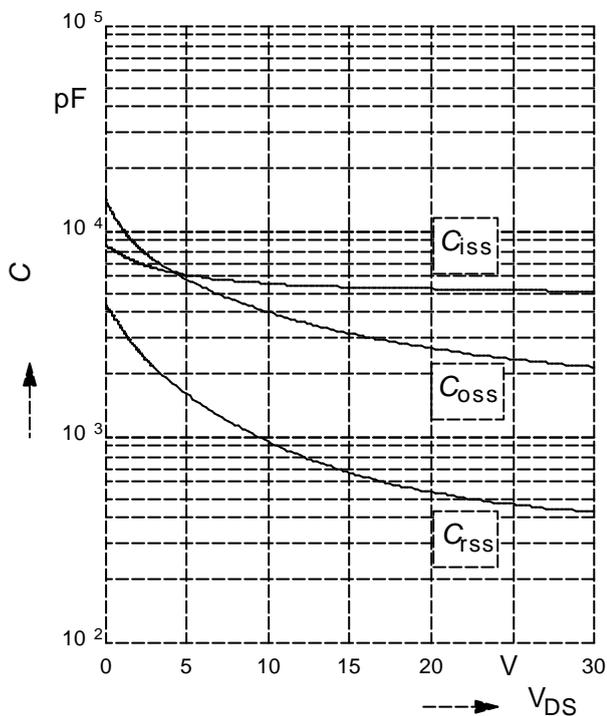
parameter:  $V_{GS} = V_{DS}$



### 11 Typ. capacitances

$$C = f(V_{DS})$$

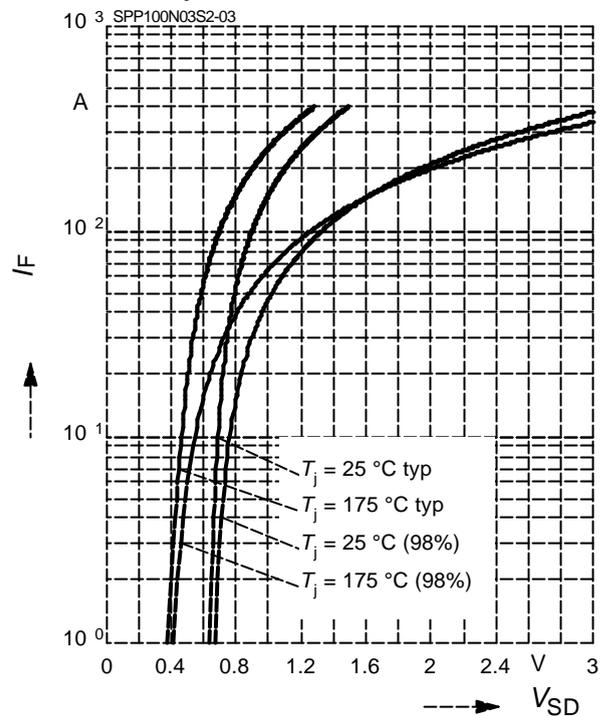
parameter:  $V_{GS} = 0\text{ V}$ ,  $f = 1\text{ MHz}$



### 12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

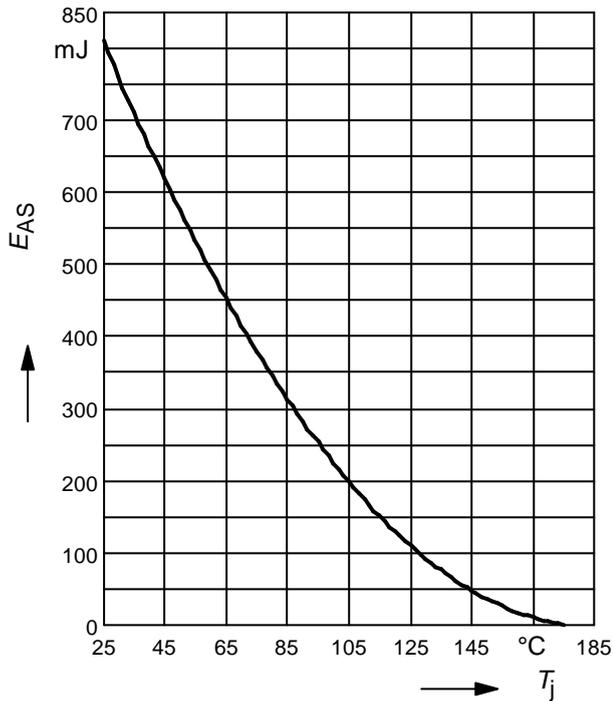
parameter:  $T_j$ ,  $t_p = 80\text{ }\mu\text{s}$



### 13 Typ. avalanche energy

$$E_{AS} = f(T_j)$$

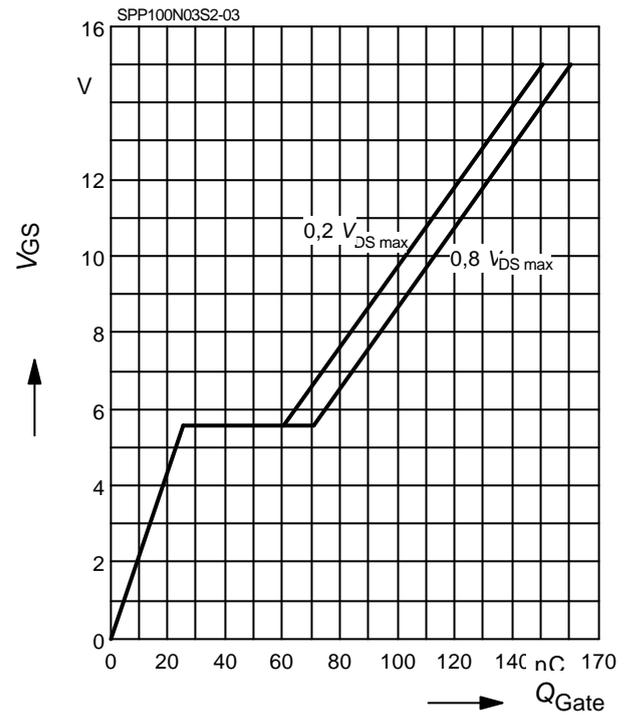
par.:  $I_D = 80 \text{ A}$ ,  $V_{DD} = 25 \text{ V}$ ,  $R_{GS} = 25 \Omega$



### 14 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

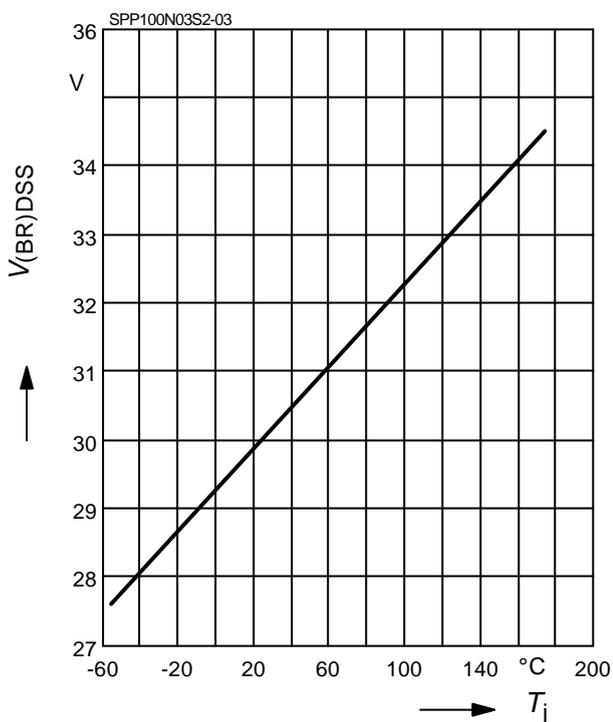
parameter:  $I_D = 100 \text{ A}$  pulsed



### 15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

parameter:  $I_D = 10 \text{ mA}$





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**Further information**

Please notice that the part number is BSPP100N03S2-03, BSPB100N03S2-03 and BSPI100N03S2-03, for simplicity the device is referred to by the term SPP100N03S2-03, SPB100N03S2-03 and SPI100N03S2-03 throughout this documentation