

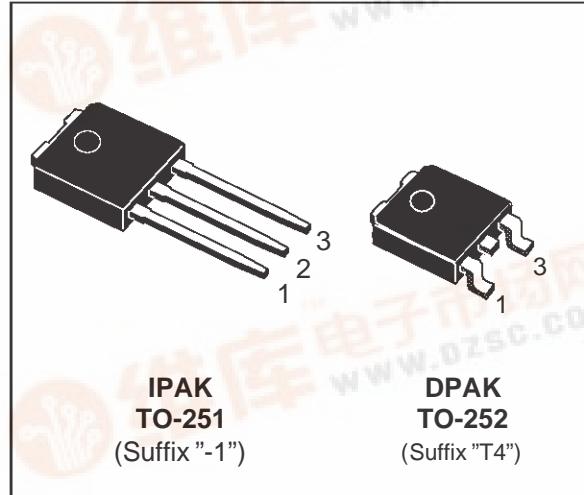


# STD5N20

## N - CHANNEL 200V - 0.7Ω - 5A - TO-251/TO-252 POWER MOS TRANSISTOR

TYPE	V <sub>DSS</sub>	R <sub>D(on)</sub>	I <sub>D</sub>
STD5N20	200 V	< 0.8 Ω	5 A

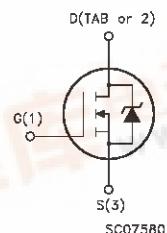
- TYPICAL R<sub>D(on)</sub> = 0.7 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 150°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")



### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- DC-DC CONVERTERS & DC-AC INVERTERS
- TELECOMMUNICATION POWER SUPPLIES
- INDUSTRIAL MOTOR DRIVES

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	200	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	200	V
V <sub>GS</sub>	Gate-source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	3.5	A
I <sub>DM(•)</sub>	Drain Current (pulsed)	20	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	45	W
	Derating Factor	0.36	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

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### THERMAL DATA

R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	2.77	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	100	°C/W
R <sub>thc-sink</sub>	Thermal Resistance Case-sink	Typ	1.5	°C/W
T <sub>L</sub>	Maximum Lead Temperature For Soldering Purpose		275	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max.)	5	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	130	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	200			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>D(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 2.5 A		0.7	0.8	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>D(on)max</sub> V <sub>GS</sub> = 10 V	5			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>D(on)max</sub> I <sub>D</sub> = 2.5 A	1.5	3		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0		450 75 15	600 100 20	pF pF pF

**ELECTRICAL CHARACTERISTICS (continued)****SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Time Rise Time	$V_{DD} = 100 \text{ V}$ $I_D = 2.5 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 3)		7 6	10 8	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 160 \text{ V}$ $I_D = 5 \text{ A}$ $R_G = 47 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 5)		400		$\text{A}/\mu\text{s}$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160 \text{ V}$ $I_D = 5 \text{ A}$ $V_{GS} = 10 \text{ V}$		18 6 7	25	nC nC nC

**SWITCHING OFF**

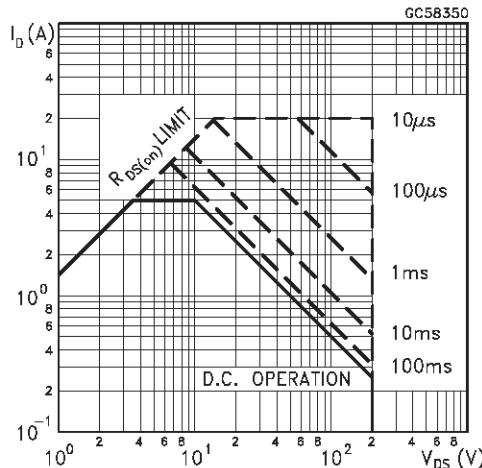
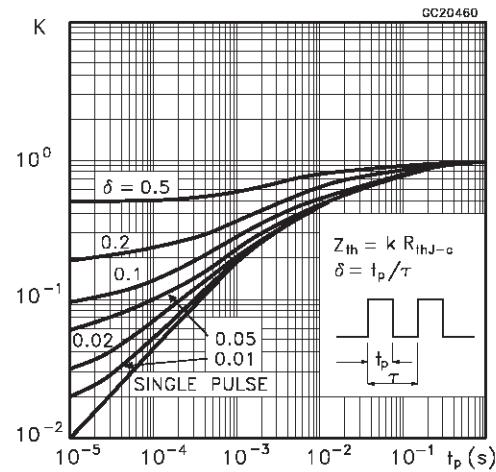
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 160 \text{ V}$ $I_D = 5 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 5)		7 5 15	10 7 20	ns ns ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				5 20	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 5 \text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ $T_j = 150 \text{ }^\circ\text{C}$ (see test circuit, figure 5)		180 1125 12.5		ns nC A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

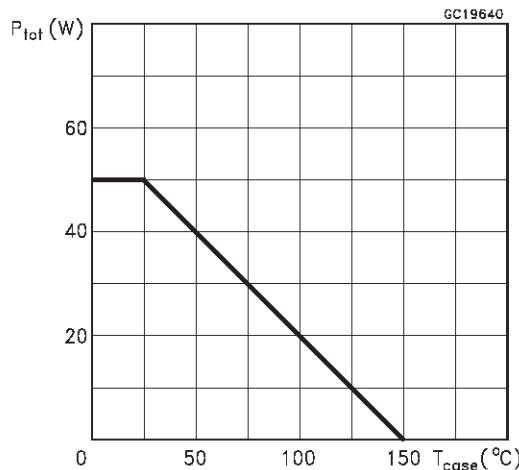
(•) Pulse width limited by safe operating area

**Safe Operating Area****Thermal Impedance**

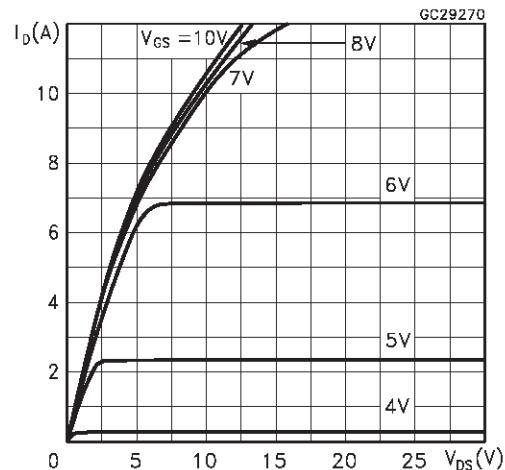
## STD5N20

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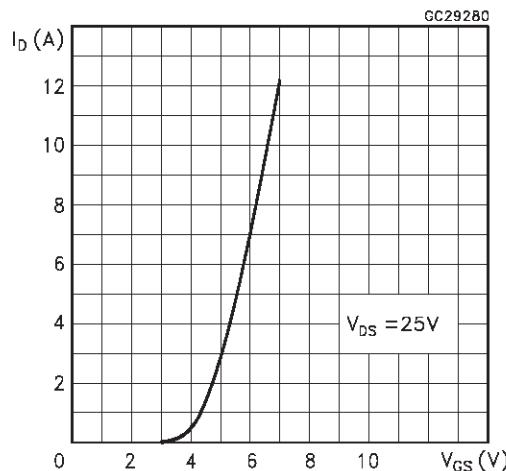
Derating Curve



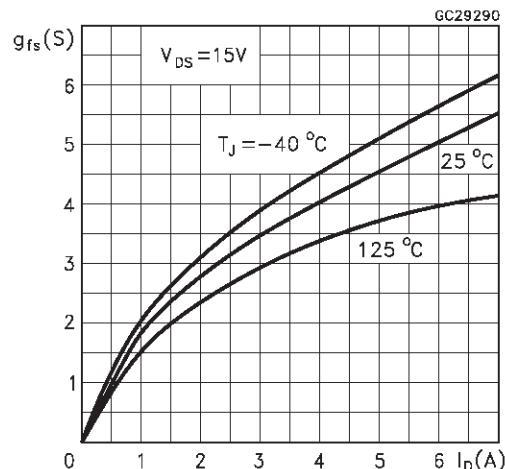
Output Characteristics



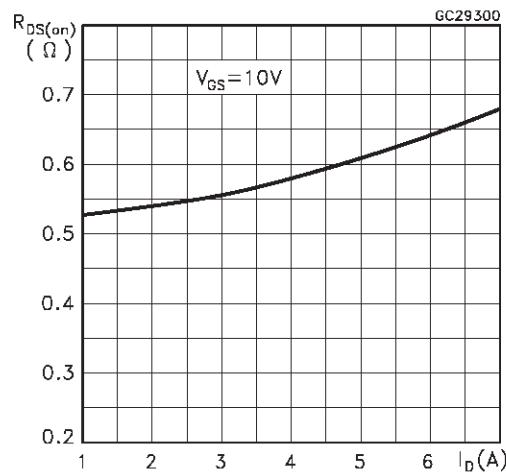
Transfer Characteristics



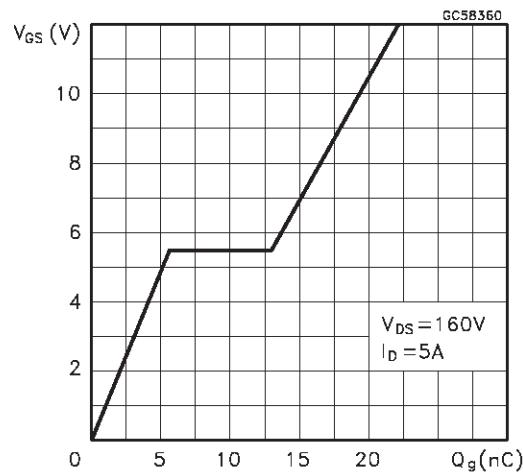
Transconductance



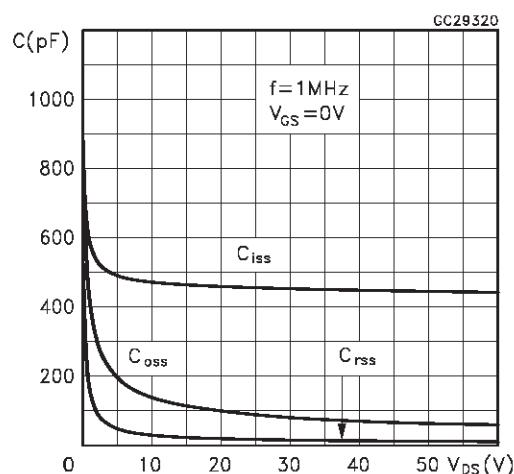
Static Drain-source On Resistance



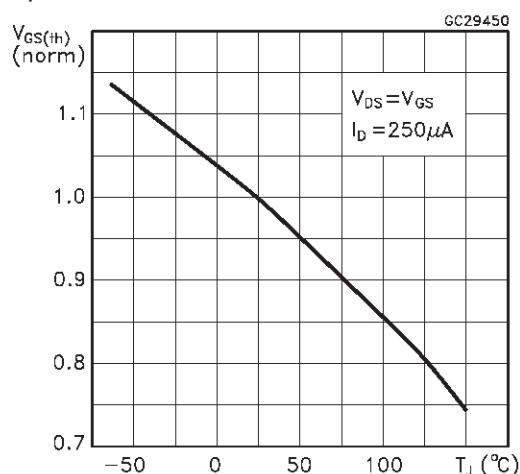
Gate Charge vs Gate-source Voltage



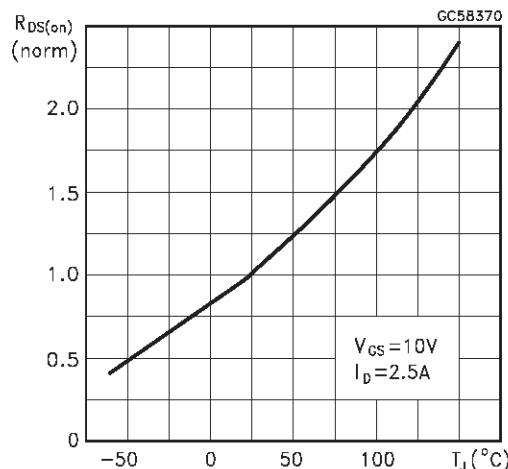
Capacitance Variations



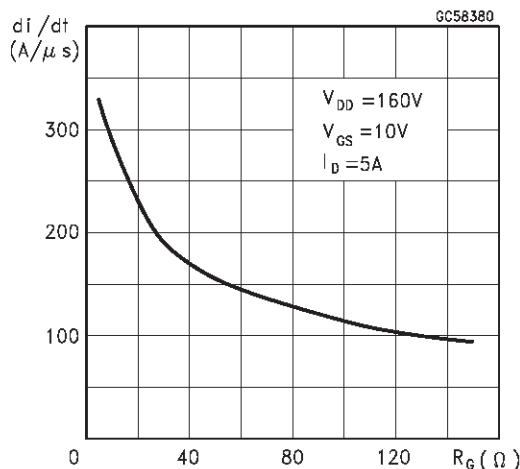
Normalized Gate Threshold Voltage vs Temperature



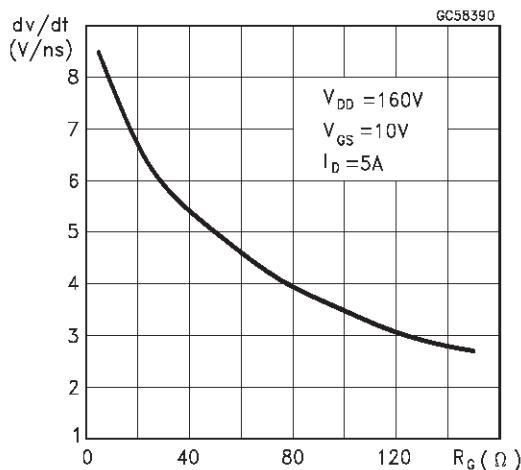
Normalized On Resistance vs Temperature



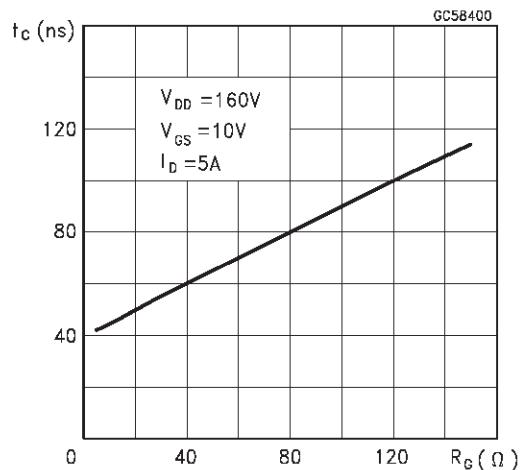
Turn-on Current Slope



Turn-off Drain-source Voltage Slope

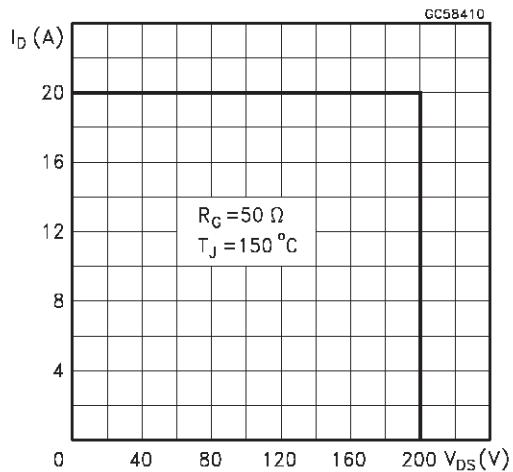


Cross-over Time

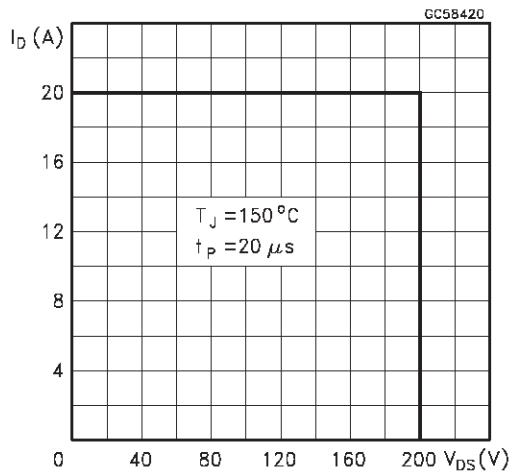


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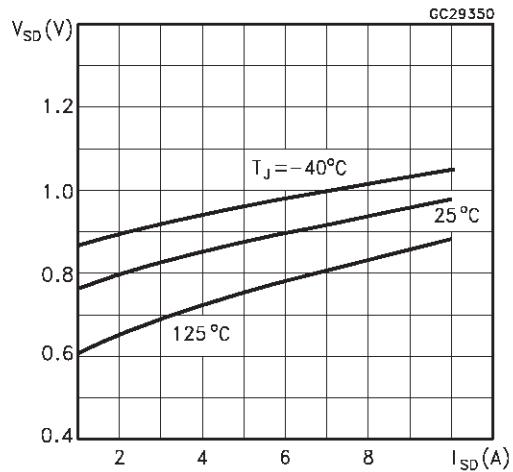
### Switching Safe Operating Area



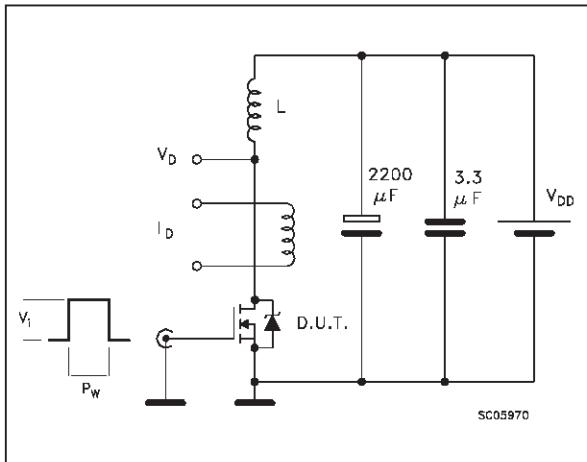
### Accidental Overload Area



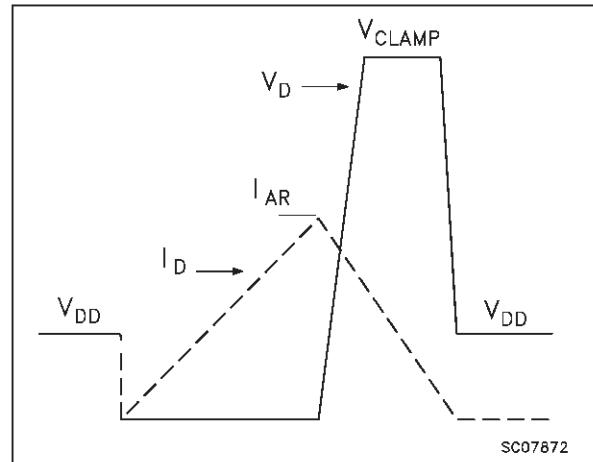
### Source-drain Diode Forward Characteristics



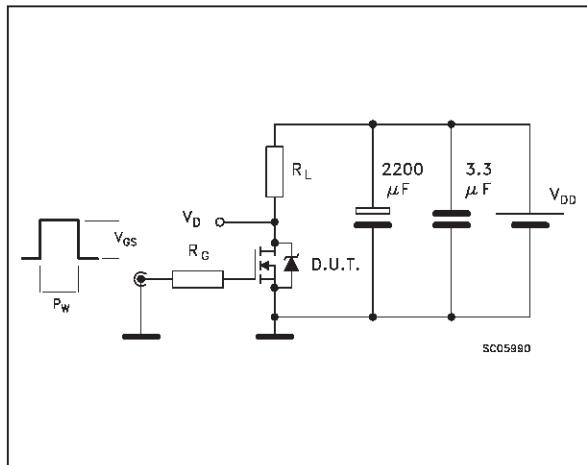
**Fig. 1:** Unclamped Inductive Load Test Circuit



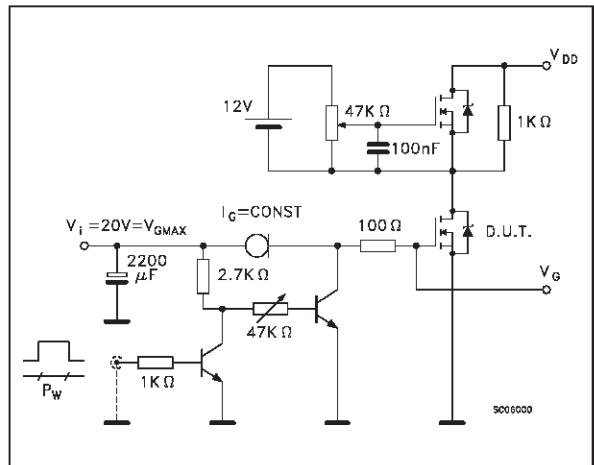
**Fig. 2:** Unclamped Inductive Waveform



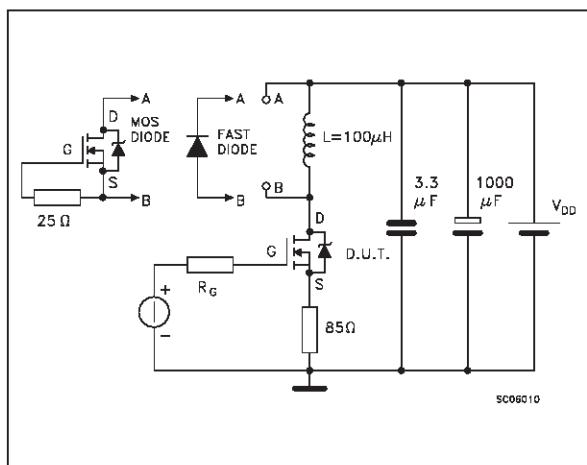
**Fig. 3:** Switching Times Test Circuits For Resistive Load



**Fig. 4:** Gate Charge test Circuit

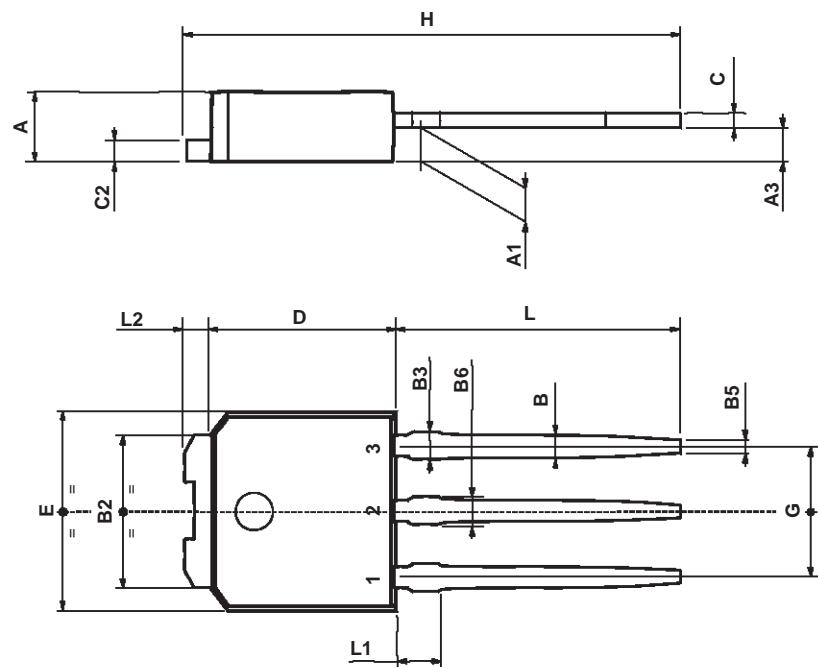


**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



**STD5N20****TO-251 (IPAK) MECHANICAL DATA**

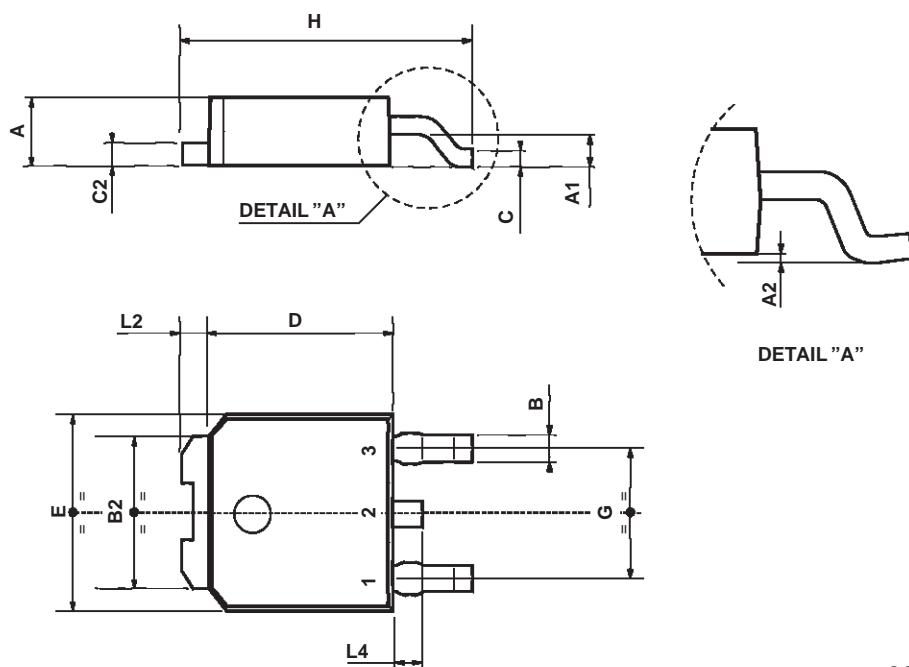
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



0068772-B

## **STD5N20**

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