



# STS3C2F100

N-CHANNEL 100V - 0.110 Ω - 3A SO-8  
 P-CHANNEL 100V - 0.320 Ω - 1.5A SO-8  
 COMPLEMENTARY PAIR STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS3C2F100(N-Channel)	100 V	< 0.145Ω	3.0 A
STS3C2F100(P-Channel)	100 V	< 0.380Ω	1.5 A

- TYPICAL R<sub>DS(on)</sub> (N-Channel) = 0.110 Ω
- TYPICAL R<sub>DS(on)</sub> (P-Channel) = 0.320 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- ULTRA LOW GATE CHARGE
- ULTRA LOW ON-RESISTANCE

### DESCRIPTION

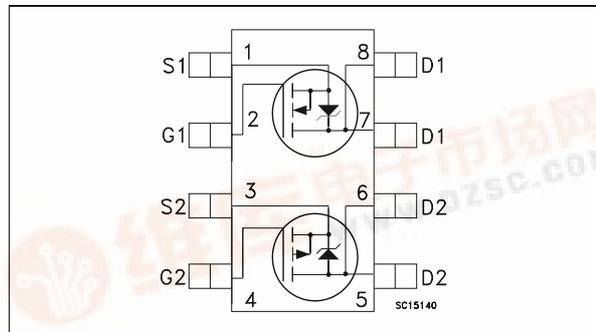
This MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- DC MOTOR DRIVES
- AUDIO AMPLIFIER



### INTERNAL SCHEMATIC DIAGRAM



### Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS3C2F100	S3C2F100	SO-8	TAPE & REEL

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	100		V
V <sub>GS</sub>	Gate- source Voltage	± 20		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	3.0	1.5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	1.9	1.0	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	12	6	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2		W
T <sub>stg</sub>	Storage Temperature	-55 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed



## STS3C2F100

**TAB.1 THERMAL DATA**

Rthj-amb(1)	Thermal Resistance Junction-ambient	62.5	°C/W
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(1) when mounted on 1 in<sup>2</sup> pad of 2 oz. copper, t ≤ 10sec.

## ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25 °C unless otherwise specified)

**TAB.2 OFF**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	n-ch p-ch	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C	n-ch p-ch			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V	n-ch p-ch			±100	nA

**TAB.3 ON**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	n-ch p-ch	2 2			V V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.5 A V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.0 A	n-ch p-ch		0.110 0.320	0.145 0.380	Ω Ω

**TAB.4 DYNAMIC**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 20 V I <sub>D</sub> = 1.5 A V <sub>DS</sub> = 30 V I <sub>D</sub> = 1.0 A	n-ch p-ch		3 4		S S
C <sub>iss</sub>	Input Capacitance		n-ch p-ch		460 705		pF pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0	n-ch p-ch		70 83		pF pF
C <sub>rss</sub>	Reverse Transfer Capacitance		n-ch p-ch		30 30		pF pF

**ELECTRICAL CHARACTERISTICS** (continued)

**TAB.5 SWITCHING ON**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	<b>N-CHANNEL</b> $V_{DD} = 50\text{ V}$ $I_D = 1.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$	n-ch p-ch		16 14		ns ns
$t_r$	Rise Time	<b>P-CHANNEL</b> $V_{DD} = 50\text{ V}$ $I_D = 1.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)	n-ch p-ch		25 20		ns ns
$Q_g$	Total Gate Charge	<b>N-CHANNEL</b> $V_{DD}=80\text{V}$ $I_D=3\text{A}$ $V_{GS}=10\text{V}$	n-ch p-ch		15 20	20 27	nC nC
$Q_{gs}$	Gate-Source Charge	<b>P-CHANNEL</b> $V_{DD} = 80\text{V}$ $I_D = 1.5\text{A}$ $V_{GS} = 10\text{V}$ (see test circuit, Figure 2)	n-ch		3.7		nC
$Q_{gd}$	Gate-Drain Charge		p-ch		2.0		nC
			n-ch		4.7		nC
			p-ch		6.0		nC

**TAB.6 SWITCHING OFF**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	<b>N-CHANNEL</b> $V_{DD} = 50\text{ V}$ $I_D = 1.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$	n-ch p-ch		32 33		ns ns
$t_f$	Fall Time	<b>P-CHANNEL</b> $V_{DD} = 50\text{ V}$ $I_D = 1.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)	n-ch p-ch		20 7.5		ns ns

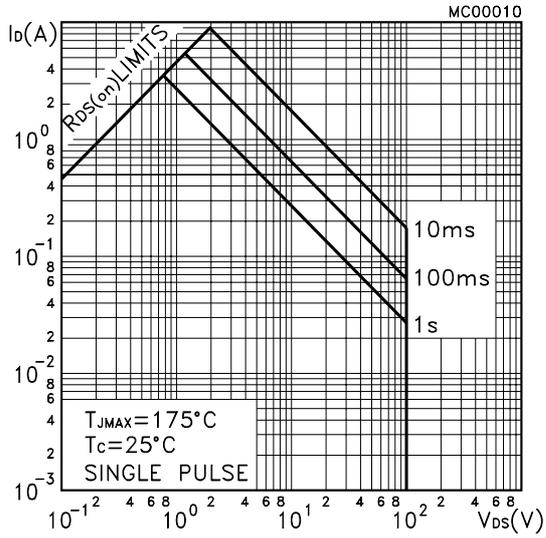
**TAB.7 SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current		n-ch			3.0	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)		p-ch n-ch p-ch			1.5 12 6.0	A A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 3\text{ A}$ $V_{GS} = 0$ $I_{SD} = 1.5\text{ A}$ $V_{GS} = 0$	n-ch p-ch			1.2 1.2	V V
$t_{rr}$	Reverse Recovery Time	<b>N-CHANNEL</b> $I_{SD} = 3\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$	n-ch p-ch		90 65		ns ns
$Q_{rr}$	Reverse Recovery Charge	<b>P-CHANNEL</b> $I_{SD} = 1.5\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 3)	n-ch		230		nC
$I_{RRM}$	Reverse Recovery Current		p-ch		175		nC
			n-ch		5.0		A
			p-ch		5.4		A

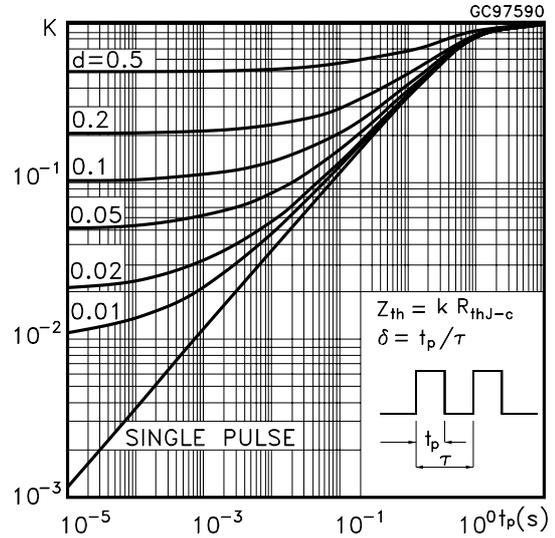
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
 (•) Pulse width limited by safe operating area.

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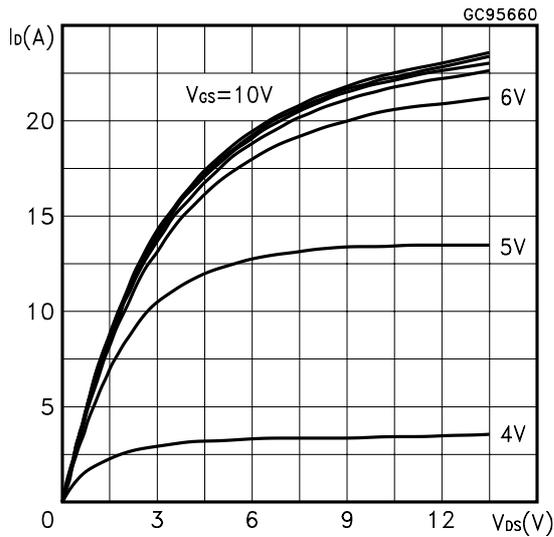
Safe Operating Area **n-ch**



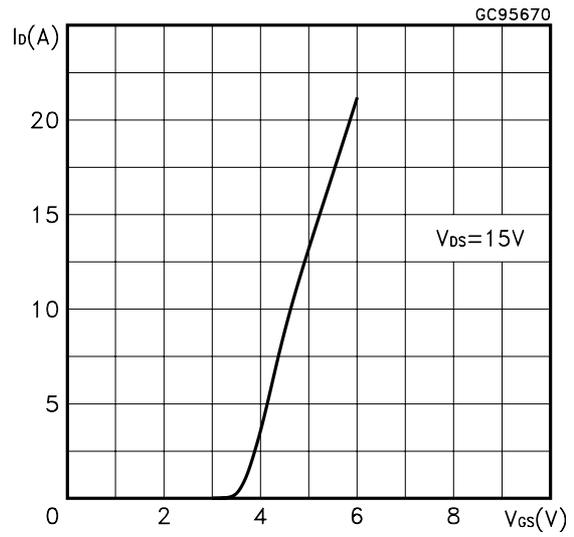
Thermal Impedance **n-ch**



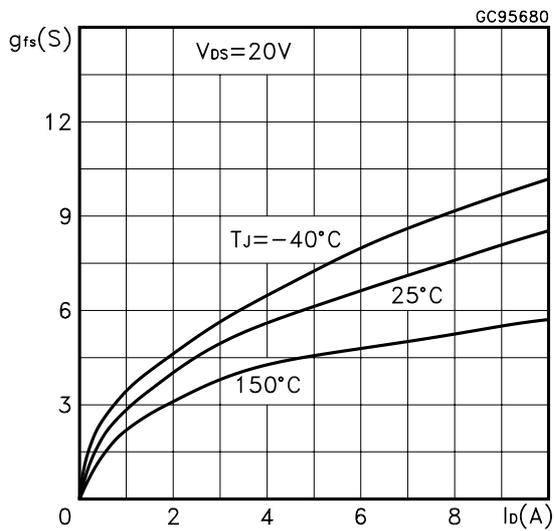
Output Characteristics **n-ch**



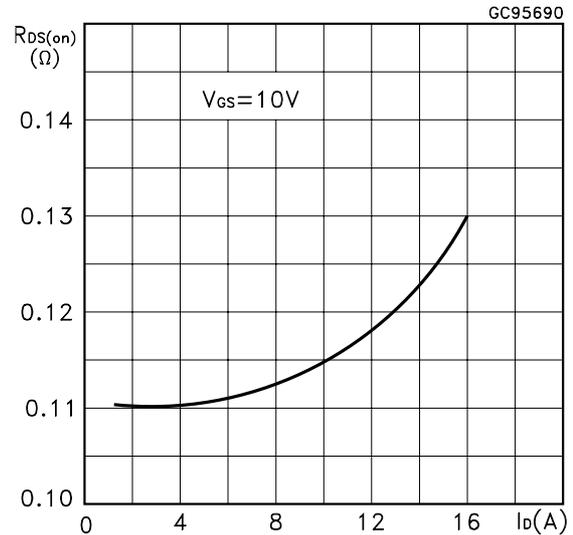
Transfer Characteristics **n-ch**



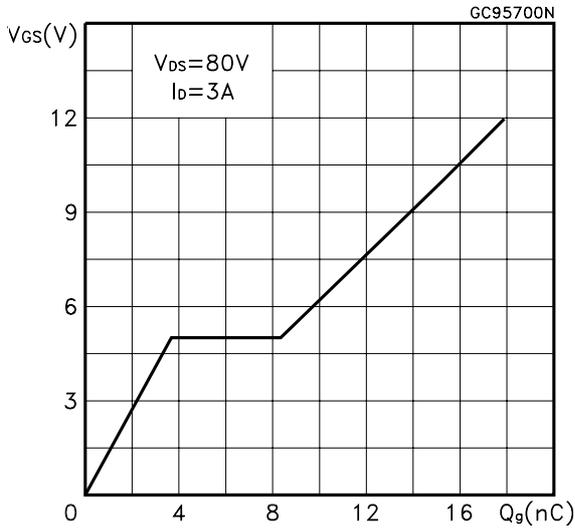
Transconductance **n-ch**



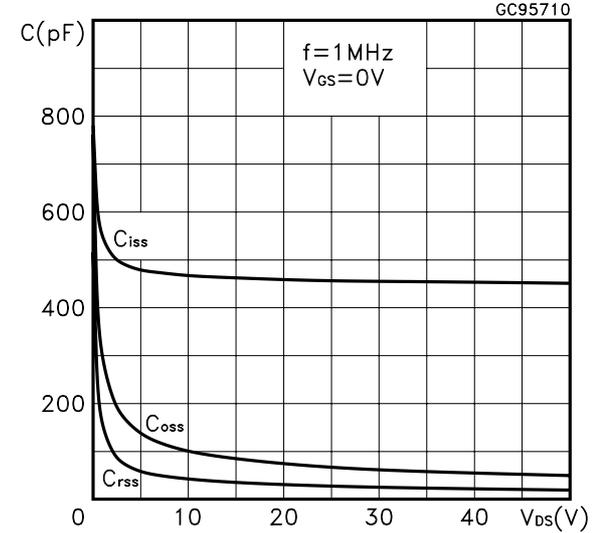
Static Drain-source On Resistance **n-ch**



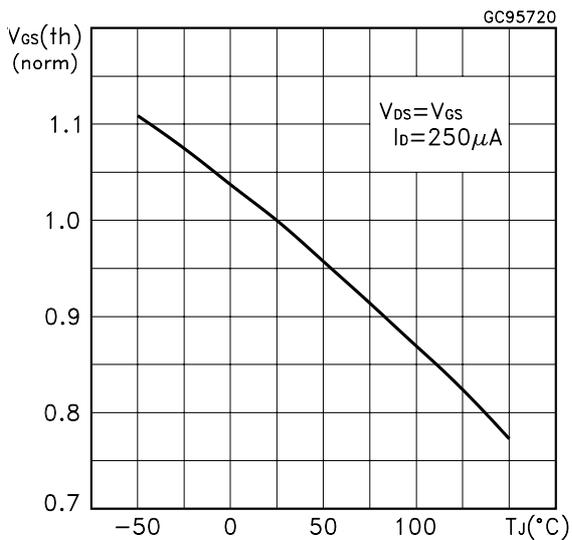
Gate Charge vs Gate-source Voltage **n-ch**



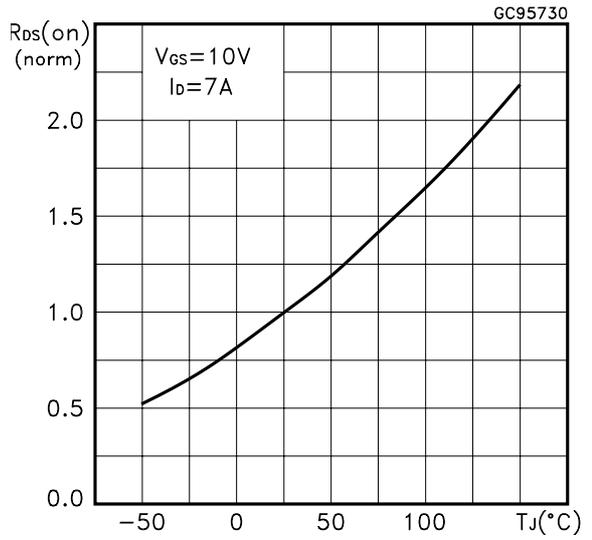
Capacitance Variations **n-ch**



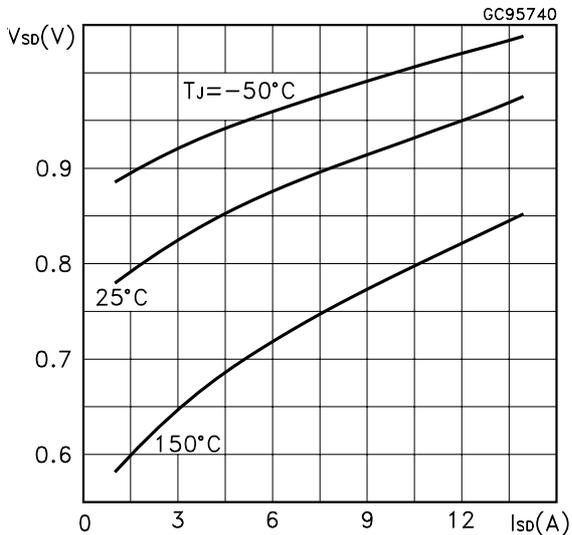
Normalized Gate Threshold Voltage vs Temperature **n-ch**



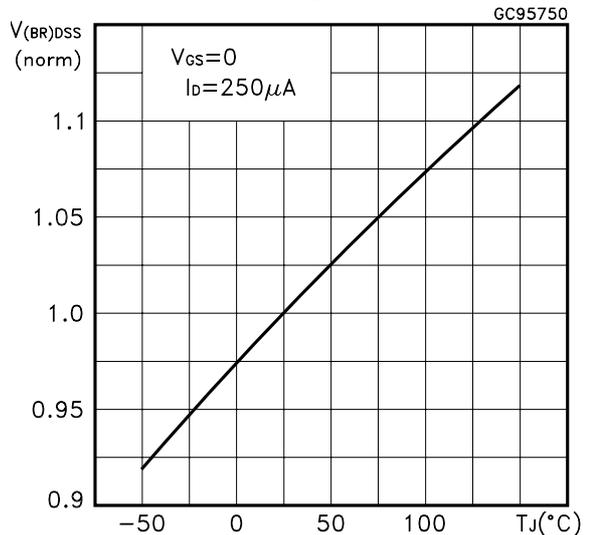
Normalized on Resistance vs Temperature **n-ch**



Source-drain Diode Forward Characteristics **n-ch**

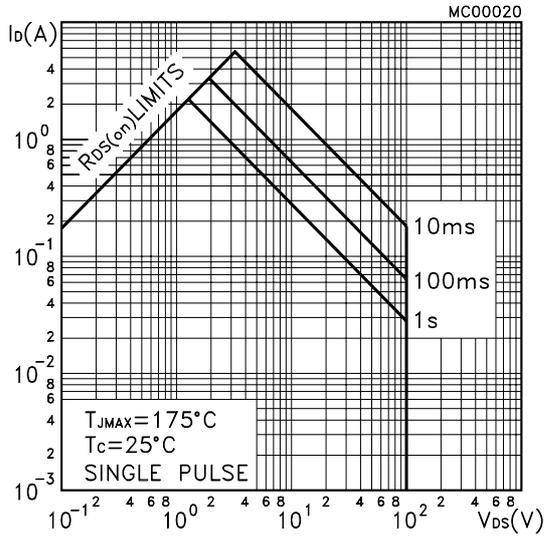


Normalized Breakdown Voltage vs Temperature **n-ch**

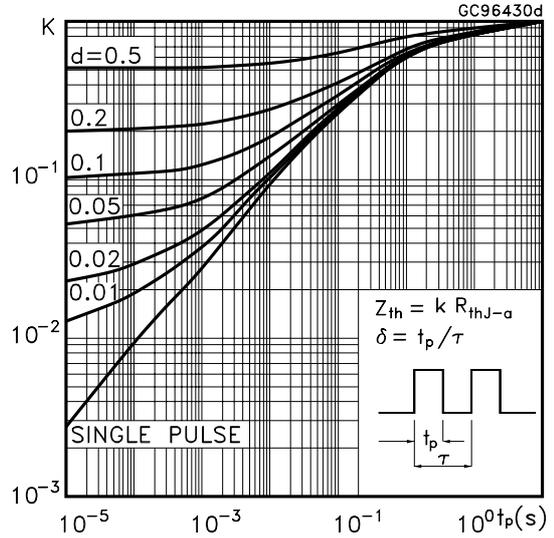


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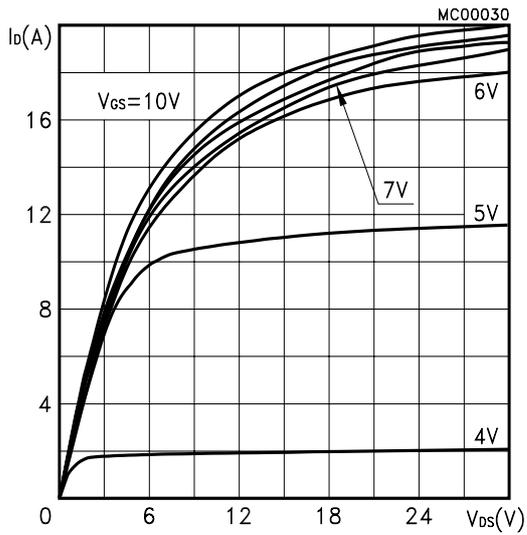
Safe Operating Area **p-ch**



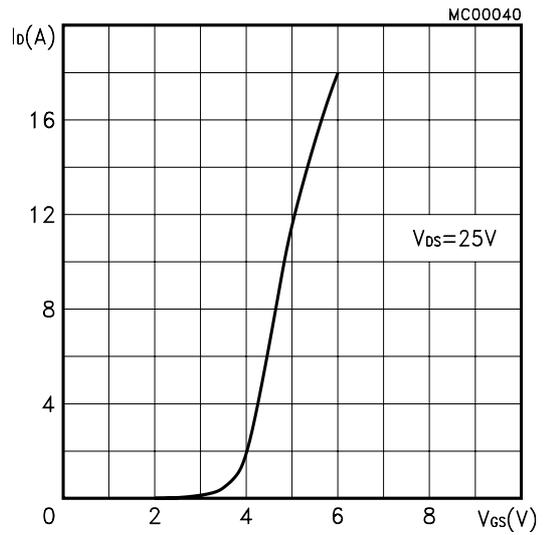
Thermal Impedance **p-ch**



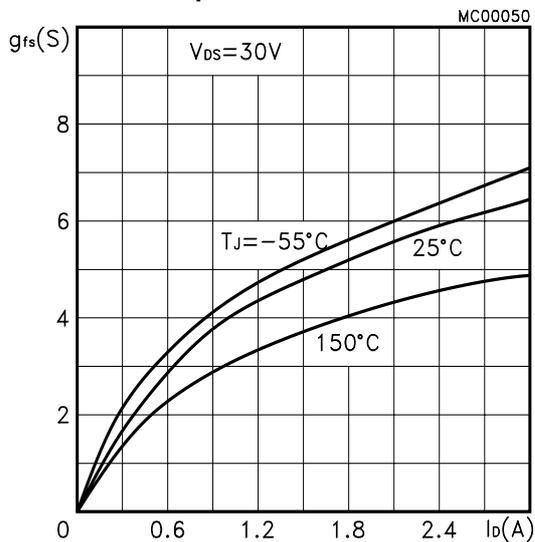
Output Characteristics **p-ch**



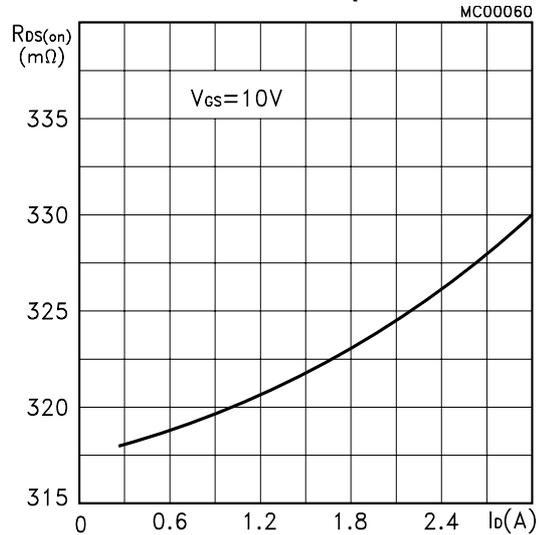
Transfer Characteristics **p-ch**



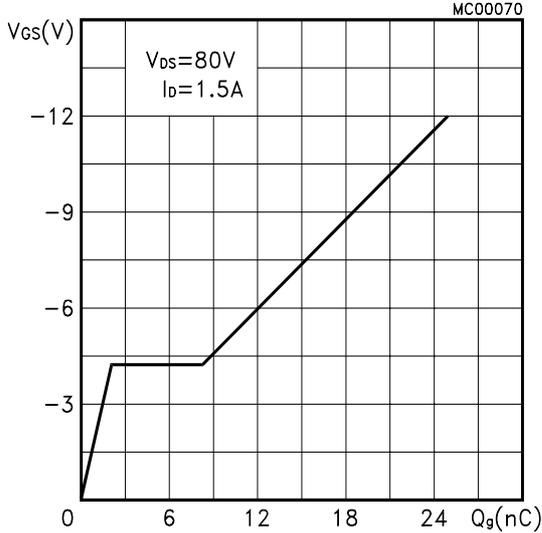
Transconductance **p-ch**



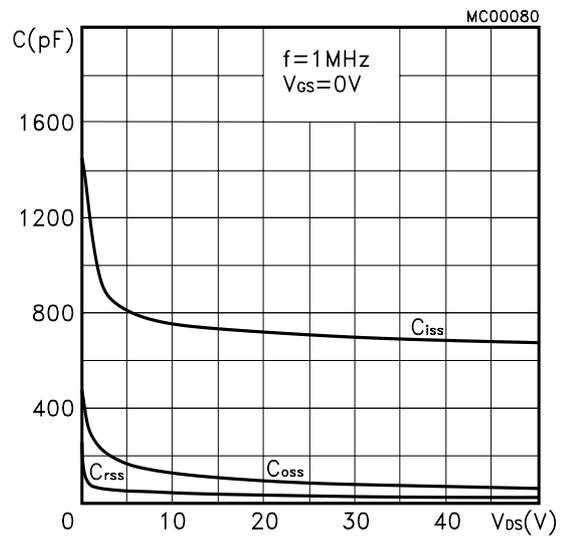
Static Drain-source On Resistance **p-ch**



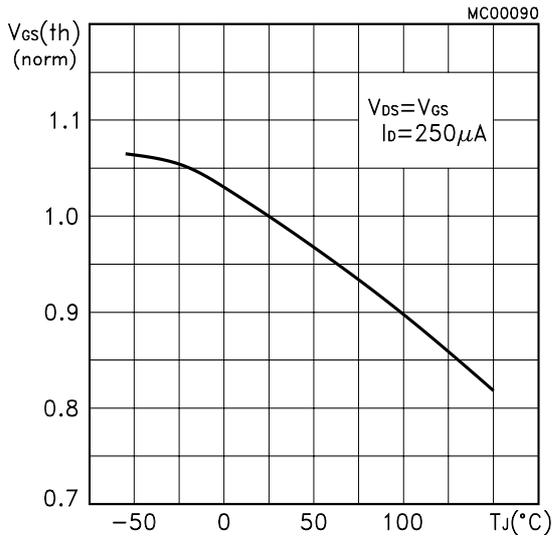
Gate Charge vs Gate-source Voltage **p-ch**



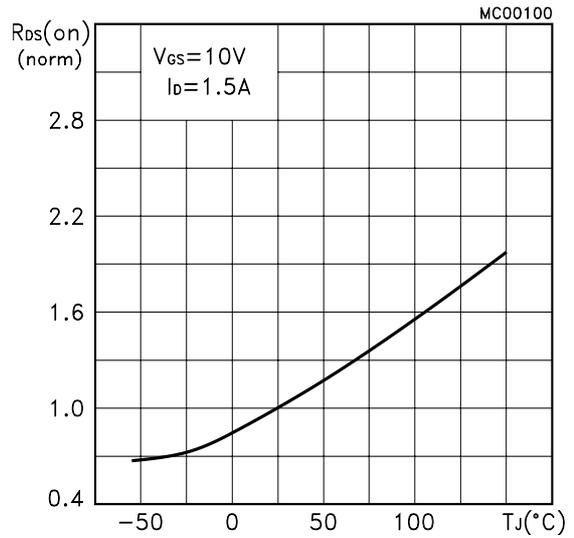
Capacitance Variations **p-ch**



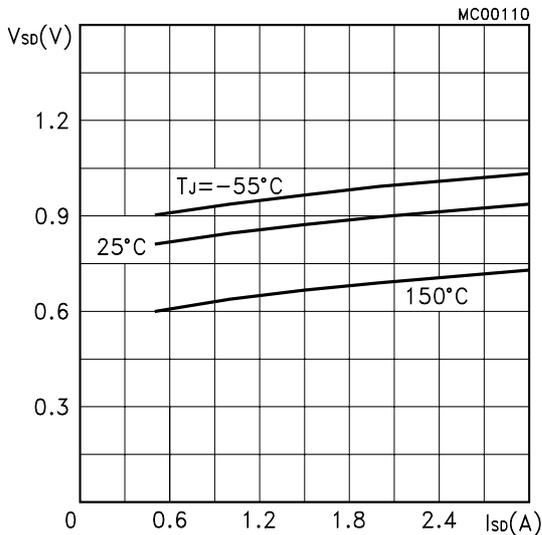
Normalized Gate Threshold Voltage vs Temperature **p-ch**



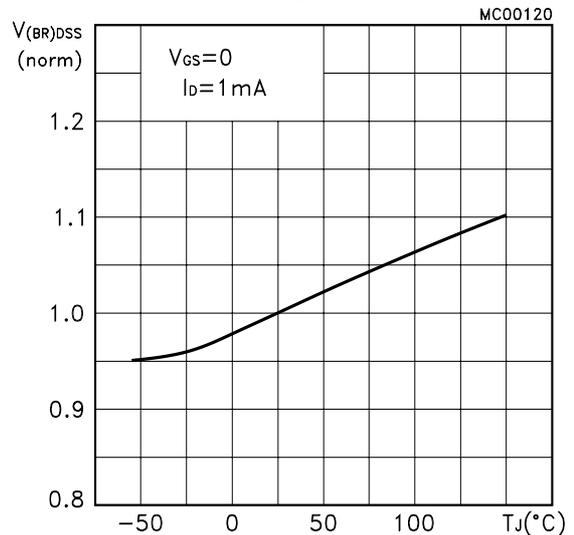
Normalized on Resistance vs Temperature **p-ch**



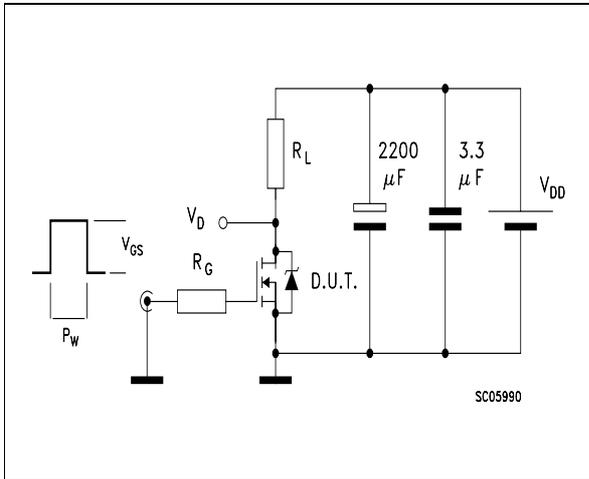
Source-drain Diode Forward Characteristics **p-ch**



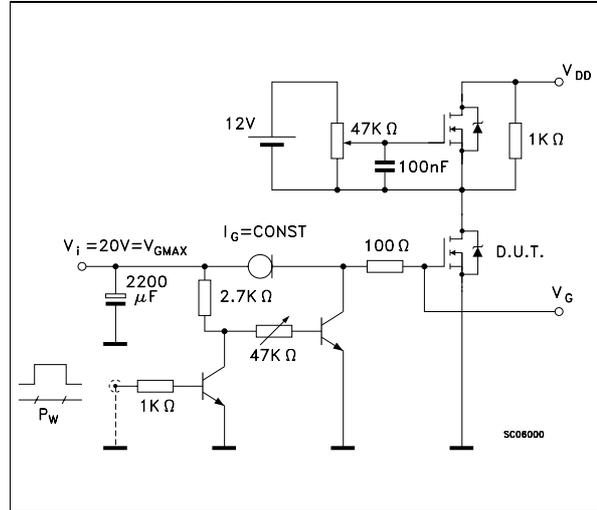
Normalized Breakdown Voltage vs Temperature **p-ch**



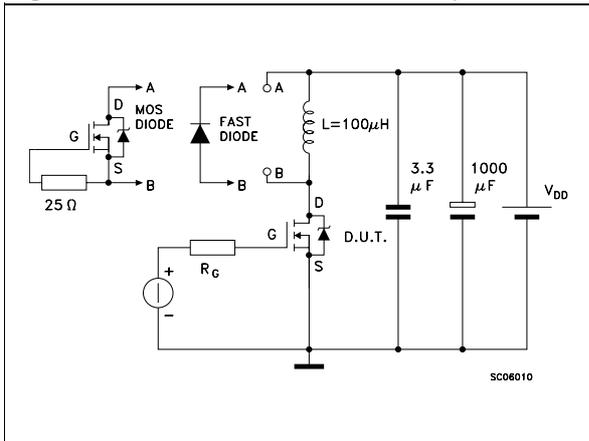
**Fig. 1: Switching Times Test Circuits For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

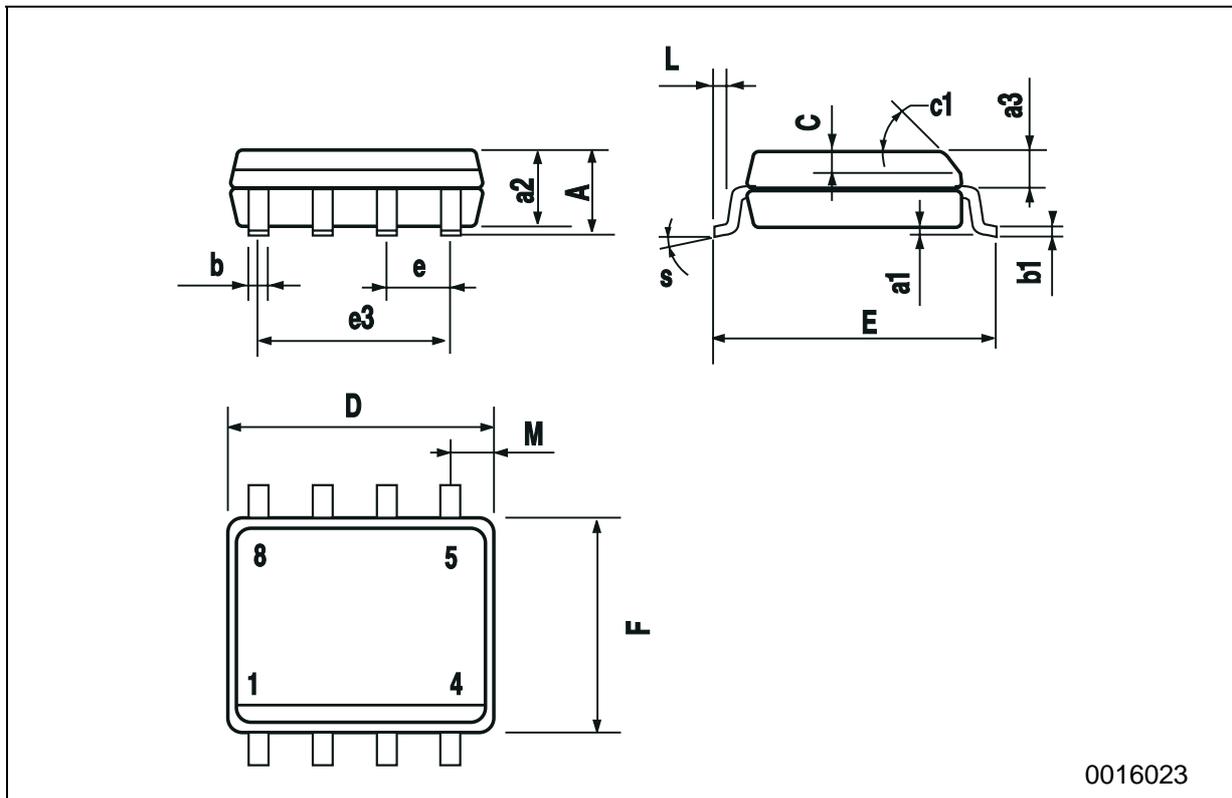


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## STS3C2F100

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### Revision History

Date	Revision	Description of Changes
Friday 18 June 2004	1.0.1	FIRST ISSUE

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