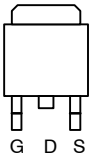
N-Channel 40-V (D-S), 175°C MOSFET, Logic Level

PRODUCT SUMMARY			
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
40	0.005 @ V_{GS} = 10 V	75[a]	130
	0.006 @ V_{GS} = 4.5 V	75[a]	

FEATURES

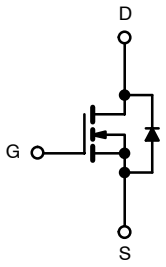
- TrenchFET® Power MOSFET
- 175°C Maximum Junction Temperature
- 100% R_g Tested

TO-263



Top View

Ordering Information: SUM75N04-05L —E3



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	75[a]	A
	T_C = 125°C		55	
Pulsed Drain Current		I_{DM}	240	
Single Pulse Avalanche Current		I_{AS}	75	
Single Pulse Avalanche Energy	L = 0.1 mH	E_{AS}	280	mJ
Power Dissipation	T_C = 25°C	P_D	250[b]	W
	T_A = 25°C [c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount[c]	R_{thJA}	40	°C/W
Junction-to-Case		R_{thJC}	0.4	

Notes
a. Package limited.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0		3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			50	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 175°C			250	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	120			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 75 A		0.004	0.005	Ω
		V_{GS} = 4.5 V, I_D = 75 A		0.005	0.006	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.0083	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.010	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	30			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		6400		pF
Output Capacitance	C_{oss}			1700		
Reverse Transfer Capacitance	C_{rss}			700		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 75 A		130	200	nC
Gate-Source Charge[c]	Q_{gs}			20		
Gate-Drain Charge[c]	Q_{gd}			30		
Gate Resistance	R_g	f = 1.0 MHz	1.4	2.8	4.2	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 75 A, V_{GEN} = 10 V, R_g = 2.5 Ω		15	30	ns
Rise Time[c]	t_r			60	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			130	260	
Fall Time[c]	t_f			70	140	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[b]						
Continuous Current	I_S				75	A
Pulsed Current	I_{SM}				240	
Forward Voltage[a]	V_{SD}	I_F = 75 A , V_{GS} = 0 V		1.0	1.3	V
Reverse Recovery Time	t_{rr}	I_F = 75 A, di/dt = 100 A/μs		65	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4	8	A
Reverse Recovery Charge	Q_{rr}			130	260	nC

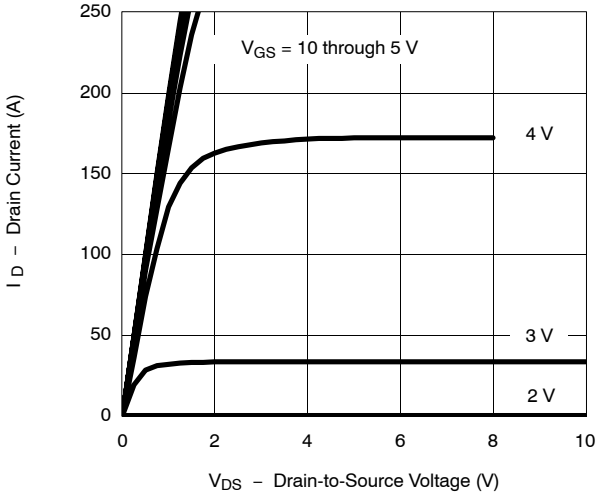
Notes

a. Pulse test: pulse width ≤ 300 μsec, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

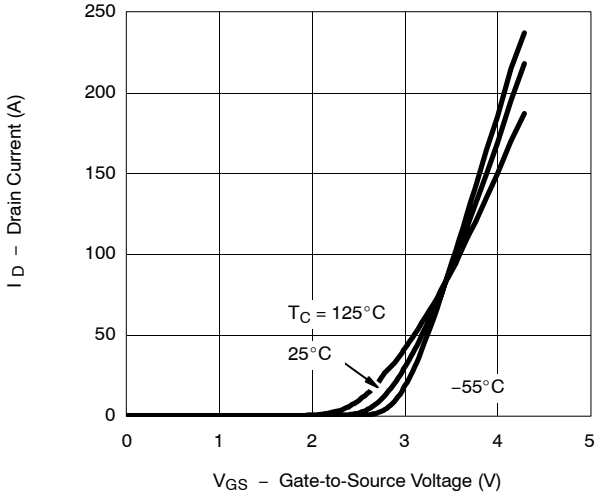
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

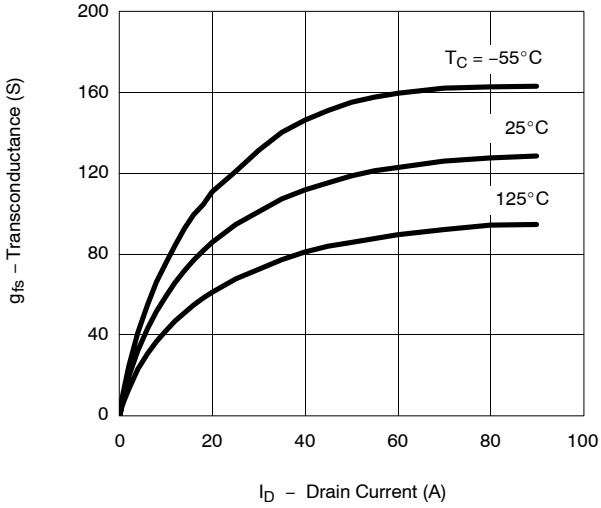
Output Characteristics



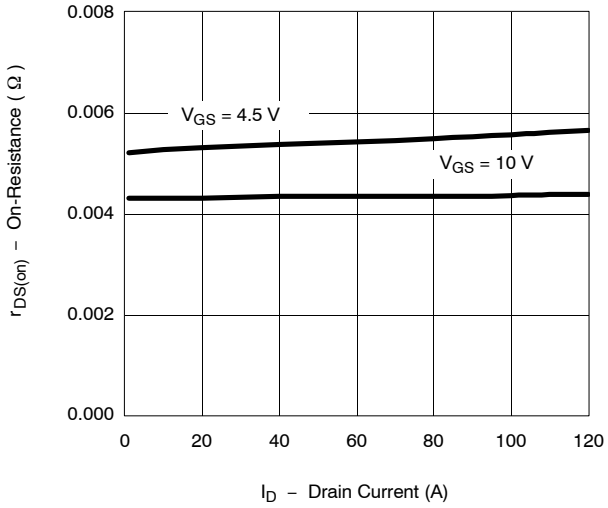
Transfer Characteristics



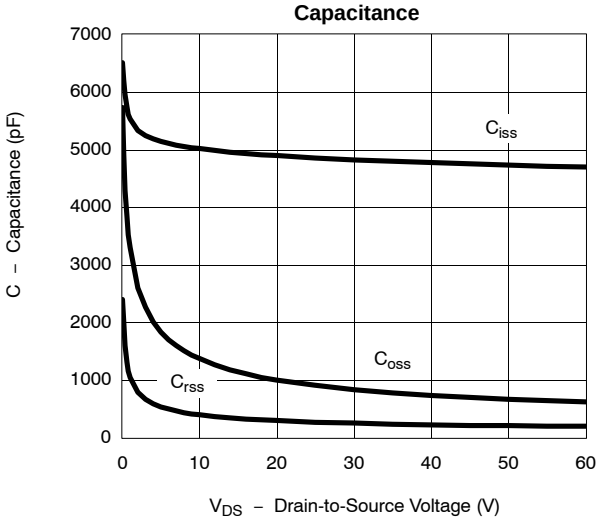
Transconductance



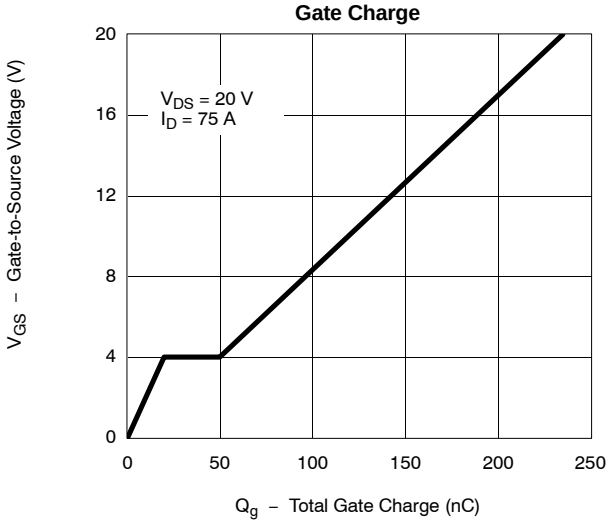
On-Resistance vs. Drain Current



Capacitance

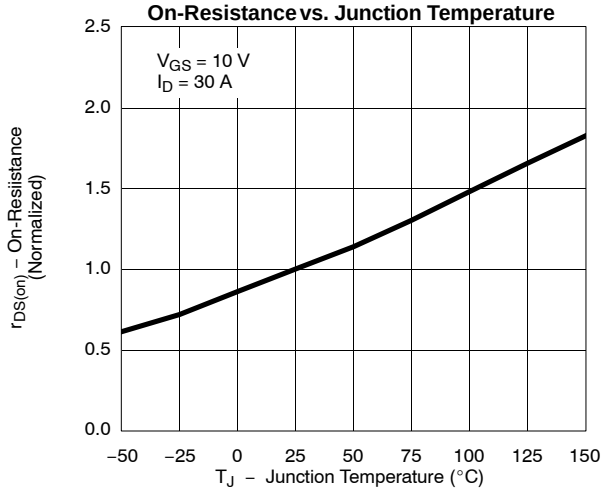


Gate Charge

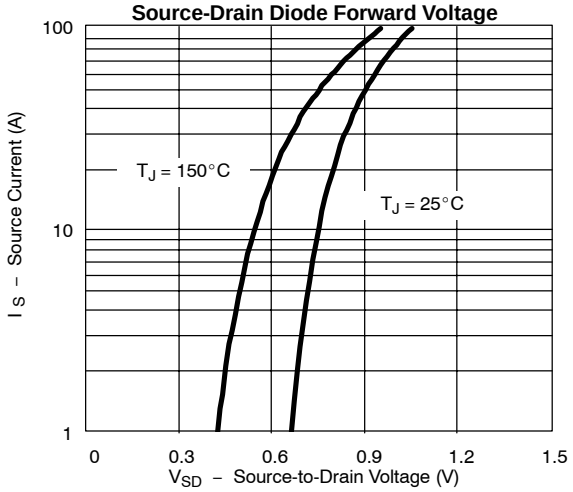


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

On-Resistance vs. Junction Temperature

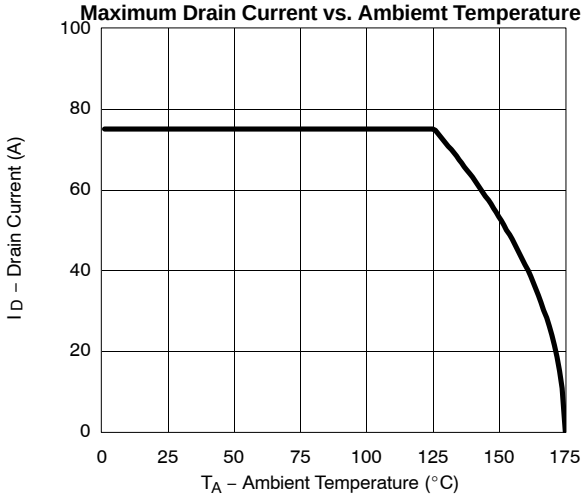


Source-Drain Diode Forward Voltage

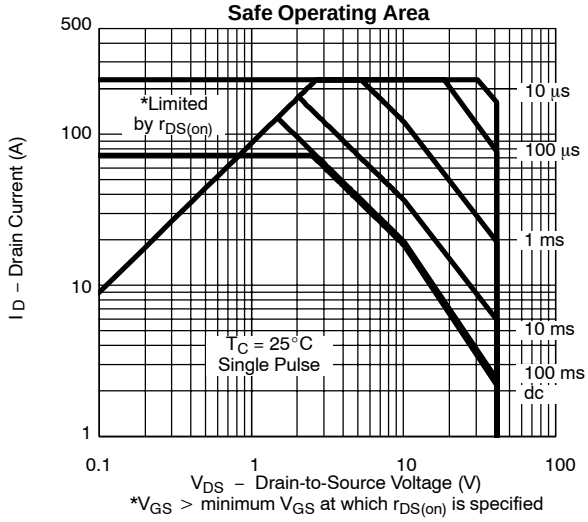


THERMAL RATINGS

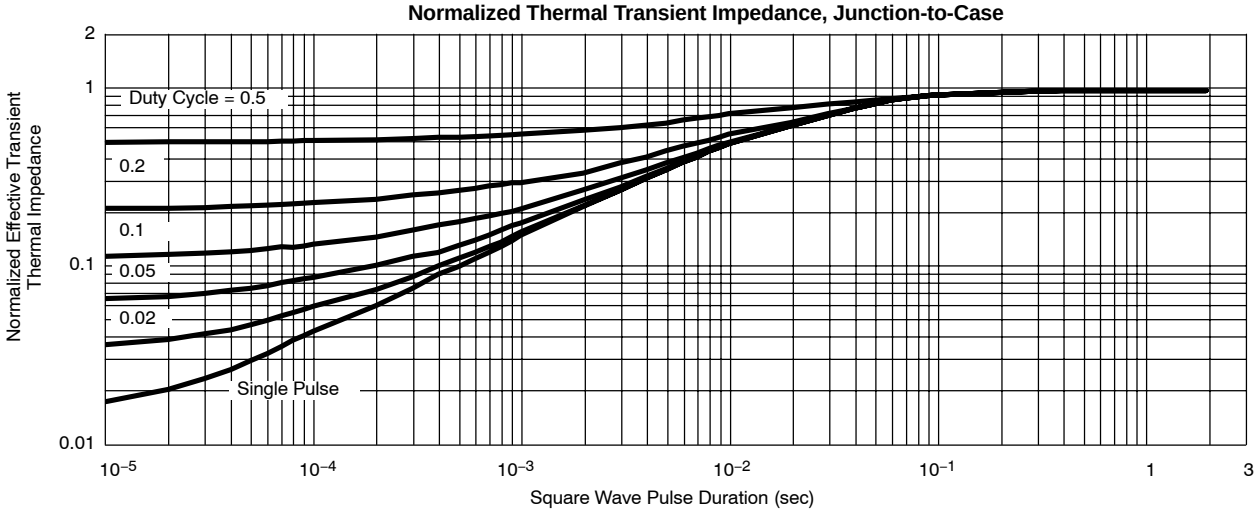
Maximum Drain Current vs. Ambiemt Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



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