



JK FLIP-FLOP

SY10EL35
SY100EL35

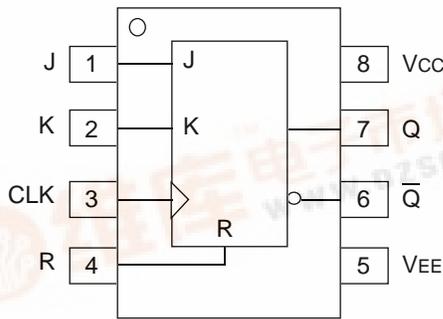
FEATURES

- 525ps propagation delay
- 2.2GHz toggle frequency
- High bandwidth output transistions
- Internal 75KΩ input pull-down resistors
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL35 are high-speed JK Flip-Flops. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave and, thus, the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

TRUTH TABLE⁽¹⁾

J	K	R	CLK	Q _{n+1}
L	L	L	Z	Q _n
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	\bar{Q}_n
X	X	H	X	L

NOTE:

1. Z = LOW-to-HIGH transition.

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply Current	—	27	32	—	27	32	—	27	32	—	27	32	mA
	10EL	—	27	32	—	27	32	—	27	32	—	27	32	
	100EL	—	27	32	—	27	32	—	27	32	—	27	37	
V _{EE}	Power Supply Voltage	—	-5.2	—	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	V
	10EL	—	-5.2	—	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	
	100EL	—	-4.5	—	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

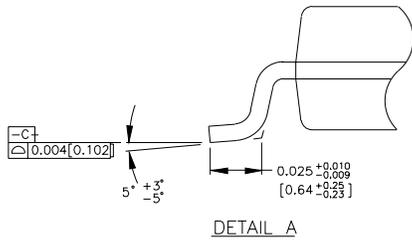
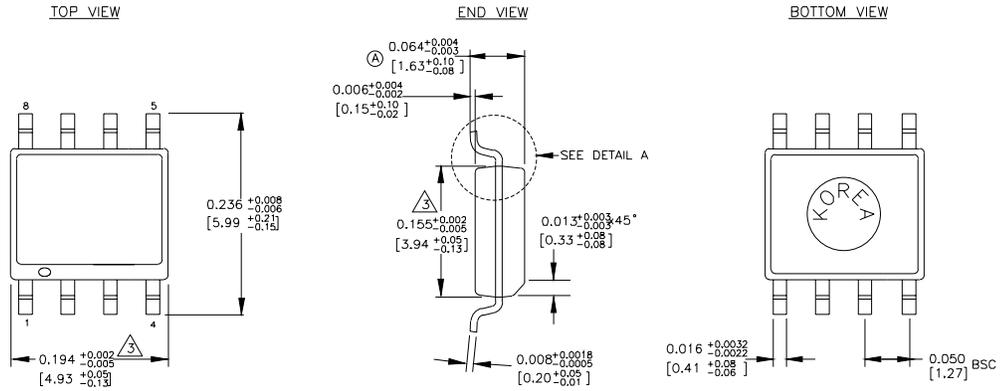
AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f _{MAX}	Maximum Toggle Frequency	1.4	2.0	—	1.8	2.2	—	1.8	2.2	—	1.8	2.2	—	GHz
t _{PLH} t _{PHL}	Propagation Delay to Output	290 225	515 450	—	340 275	515 450	690 625	350 275	525 450	700 625	395 350	570 525	745 700	ps
t _S	Set-up Time	150	0	—	150	0	—	150	0	—	150	0	—	ps
t _H	Hold Time	250	100	—	250	100	—	250	100	—	250	100	—	ps
t _{RR}	Reset Recovery	400	200	—	400	200	—	400	200	—	400	200	—	ps
t _{PW}	Minimum Pulse Width CLK, Reset	400	—	—	400	—	—	400	—	—	400	—	—	ps
t _r t _f	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL35ZC	Z8-1	Commercial
SY10EL35ZCTR	Z8-1	Commercial
SY100EL35ZC	Z8-1	Commercial
SY100EL35ZCTR	Z8-1	Commercial

8 LEAD SOIC .150" WIDE (Z8-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

