查询TC129C14A 供应商

TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TC,129C14A, TCM129C16A, TCM129C17A COMBINED SINGLE-CHIP PCM CODEC AND FILTER

SCTS030E – AUGUST 1989 – REVISED OCTOBER 1996

- **Replace Use of TCM2910A and TCM2911A in Tandem With TCM2912B/C**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption:**
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 Hz to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage References**
- **Improved Version of TCM29C13 Series and TCM129C13 Series**

FEATURES TABLE

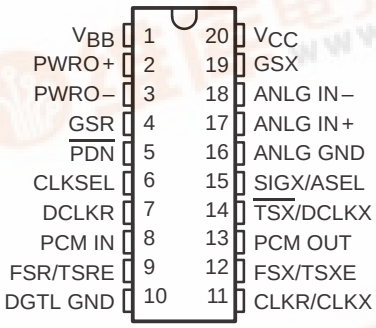
FEATURE	29C13A 129C13A	29C14A 129C14A	29C16A 129C16A	29C17A 129C17A
Number of Pins:				
24		X		
20	X			
16			X	X
μ-Law/A-Law Coding:				
μ-Law	X	X	X	
A-Law	X	X		
Gain Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

description

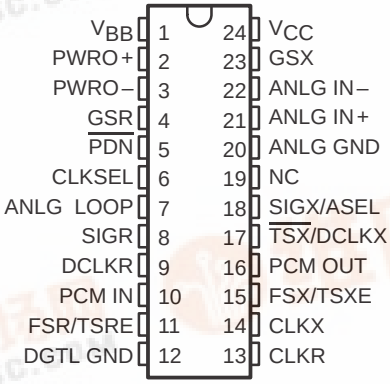
The TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A are single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A or TCM2911A in tandem with the TCM2912C. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data storage systems
- Digital signal processing

TCM29C13A, TCM129C13A
DW OR N PACKAGE
(TOP VIEW)

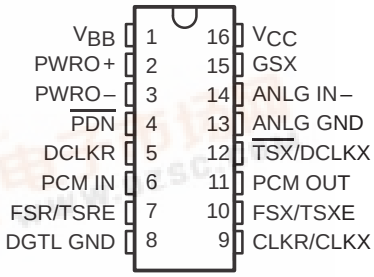


TCM29C14A, TCM129C14A
DW PACKAGE
(TOP VIEW)



NC – No internal connection

TCM29C16, TCM29C16A,
TCM129C16, TCM129C17A
DW OR N PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

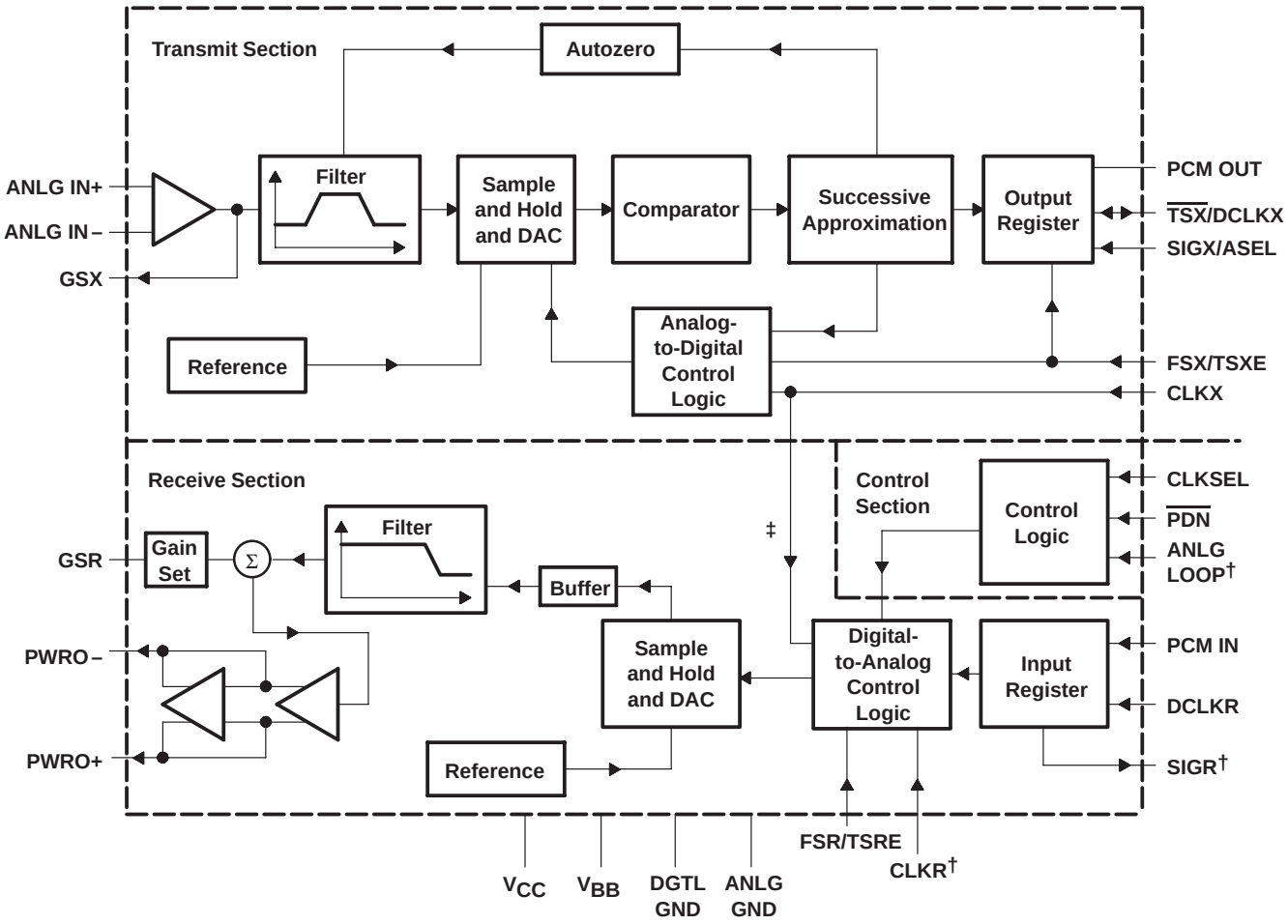
description (continued)

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM29C13A, TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A provide the band-pass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information. These devices contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

The TCM29C13A, TCM29C14A, TCM29C16A, and TCM29C17A are characterized for operation from 0°C to 70°C. The TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A are characterized for operation from –40°C to 85°C.

functional block diagram



† TCM29C14A and TCM129C14A only.
‡ TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129C17A only

Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
ANLG GND	16	20	13		Analog ground return for all internal voice circuits. ANLG GND is internally connected to DGTL GND.
ANLG IN+	17	21		I	Noninverting analog input to uncommitted transmit operational amplifier. ANLG IN+ is internally connected to ANLG GND on TCM29C16A, TCM129C16A, TCM29C17A, and TCM129C17A.
ANLG IN–	18	22	14	I	Inverting analog input to uncommitted transmit operational amplifier.
ANLG LOOP		7		I	Provides loopback test capability. When ANLG LOOP is high, PWRO+ is internally connected to ANLG IN.
CLKR	11	13	9	I	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for the TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129C17A.
CLKSEL	6	6		I	Clock-frequency selection. CLKSEL must be connected to V_{BB}, V_{CC}, or GND to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to GND, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
CLKX	11	14	9	I	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable-date-rate mode. CLKR and CLKX are internally connected for the TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129c17A.
DCLKR	7	9	5	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receiver data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	10	12	8		Digital ground for all internal logic circuits. DGTL GND is internally connected to ANLG GND.
FSR/TSRE	9	11	7	I	Frame-synchronization clock input/time-slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and nonsignaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
FSX/TSXE	12	15	10	I	Frame-synchronization clock input/time-slot enable for transmit channel. FSX/TSXE operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSR	4	4		I	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
GSX	19	23	15	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.

Terminal Functions (Continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
PCM IN	8	10	6	I	Receive PCM input. PCM data is clocked in on PCM IN on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	13	16	11	O	Transmit PCM output. PCM data is clocked out on PCM OUT on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{\text{PDN}}$	5	5	4	I	Power-down select. The device is inactive with a TTL low-level input to this $\overline{\text{PDN}}$ and active with a TTL high-level input to this $\overline{\text{PDN}}$.
PWRO+	2	2	2	O	Noninverting output of power amplifier. PWRO+ drives transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
PWRO–	3	3	3	O	Inverting output of power amplifier. PWRO– is functionally identical with and complementary to PWRO+.
SIGR		8		O	Signaling bit output, receive channel. In the fixed-data-rate mode, SIGR outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
SIGX/ASEL	15	18		I	A-law and μ-law operation select. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or GND, μ-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LBS) of the PCM word during signaling frames on PCM OUT (TCM29C14A and TCM129C14A only). SIGX/ASEL is internally connected to provide μ-law operational for TCM29C16A and TCM129C16A and A-law operation for TCM29C17A and TCM129C17A.
$\overline{\text{TSX}}$/DCLKX	14	17	12	I/O	Transmit channel time-slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output to be used as an enable signal for a 3-state output buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at a TTL level from 64 kHz to 2.048 MHz.
V_{BB}	1	1	1		Most negative supply voltage. Input is –5 V ±5%.
V_{CC}	20	24	16		Most positive supply voltage. Input is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 15 V
Output voltage range, V_O . . . . . –0.3 V to 15 V
Input voltage range, V_I . . . . . –0.3 V to 15 V
Digital ground voltage range . . . . . –0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 1375 mW
Operating free-air temperature range, T_A: TCM29CxxA . . . . . 0°C to 70°C
TCM129CxxA . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		–4.75	–5	–5.25	V
	Digital ground voltage, with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
V_I	CLKSEL input voltage	2.048 MHz	V_{BB}		V_{BB} +0.5	V
		1.544 MHz	0		0.5	
		1.536 MHz	V_{CC} –0.5		V_{CC}	
R_L	Load resistance	GSX	10			kΩ
		PWRO+ and/or PWRO–	300			Ω
C_L	Load capacitance	GSX			50	pF
		PWRO+ and/or PWRO–			100	
T_A	Operating free-air temperature	TCM29CxxA	0		70	°C
		TCM129CxxA	–40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltage is at analog inputs and outputs. V_{CC} and V_{BB} terminals are with respect to ANLG GND. All other voltages are referenced to DGTL GND unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29CxxA			TCM129CxxA			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Operating			7	9		8	13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		0.5	1.1		0.7	1.5	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		0.3	0.9		0.4	1	
I_{BB}	Supply current from V_{BB}	Operating			−7	−9		−8	−13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		−0.5	−1		−0.7	−1.5	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		−0.3	−0.9		−0.4	−1.1	
P_D	Power dissipation	Operating			70	90		80	130	mW
		Standby	FSX or FSR at V_{IL} after 300 ms		5	10		7	15	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		3	8		4	10	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

ground terminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC resistance between ANLG GND and DGTL GND			34		Ω

digital interface

PARAMETER			TEST CONDITIONS	TCM29CxxA			TCM129CxxA			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = −9.6 mA	2.4			2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			2.4			
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIGR		I_{OL} = 3.2 mA			0.4			0.5	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10			12	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10			12	μA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN –	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN –				±25	mV
Common-mode rejection at ANLG IN +, ANLG IN –		55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN –		10			MΩ

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage at PWRO+, PWRO– (single ended)	Relative to ANLG GND		80	180	mV
Output resistance at PWRO+, PWRO–			1		Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = 5 V, T_A = 25°C (see Notes 4, 5, and 6) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law, Signal input = 1.068 Vrms for A-law		±0.04	±0.2	dBm0
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.04	±0.2	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	
Receive gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted‡	ANLG IN+ = ANLG GND, ANLG IN– = GSX		1	7	dBrnC0
Transmit noise, C-message weighted with 8-bit signaling (TCM129C14A and TCM29C14A only)	ANLG IN+ = ANLG GND, ANLG IN– = GSX, 6th frame signaling			13	dBrnC0
Transmit noise, psophometrically weighted‡	ANLG IN+ = ANLG GND, ANLG IN– = GSX		–82	–80	dBm0p
Receive noise, C-message-weighted quiet code	PCM IN = 11111111 (μ-law), PCM IN = 10101010 (A-law), Measured at PWRO+		2	5	dBrnC0
Receive noise, C-message-weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		3	6	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level			–81	dBm0p

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.
‡ This parameter is achieved through the use of patented circuitry and is not recommended for applications in which composite signals on the transmit side are below –55 dBm0.

power supply rejection ratio and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV(peak-to-peak), f measured at PCM OUT		–40		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV(peak-to-peak), f measured at PCM OUT		–35		dB
	30 ≤ f < 50 kHz			–55		
V_{CC} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV(peak-to-peak), f measured at PWRO+		–40		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV(peak-to-peak), Narrow-band f measured at PWRO+		–40		dB
	30 ≤ f < 50 kHz			–45		
Crosstalk attenuation, transmit to receive (single ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, Unity gain, PCM IN = lowest decode level, Measured at PWRO+	75			dB
Crosstalk attenuation, receive to transmit (single ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	75			dB

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ –30 dBm0	36			dB
	–30 > ANLG IN+ ≥ –40 dBm0	30			
	–40 > ANLG IN+ ≥ –45 dBm0	25			
Receive signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ –30 dBm0	36			dB
	–30 > ANLG IN+ ≥ –40 dBm0	30			
	–40 > ANLG IN+ ≥ –45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			–46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			–46	dBm0
Intermodulation distortion, end to end spurious out-of-band signals, end to end	CCITT G.712 (7.1)			–35	dBm0
	CCITT G.712 (7.2)			–49	
	CCITT G.712 (6.1)			–25	
	CCITT G.712 (9)			–40	
Transmit absolute delay time to PCM OUT	Fixed-data rate, f_{CLKX} = 2.048 MHz, Input to ANLG IN + 1.02 kHz at 0 dBm0		245		µs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		µs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed data rate, Digital input is DMW codes f_{CLKR} = 2.048 MHz,		190		µs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		µs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	16.67 Hz		–30	dB
		50 Hz		–25	
		60 Hz		–23	
		200 Hz	–1.8	–0.125	
		300 Hz to 3 kHz	–0.15	0.15	
		3.3 kHz	–0.35	0.15	
		3.4 kHz	–1	–0.1	
		4 kHz		–14	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.15	dB
		200 Hz	–0.5	0.15	
		300 Hz to 3 kHz	–0.15	0.15	
		3.3 kHz	–0.35	0.15	
		3.4 kHz	–1	–0.1	
		4 kHz		–14	
		4.6 kHz		–30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 3 and 4)

		MIN	NOM	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 7)	220			ns
	Clock duty cycle, $[t_{w(CLK)}/t_{c(CLK)}]$ for CLKX and CLKR	45%	50%	55%	

NOTE 7: FSX CLK must be phase locked with CLKX. FSR CLK must be phase locked with CLKR.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before bit 7 falling edge of CLKX (TMC29C14A and TCM129C14A only)	0		ns
$t_{h(SIGX)}$	Hold time after bit 8 falling edge of CLKX (TCM29C14A and TCM129C14A only)	0		ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Receive data setup time	50		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

		MIN	MAX	UNIT
$t_{d(TSDX)}$	Time-slot delay time from DCLKX (see Note 8)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

NOTE 8: t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

		MIN	MAX	UNIT
$t_{d(TSDR)}$	Time-slot delay time from DCLKR (see Note 9)	140	$t_{d(DCLKR)}$–140	ns
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}$–100	ns
$t_{su(PCM\ IN)}$	Receive data setup time	50		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns
$t_{c(DCLKR)}$	Data clock period	488	15620	ns
$t_{(SER)}$	Time-slot end receive time	0		ns

NOTE 9: t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

			MIN	MAX	UNIT
t_{FSLX}	Transmit frame-sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame-sync minimum down time		1952		ns
$t_{w(DCLK)}$	Pulse duration, data clock			10	µs

switching characteristics

delay time over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3 and 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) (see Note 10)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) (see Note 10)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time-slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) (see Note 10)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM29C14A and TCM129C14A only)		0	2	µs

NOTE 10: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

delay time over recommended ranges of operating conditions, variable-data-rate mode (see Note 11 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Delay from time-slot enable to PCM OUT		0	50	ns
t_{pd9}	Delay from time-slot disable to PCM OUT		0	80	ns
t_{pd10}	Delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

NOTE 11: Timing parameters t_{pd8} and t_{pd9} are referenced to the high-impedance state.

PARAMETER MEASUREMENT INFORMATION

CLKR and CLKX selection requirements for DSP-based applications

CLKX and CLKR must be selected as follows:

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
–5 V†	= (256) × (frame-sync frequency)	TCM29C13A/14A/16A/17A
		TCM129C13A/14A/16A/17A
0 V	= (193) × (frame-sync frequency)	TCM29C13A/14A
		TCM129C13A/14A
5 V	= (192) × (frame-sync frequency)	TCM29C13A/14A
		TCM129C13A/14A

† CLKSEL is internally set to –5 V for TCM29C16A/1A7 and TCM129C16A/17A e.g., for frame-sync frequency = 9.6 kHz

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
–5 V†	= 2.4576 MHz	TCM29C13A/14A/16A/17A
		TCM129C13A/14A/16A/17A
0 V	= 1.8528 MHz	TCM29C13A/14A
		TCM129C13A/14A
5 V	= 1.8432 MHz	TCM29C13A/14A
		TCM129C13A/14A

† CLKSEL is internally set to –5 V for TCM29C16A/1A7 and TCM129C16A/17A.

Corner frequency at 8-kHz frame-sync frequency = 3 kHz, therefore, the corner frequency = (3/8) × (frame-sync frequency for nonstandard frame sync).

PARAMETER MEASUREMENT INFORMATION

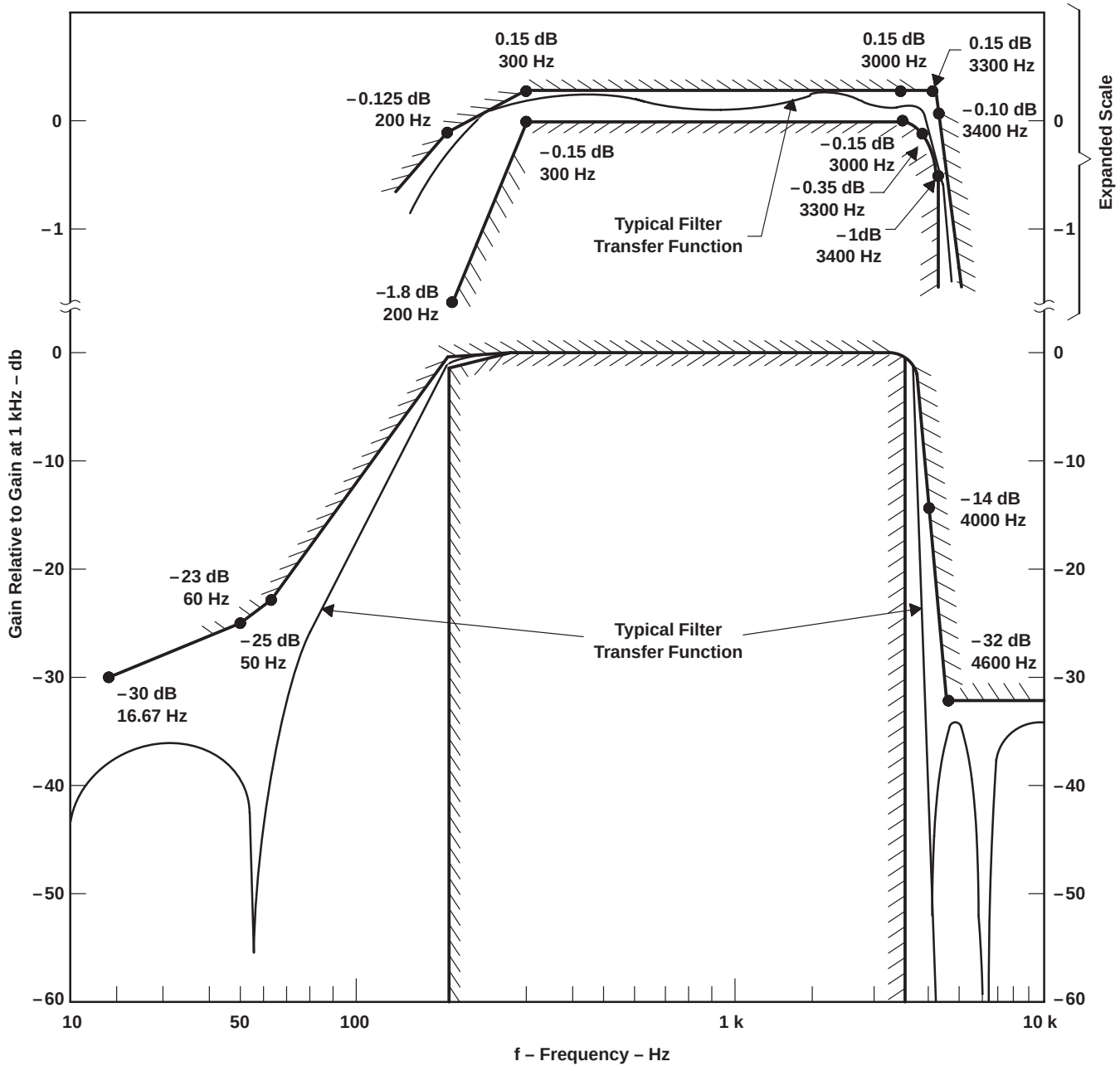
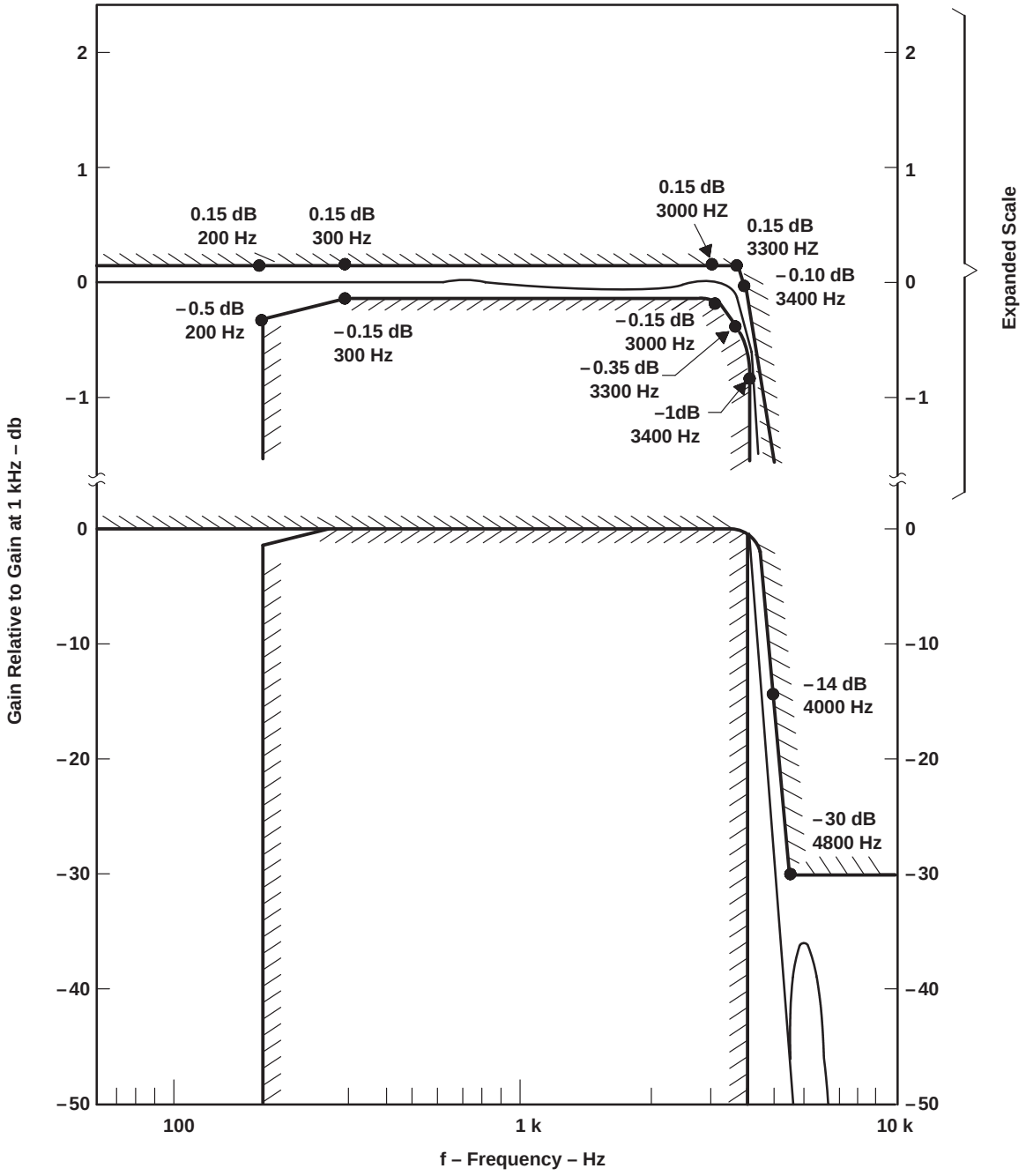


Figure 1. Transmit Filter Transfer Characteristics

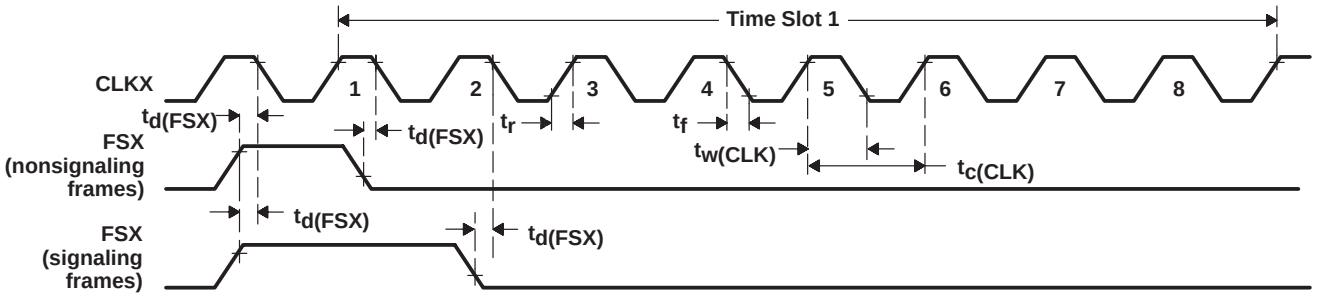
PARAMETER MEASUREMENT INFORMATION



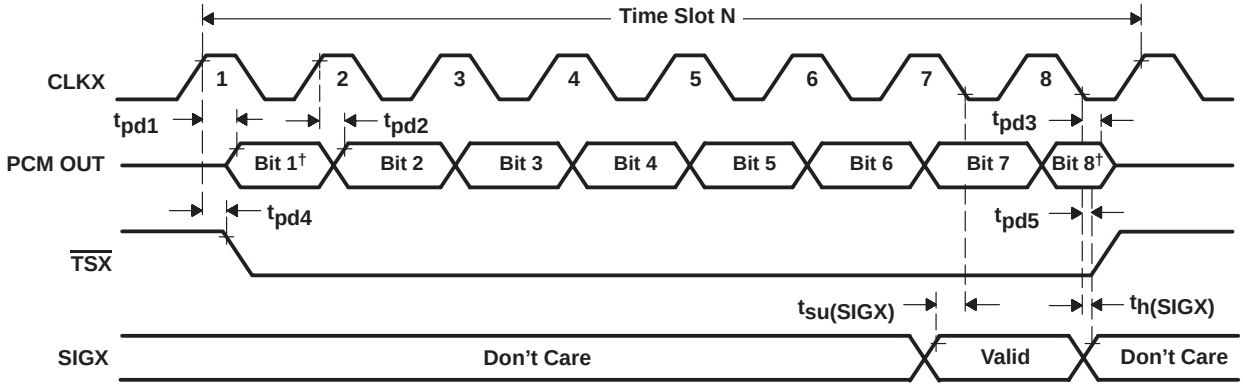
NOTE A: This is a typical transfer function of the receive filter component.

Figure 2. Receive Filter Transfer Characteristics

PARAMETER MEASUREMENT INFORMATION



FRAME SYNCHRONIZATION TIMING



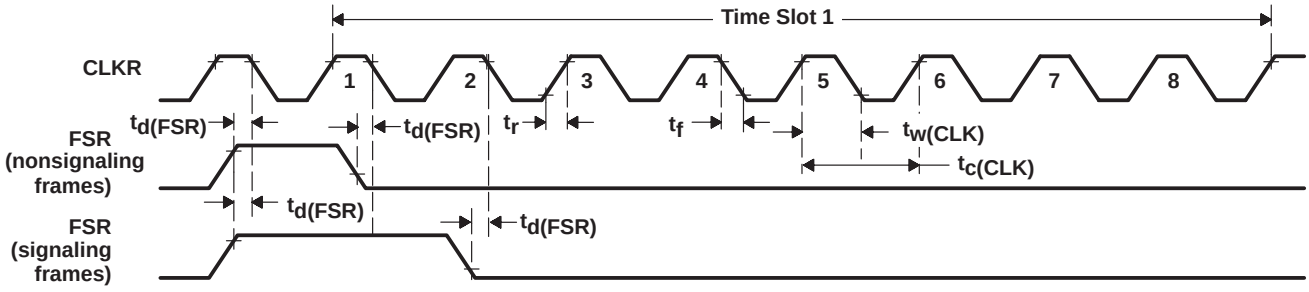
OUTPUT TIMING

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

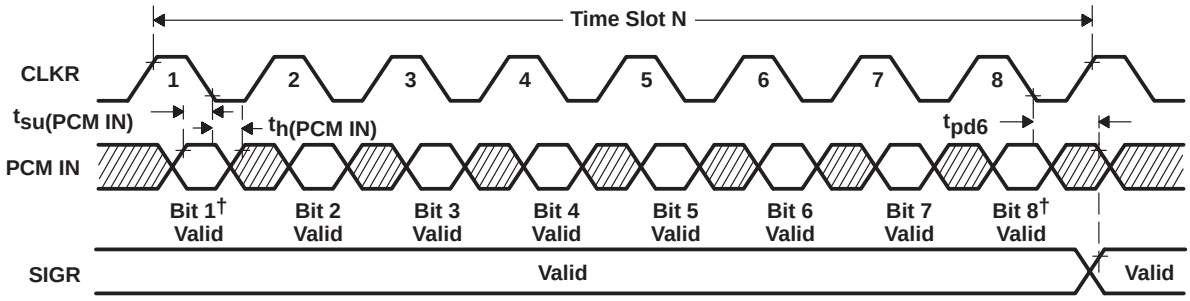
NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 3. Transmit Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION



FRAME SYNCHRONIZATION TIMING



INPUT TIMING

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 4. Receive Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION

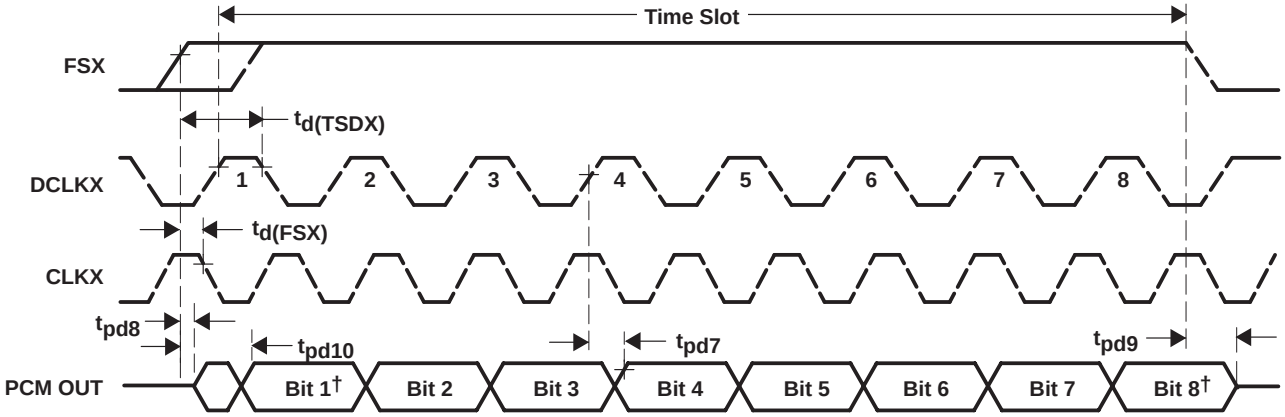


Figure 5. Transmit Timing (Variable-Data Rate)

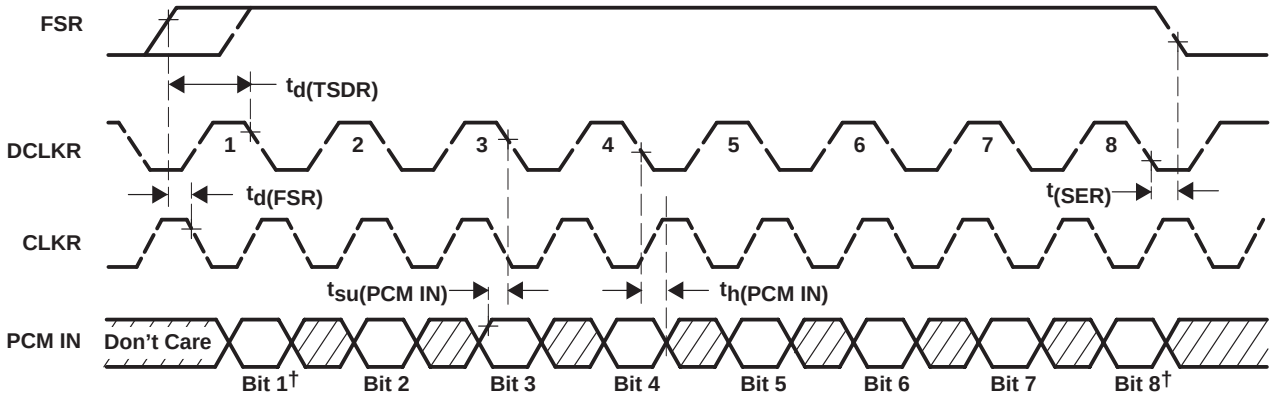


Figure 6. Receive Timing (Variable-Data Rate)

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: All timing parameters are referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which references the high-impedance state.

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM29CxxA and TCM129CxxA devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector, and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent), between each power supply and GND (see Figure 7). If it is possible that a TCM29CxxA- or TCM129CxxA-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up also can occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power-down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

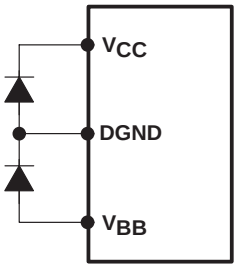


Figure 7. Diode Configuration for Latch-Up Protection Circuitry

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Valid digital information, such as on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR remains low until it is updated by a signalling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 μs after an interruption of CLKX. SIGR is held low approximately 20 μs after an interruption of CLKR. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced 15 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. to place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to an average of 3 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 10 μs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in the high-impedance state within 300 ms.

PRINCIPLES OF OPERATION

fixed-data-rate timing (see Figure 8)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB} and uses master clocks CLKX and CLKR, frame-synchronizer clocks FSX and FSR, and the output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame synchronization pulse one master-clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM12914A and TCM29C14A only). Data is transmitted on PCM OUT on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLKR following FSR. A digital-to-analog (D/A) conversion is performed on received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock-selection terminal (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A only). The TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM29C16A, TCM29C17A, TCM129C16A, and TCM129C17A fixed-data-rate mode operates at 2.048 MHz only.

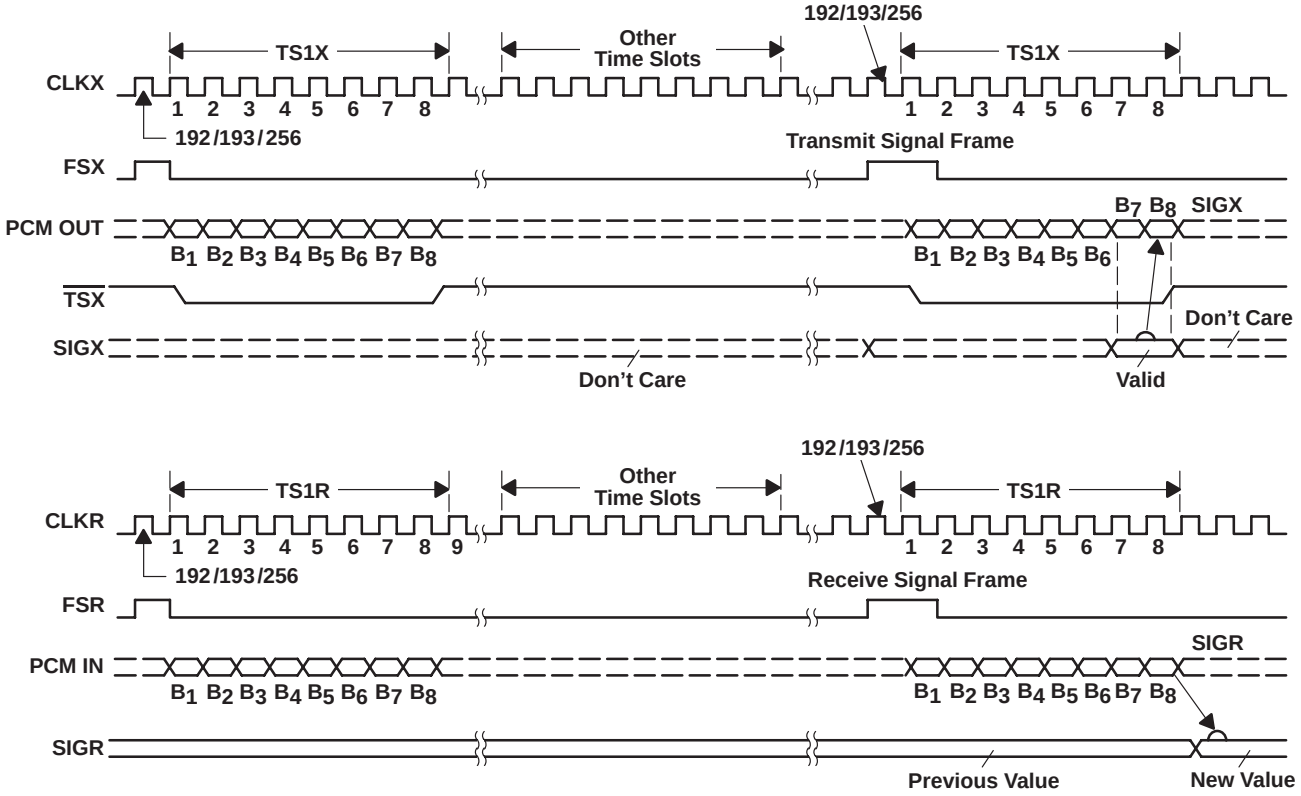


Figure 8. Signaling Timing (Fixed-Data Rate Only)

PRINCIPLES OF OPERATION

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. Master clocks in the TCM129C13A, TCM129C14A, TCM29C13A, and TCM29C14A are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM129C16A, TCM129C17A, TCM29C16A, and TCM29C17A is restricted to 2.048 MHz.

When the FSX/TSXE is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word is repeated in all remaining time slots in the 125-μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

Only the TCM29C14A provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame-sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec decodes the seven most significant bits in accordance with CCITT G.733 recommendations and outputs the logical state of the LSB on SIGR until it is updated in the next signaling frame. Timing relationships for signaling operations are shown in Figure 8. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones: dial tone, ring-back tone, busy tone, and reorder tone.

PRINCIPLES OF OPERATION

analog loopback

A distinctive feature of the TCM29C14A and TCM129C14A is the analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. When ANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO–, and ANLG IN– is internally connected to GSX (see Figure 8).

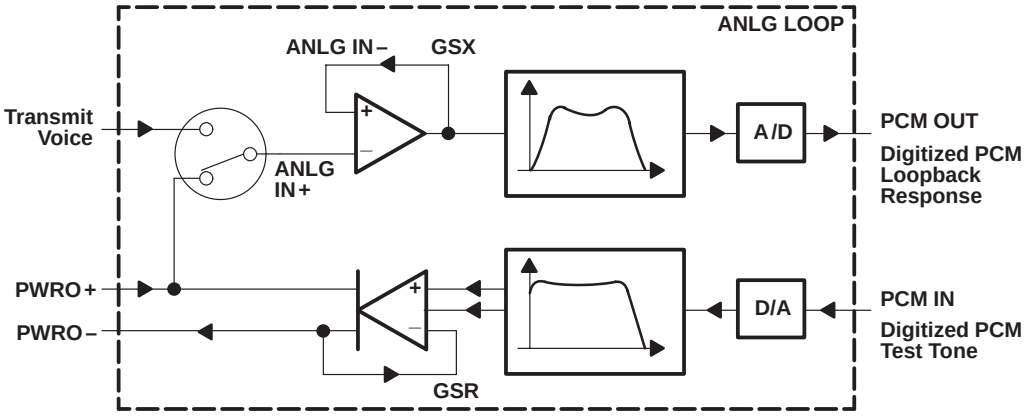


Figure 9. TCM29C14A and TCM129C14A Analog Loopback Configuration

Due to the difference in the transmit and receive transmission levels, a 0-dBm0 code into PCM IN emerges from PCM OUT as a 3-dBm0 code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBm0.

precision voltage references

Voltage references that determine the gain dynamic range characteristics of the device are generated internally. No external components are required to provide the voltage references. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage, which is calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB can be achieved in absolute gain for each half channel, providing the user a significant margin to compensate for error in other system components.

conversion laws

The TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when ASEL is connected to V_{BB}, and μ-law operation is selected by connecting ASEL to V_{CC} or GND. Signaling is not allowed during A-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed-data-rate timing mode to modify the LSB of the PCM output is signaling frames.

The TCM29C16A and TCM129C16A are μ-law only; the TCM29C17A and TCM129C17A are A-law only.

PRINCIPLES OF OPERATION

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN+ can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing filter section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

The pass-band section provides flatness and stop-band attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching-systems requirements.

A high-pass section configuration has been chosen to reject low-frequency noise from 50-Hz and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign-bit-averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

PRINCIPLES OF OPERATION

receive output power amplifiers

A balanced-output amplifier allows maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300-Ω single-ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of GSR. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO–, the receive level is maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and –12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO–.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

APPLICATION INFORMATION

output gain-set design considerations (see Figure 9)

PWRO+ and PWRO– are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO–
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.006 Vrms).

$$V_{OD} = A \bullet V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

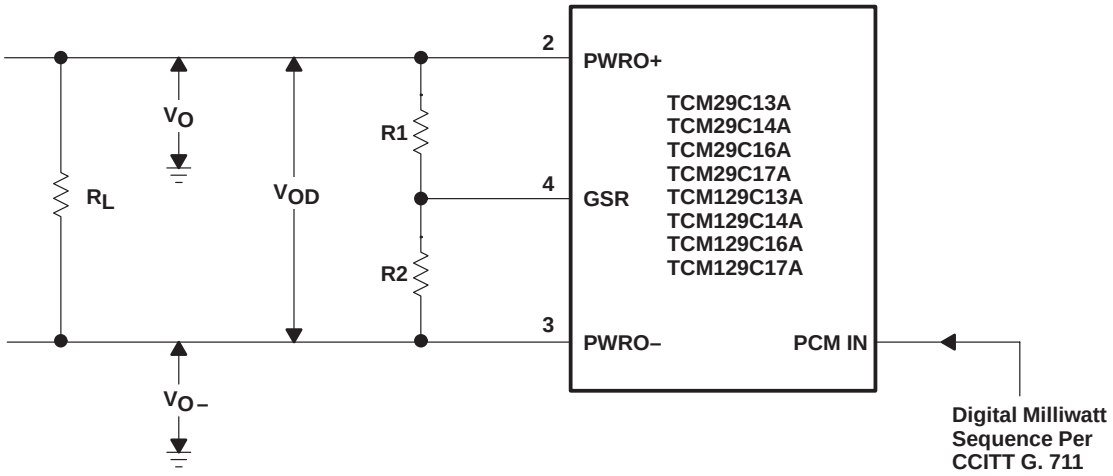


Figure 10. Gain-Setting Configuration

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