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NTE937M
Integrated Circuit
JFET Input Operational Amplifier

Description:

The NTE937M is a monolithic JFET input operational amplifier in an 8–Lead DIP type package incorporating well–matched, high voltage JFET's on the same chip with standard bi–polar transistors. This amplifier features low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common–mode rejection. It is also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages:

- Replaces Expensive Hybrid and Module FET OP Amps
- Rugged JFET's Allow Blow–Out Free Handling Compared with MOSFET Input Device
- Excellent for Low Noise Applications using either High or Low Source Impedance – Very Low 1/f Corner
- Offset Adjust does not Degrade Drift or Common–Mode Rejection as in Most Monolithic Amplifiers
- New Output Stage Allows use of Large Capacitive Loads (10,000pF) without Stability Problems
- Internal Compensation and Large Differential Input Voltage Capability

Applications:

- Precision High Speed Integrators
- Fast D/A and A/D Converters
- High Impedance Buffers
- Wideband, Low Noise, Low Drift Amplifiers
- Logarithmic Amplifiers
- Photocell Amplifiers
- Sample and Hold Circuits

Absolute Maximum Ratings:

Supply Voltage . . . . ±18V
Maximum Power Dissipation (at +25°C, Note 1), P_d 500mW
Differential Input Voltage . . . . ±30V
Input Voltage Range (Note 2) . . . . ±16V
Output Short–Circuit Duration . . . . Continuous
Maximum Operating Junction Temperature (Note 1), $T_J$max . . . . +100°C
Storage Temperature Range, T_{stg} . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . +300°C
Thermal Resistance, Junction–to–Ambient (Note 1), R_{thJC} . . . . +155°C/W

Note 1. The maximum power dissipation for this device must be derated at elevated temperatures and is dictated by $T_J$max, R_{thJC}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_J\text{max} – T_A)/R_{thJC}$ or the +25°C $P_d$max, whichever is less.

Note 2. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DC Electrical Characteristics: (T_A = +25C, V_S = ±15V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}		–	5	10	mA

DC Electrical Characteristics: (V_S = ±15V, 0° ≤ T_A ≤ +70°C, T_{HIGH} = +70°C unles otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	R_S = 50Ω, T_A = +25°C	–	3	10	mV
		Over Temperature	–	–	13	mV
Average TC of Input Offset Voltage	$\Delta V_{OS}/\Delta T$	R_S = 50Ω	–	5	–	µV/°C
Change in Average TC with V_{OS} Adjust	$\Delta TC/\Delta V_{OS}$	R_S = 50Ω, Note 3	–	0.5	–	µV/°C
Input Offset Current	I_{OS}	T_J = +25°C, Note 4	–	3	50	pA
		$T_J \le T_{HIGH}$	–	–	2	nA
Input Bias Current	I_B	T_J = +25°C, Note 4	–	30	200	pA
		$T_J \le T_{HIGH}$	–	–	8	nA
Input Resistance	R_{IN}	T_J = +25°C	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VOL}	T_A = +25°C, V_O = ±10V, R_L = 2k	25	200	–	V/mV
		Over Temperature	15	–	–	V/mV
Output Voltage Swing	V_O	R_L = 10k	±12	±13	–	V
		R_L = 2k	±10	±12	–	V
Input Common–Mode Voltage Range	V_{CM}		±10	+15.1 –12	–	V
Common–Mode Rejection Ratio	CMRR		–	80	100	dB
Supply Voltage Rejection Ratio	PSRR	Note 5	–	80	100	dB

Note 3. The temperature coeficient of the adjust input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common–mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 4. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_J = T_A + R_{thJC} P_d$ where R_{thJC} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

AC Electrical Characteristics: (T_A = +25C, V_S = ±15V unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Slew Rate	SR	A_V = 5		30	50	–	V/µs
Gain Bandwidth Product	GBW			–	20	–	MHz
Settling Time to 0.01%	t_s	Note 6		–	1.5	–	µs
Equivalent Input Noise Voltage	e_N	R_S = 100Ω	f = 100Hz	–	15	–	nV/√Hz
			f = 1000Hz	–	12	–	nV/√Hz
Equivalent Input Current Noise	i_N	f = 100Hz		–	0.01	–	pA/√Hz
		f = 1000Hz		–	0.01	–	pA/√Hz
Input Capacitance	C_{IN}			–	3	–	pF

Note 6. A_V = –5, the feedback resistor from output to input is 2kΩ and the output step is 10V.

Pin Connection Diagram