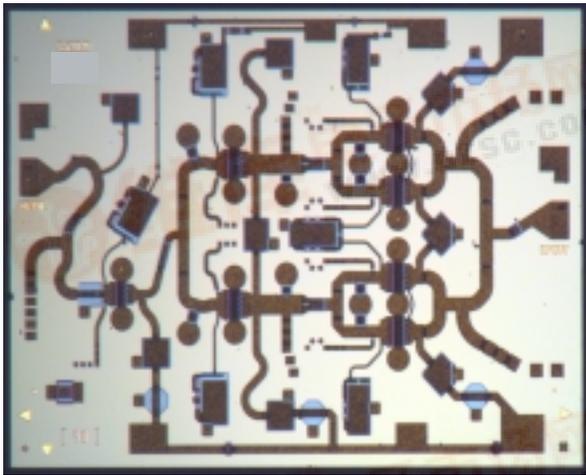


## 23 - 29 GHz High Power Amplifier

## TGA9070-SCC



### Key Features and Performance

- 0.25um pHEMT Technology
- 23 GHz - 29 GHz Frequency Range
- Nominal 1 Watt (28GHz) @ P1dB
- Nominal Gain of 23 dB
- Bias 7V @ 400 mA
- Chip Dimensions 4.1mm x 3.0mm

### Primary Applications

- LMDS
- Point-to-Point Radio

### Description

The TriQuint TGA9070-SCC is a three stage HPA MMIC design using TriQuint's proven 0.25 um Power pHEMT process to support a variety of millimeter wave applications including point-to-point digital radio, LMDS/LMCS and Ka-band satellite spacecraft and ground terminals.

The three stage design consists of a 400 um input device driving a pair of 600 um interstage devices followed by four 600 um output devices.

The TGA9070 provides greater than 1W of output power across 23-29 GHz with a typical PAE of 35%. Typical small signal gain is 23 dB.

The TGA9070 requires minimum off-chip components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form.

TABLE I  
RECOMMENDED MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE	NOTES
V <sup>+</sup>	POSITIVE SUPPLY VOLTAGE	8 V	
I <sup>+</sup>	POSITIVE SUPPLY CURRENT	1 A	<u>1/</u>
P <sub>D</sub>	POWER DISSIPATION	8 W	
P <sub>IN</sub>	INPUT CONTINUOUS WAVE POWER	20dBm	
T <sub>CH</sub>	OPERATING CHANNEL TEMPERATURE	150 °C	<u>2/</u> <u>3/</u>
T <sub>M</sub>	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T <sub>STG</sub>	STORAGE TEMPERATURE	-65 to 150 °C	

- 1/ Total current for all 3 stages
- 2/ Junction operating temperature will directly affect the device mean time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ These ratings apply to each individual FET

TABLE II  
DC PROBE TESTS (100%)  
(T<sub>A</sub> = 25 °C ± 5 °C)

NOTES	SYMBOL <u>2/</u>	TEST CONDITIONS <u>3/</u>	LIMITS		UNITS
			MIN	MAX	
	I <sub>DSS1</sub>	STD	40	188	mA
<u>1/</u>	V <sub>P1</sub>	STD	0.5	1.5	V
<u>1/</u>	V <sub>P2</sub>	STD	0.5	1.5	V
<u>1/</u>	V <sub>P3</sub>	STD	0.5	1.5	V
<u>1/</u>	V <sub>P4</sub>	STD	0.5	1.5	V
<u>1/</u>	V <sub>P5</sub>	STD	0.5	1.5	V
<u>1/</u>	V <sub>BVGD1-5</sub>	STD	12	30	V
<u>1/</u>	V <sub>BVGS1</sub>	STD	12	30	V

- 1/ V<sub>P</sub>, V<sub>BVGD</sub>, and V<sub>BVGS</sub> are negative
- 2/ Subscripts are referred to Q1, Q2, Q3, Q4, Q5 accordingly.
- 3/ The measurement conditions are subject to change at the manufacture's discretion (with appropriate notification to the buyer).

STD – Standard Test Conditions (see Table III for definitions)

TABLE IV  
ELECTRICAL CHARACTERISTICS  
( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )  
 $V_d = 6\text{V}$ ,  $I_d = 400\text{ mA}$

NOTE	TEST	MEASUREMENT CONDITIONS <u>1/</u>	VALUE			UNITS
			MIN	TYP	MAX	
<u>2/</u>	POWER OUTPUT AT 1 dB GAIN COMPRESSION	F = 23 - 27 GHz	28.5	30		dBm
		F = 28 GHz	29	30.5		dBm
		F = 29 GHz	28.5	30		dBm
	POWER ADDED EFFICIENCY	F = 23 - 29 GHz		35		%
	SMALL-SIGNAL GAIN MAGNITUDE	F = 23 GHz	19	21	26	dB
		F = 24 - 28 GHz	20	23	28	dB
		F = 29 GHz	19	21	26	dB
	INPUT RETURN LOSS MAGNITUDE	F = 23 - 29 GHz		-10		dB
	OUTPUT RETURN LOSS MAGNITUDE	F = 23 - 29 GHz		-10		dB

1/ RF Probe data is taken at 1 GHz steps

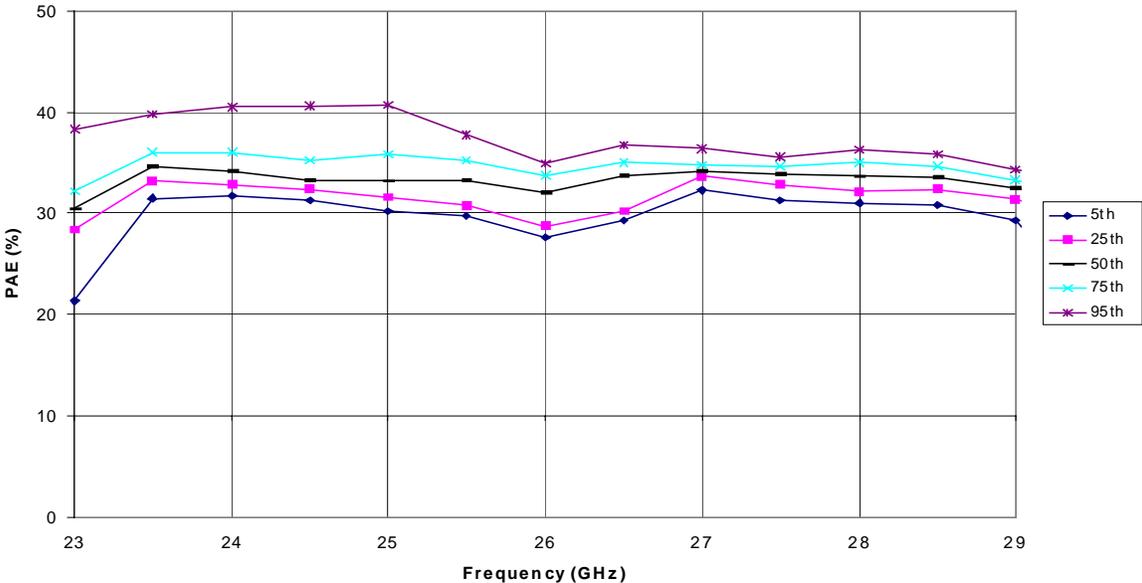
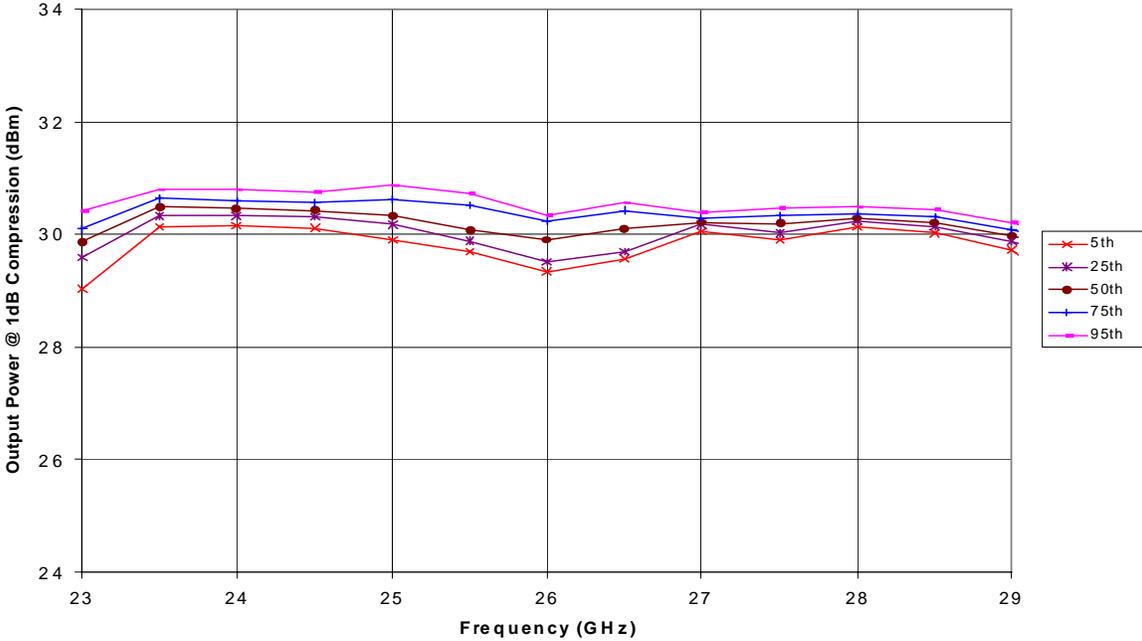
2/  $\Delta P/\Delta T$  typically  $-0.02\text{dB}/^\circ\text{C}$

TABLE V  
RELIABILITY DATA

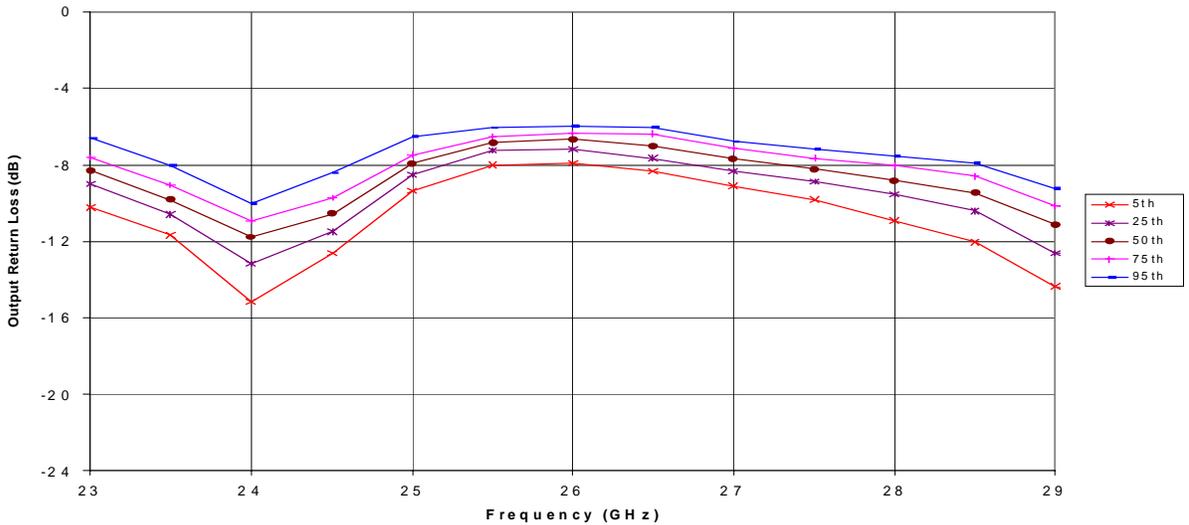
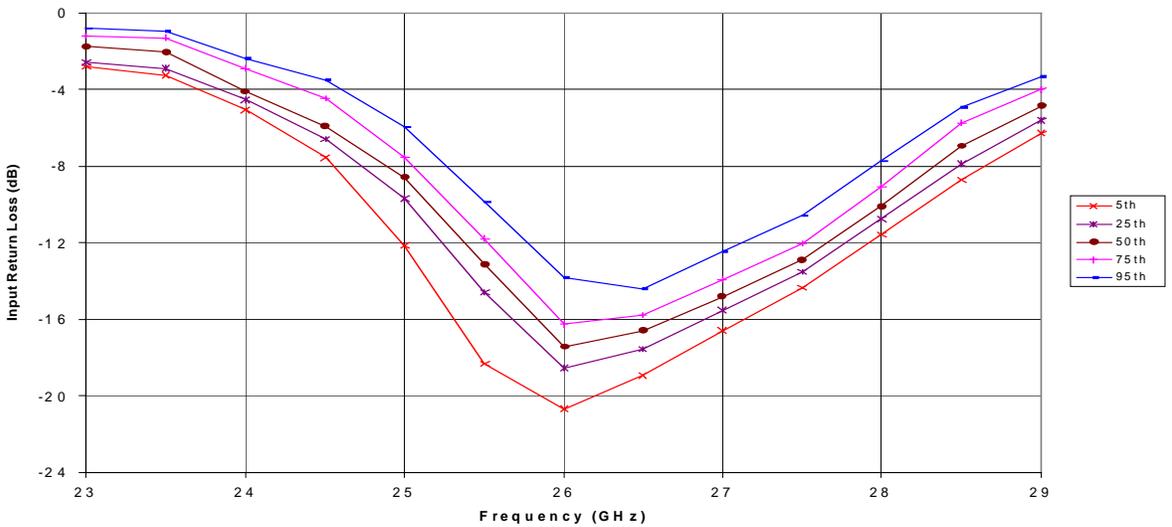
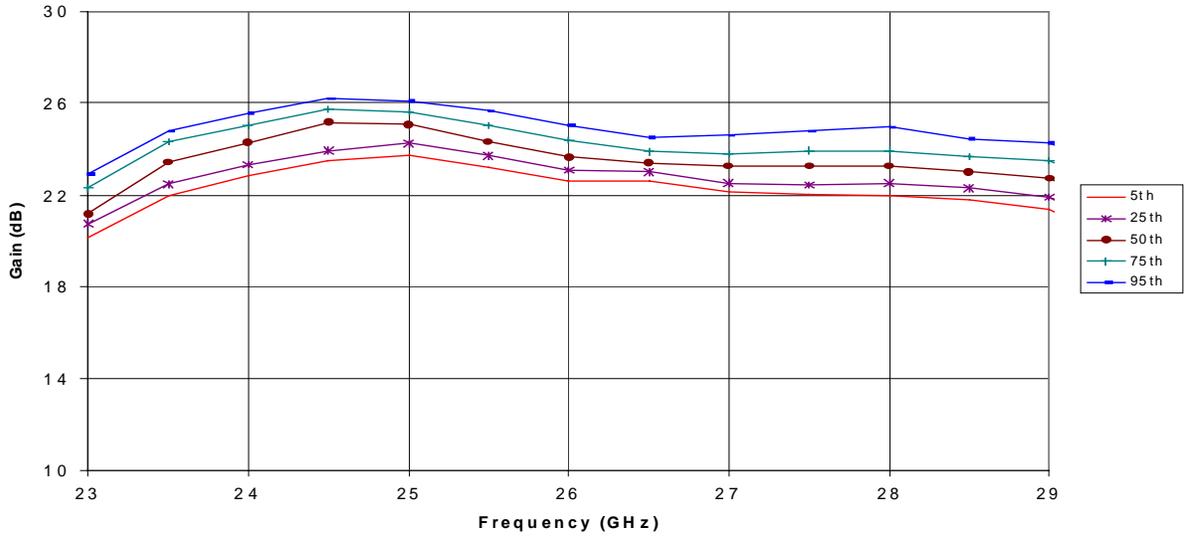
PARAMETER	BIAS CONDITIONS		$P_{\text{DISS}}$ (W)	$R_{\theta\text{JC}}$ (C/W)	$T_{\text{CH}}$ ( $^\circ\text{C}$ )	MTTF (HRS)
	$V_D$ (V)	$I_D$ (mA)				
$R_{\theta\text{JC}}$ Thermal resistance (channel to backside)	6	400	2.4	22.08	123	$> 2\text{ E}6$
	7	400	2.8	22.5	133	$> 1\text{ E}6$

Note: Assumes eutectic attach using 80/20 AuSn mounted to a 10mil CuMo Carrier at  $70^\circ\text{C}$  baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

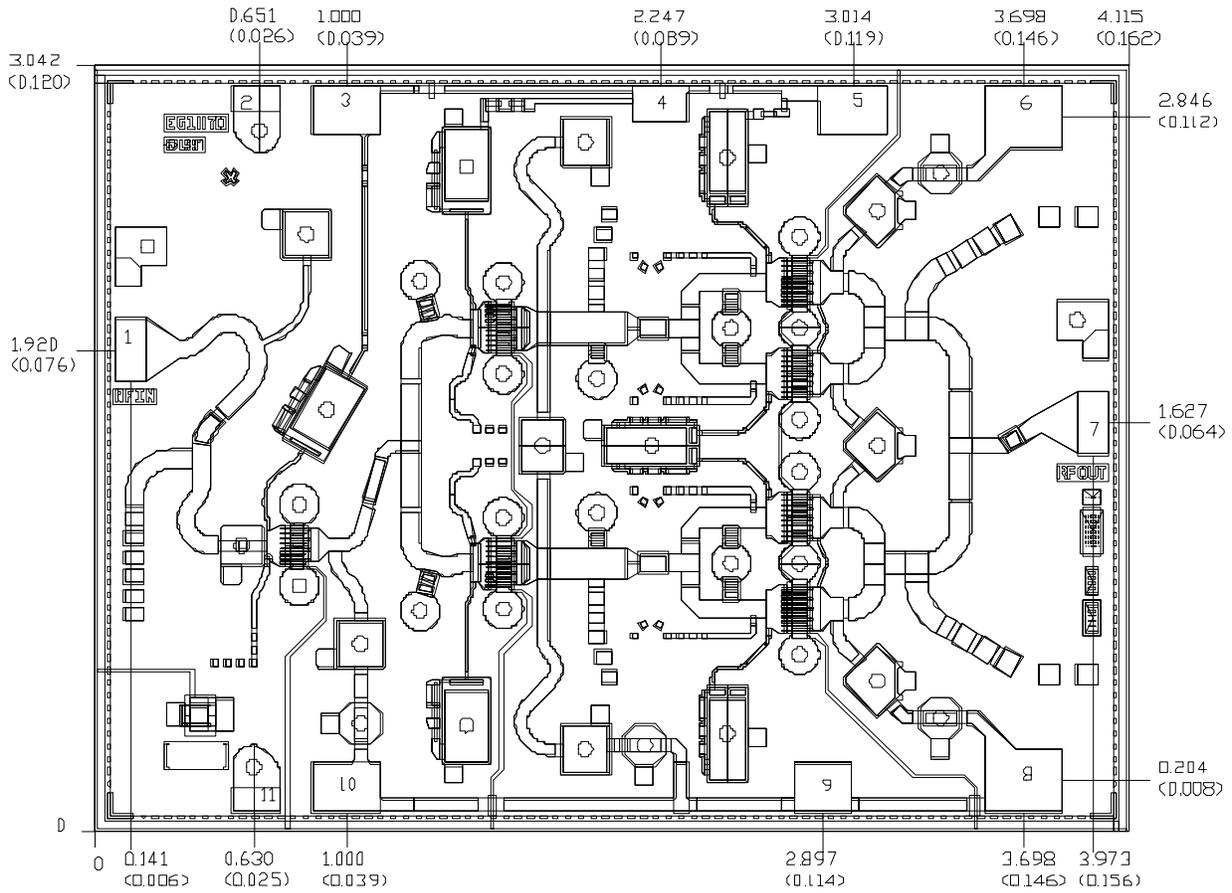
**Statistical Performance Summary**



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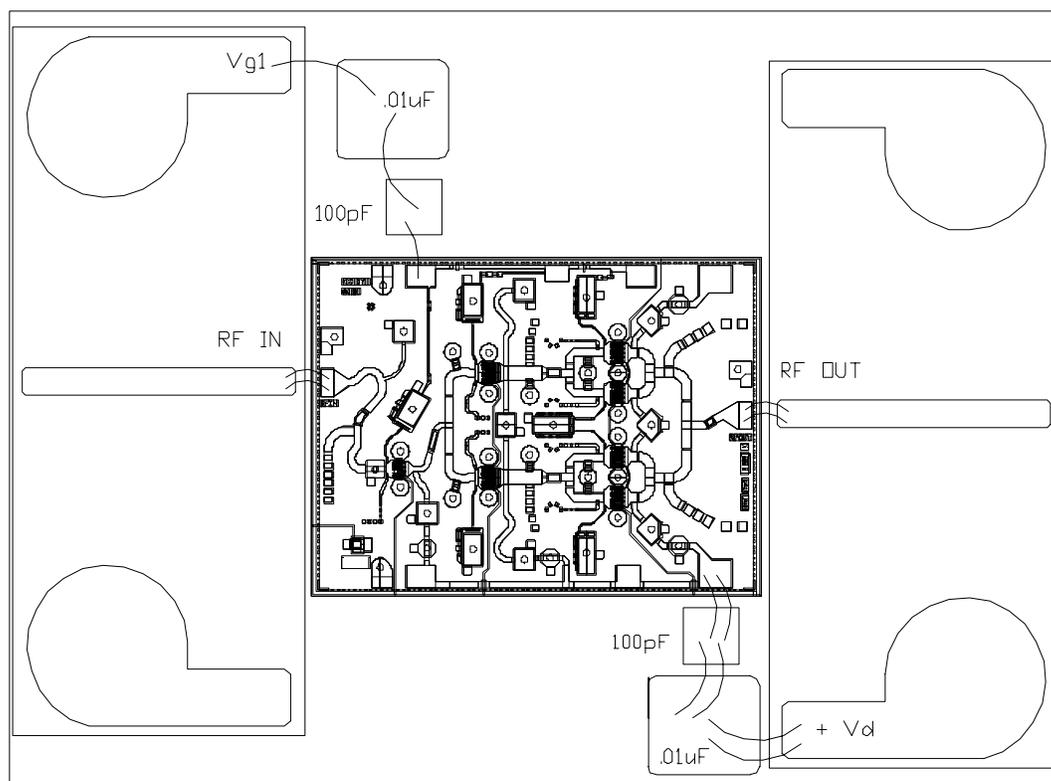


**Mechanical Characteristics**



Units: millimeters (inches)  
 Thickness: 0.1016 (0.004) (reference only)  
 Chip edge to bond pad dimensions are shown to center of bond pad.  
 Chip size tolerance: +/- 0.0508 (0.002)

Bond Pad #1 (RF Input)	0.120 x 0.249	(0.005 x 0.010)
Bond Pad #2 (Gnd)	0.190 x 0.100	(0.008 x 0.004)
Bond Pad #3 (Vg1)	0.270 x 0.195	(0.011 x 0.008)
Bond Pad #4 (Vg2)	0.220 x 0.144	(0.009 x 0.006)
Bond Pad #5 (Vg3)	0.270 x 0.195	(0.011 x 0.008)
Bond Pad #6 & #8 (Vd3)	0.306 x 0.250	(0.012 x 0.010)
Bond Pad #7 (RF Output)	0.120 x 0.249	(0.005 x 0.010)
Bond Pad #9 (Vd2)	0.220 x 0.195	(0.009 x 0.008)
Bond Pad #10 (Vd1)	0.270 x 0.195	(0.011 x 0.008)
Bond Pad #11 (Gnd)	0.190 x 0.100	(0.008 x 0.004)



**Chip Assembly and Bonding Diagram**

Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C