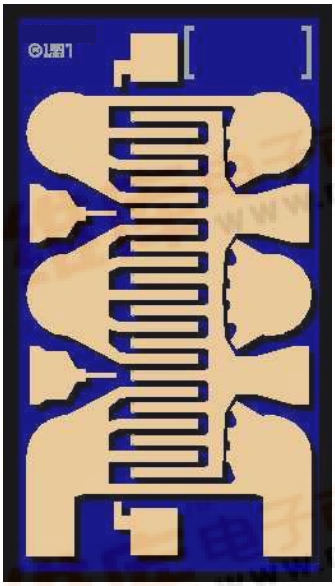
TriQuint SEMICONDUCTOR

Product Data Sheet
March 31, 2003

2.4 mm Discrete HFET

TGF4240-SCC



Key Features and Performance

- 2400 µm x 0.5 µm HFET
- Nominal Pout of 31.5 dBm at 8.5 GHz
- Nominal Gain of 10.0 dB at 8.5 GHz
- Nominal PAE of 56 % at 8.5 GHz
- Frequency Range: DC - 12 GHz
- Suitable for high reliability applications
- 0.6 x 1.0 x 0.1 mm (0.024 x 0.040 x 0.004 in)

Primary Applications

- Cellular Base Stations
- High-reliability space
- Military

DESCRIPTION

The TriQuint TGF4240-SCC is a single gate 2.4 mm Discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high-efficiency power applications up to 12 GHz in Class A and Class AB operation.

Typical performance at 8.5 GHz is 31.5 dBm power output, 10 dB Gain, and 56% PAE.

Bond-pad and backside metalization is gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire-bonding processes.

The TGF4240-SCC is readily assembled using automatic equipment.

TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER 1/	VALUE	NOTES
V_{DS}	Drain to Source Voltage	12 V	
V_{GS}	Gate to Source Voltage Range	0 to -5.0 Volts	
P_D	Power Dissipation	TBD	2/
T_{CH}	Operating Channel Temperature	150°C	3/, 4/
T_{STG}	Storage Temperature	-65 to 200°C	
T_M	Mounting Temperature (30 seconds)	320°C	

1/ These ratings represent the maximum values for this device. Stresses beyond those listed under "Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "DC Probe Characteristics" is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

2/ When operated at this bias condition with a base plate temperature of 70 ^{0}C, the median life is reduced from TBD to TBD hours.

3/ Junction temperature will directly affect the device Mean Time to Failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels

4/ These ratings apply to each individual FET

TABLE II
DC PROBE CHARACTERISTICS
(T_A = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note
I_{DSS}	Saturated Drain Current	--	588	--	mA	1/
G_M	Transconductance	--	396	--	mS	1/
V_P	Pinch-off Voltage	1	1.85	3	V	2/
V_{BGS}	Breakdown Voltage Gate-Source	17	22	30	V	2/
V_{BGD}	Breakdown Voltage Gate-Drain	17	22	30	V	2/

1/ Total for two FETS
2/ V_P, V_{BGS}, and V_{BGD} are negative.

TABLE III
ELECTRICAL CHARACTERISTICS
(T_A = 25 °C, Nominal)
Bias Conditions: Vd = 8 V, Id = 100 mA

Symbol	Parameter	Typical	Unit
Pout	Output Power	31.5	dBm
Gp	Power Gain	10	dB
PAE	Power Added Efficiency	56	%

TABLE IV
THERMAL INFORMATION*

Parameter	Test Conditions	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 8 V I_D = 100 mA Pdiss = TBD	TBD	TBD	TBD

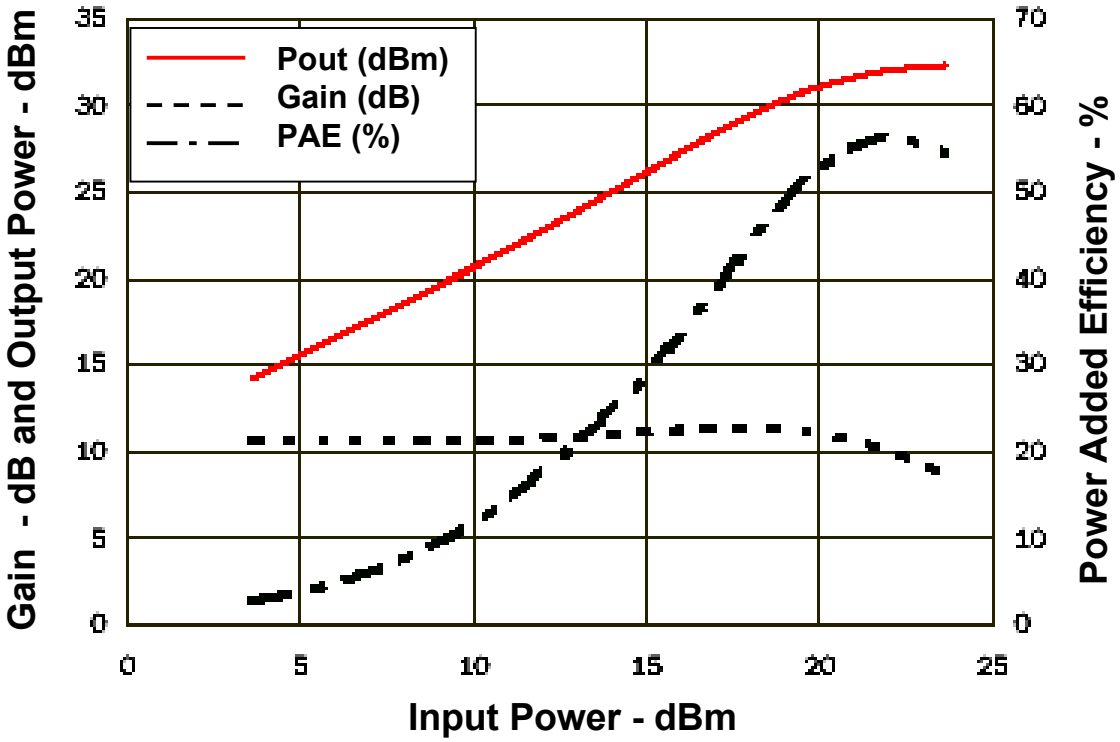
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

* The thermal information is a result of a detailed thermal model.

TYPICAL PERFORMANCE

Bias Conditions: Freq = 8.5 GHzm Vd = 8V, Id = 100mA

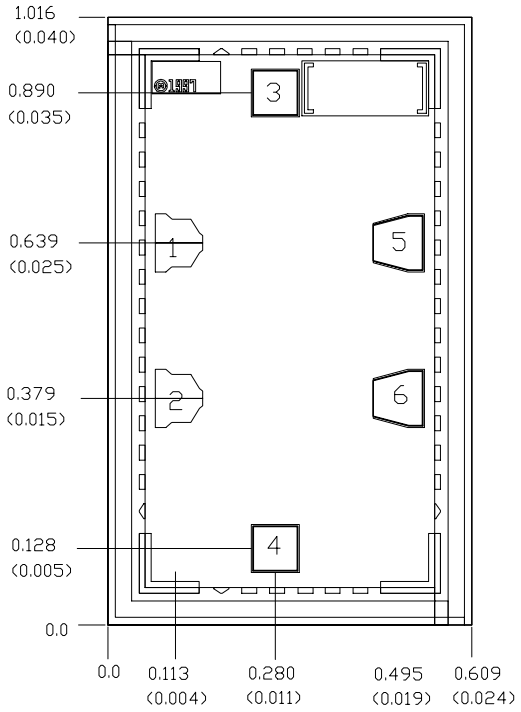
(T_A = 25 °C, Nominal)



Unmatched Modeled S-Parameter Data for the TGF4240-SCC

FREQ (GHz)	S11 MAG dB	ANG (°) deg	S21 MAG dB	ANG (°) deg	S12 MAG dB	ANG (°) deg	S22 MAG dB	ANG (°) deg
0.5	-0.336	-62.251	20.588	144.748	-31.032	56.129	-13.423	-116.099
1.0	-0.642	-100.759	17.874	122.599	-27.740	36.651	-10.066	-135.107
1.5	-0.803	-122.281	15.374	109.317	-26.741	25.761	-8.938	-144.013
2.0	-0.881	-135.190	13.286	100.360	-26.363	19.133	-8.381	-148.390
2.5	-0.920	-143.616	11.538	93.616	-26.216	14.702	-8.008	-150.580
3.0	-0.940	-149.505	10.046	88.120	-26.175	11.520	-7.705	-151.636
3.5	-0.948	-153.846	8.747	83.392	-26.194	9.118	-7.428	-152.083
4.0	-0.950	-157.179	7.598	79.175	-26.255	7.243	-7.161	-152.203
4.5	-0.948	-159.826	6.565	75.316	-26.343	5.750	-6.898	-152.157
5.0	-0.942	-161.984	5.626	71.723	-26.452	4.553	-6.638	-152.041
5.5	-0.934	-163.785	4.764	68.337	-26.580	3.595	-6.381	-151.912
6.0	-0.925	-165.317	3.966	65.118	-26.726	2.843	-6.128	-151.804
6.5	-0.914	-166.642	3.221	62.039	-26.886	2.275	-5.879	-151.737
7.0	-0.902	-167.805	2.522	59.080	-27.058	1.876	-5.636	-151.720
7.5	-0.890	-168.839	1.862	56.227	-27.242	1.639	-5.400	-151.757
8.0	-0.877	-169.769	1.236	53.470	-27.436	1.559	-5.172	-151.850
8.5	-0.863	-170.615	0.640	50.801	-27.639	1.634	-4.951	-151.995
9.0	-0.849	-171.390	0.071	48.214	-27.851	1.866	-4.739	-152.191
9.5	-0.835	-172.108	-0.475	45.704	-28.068	2.256	-4.535	-152.432
10	-0.821	-172.776	-1.000	43.267	-28.291	2.807	-4.340	-152.714
10.5	-0.807	-173.404	-1.506	40.901	-28.515	3.521	-4.154	-153.033
11.0	-0.793	-173.996	-1.995	38.603	-28.740	4.403	-3.976	-153.385
11.5	-0.779	-174.558	-2.468	36.371	-28.964	5.454	-3.807	-153.764
12.0	-0.765	-175.093	-2.928	34.202	-29.186	6.679	-3.645	-154.169
12.5	-0.751	-175.607	-3.374	32.095	-29.401	8.076	-3.491	-154.594
13.0	-0.737	-176.100	-3.808	30.048	-29.606	9.646	-3.345	-155.037
13.5	-0.724	-176.576	-4.232	28.060	-29.800	11.386	-3.206	-155.494
14.0	-0.711	-177.036	-4.645	26.131	-29.979	13.288	-3.074	-155.964

Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond Pad #1 (gate)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #2 (gate)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #3 (gate)*	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #4 (gate)*	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #5 (drain)	0.083 x 0.077 (0.003 x 0.003)
Bond Pad #6 (drain)	0.083 x 0.077 (0.003 x 0.003)

Minimum connections to Bond pads 1 to 2 and 5 to 6.
Sources are connected to backside metalization.

*Alternate gate pads used for paralleling TGF4240's or for multiple gate wires.

NOTE: Gate bias supplies should be designed to sink or source gate current. The magnitude and direction of the gate current is a function of bias point, load impedence, and drive level.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handing, assembly and test.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

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Note: Die are shipped in gel pack unless otherwise specified.