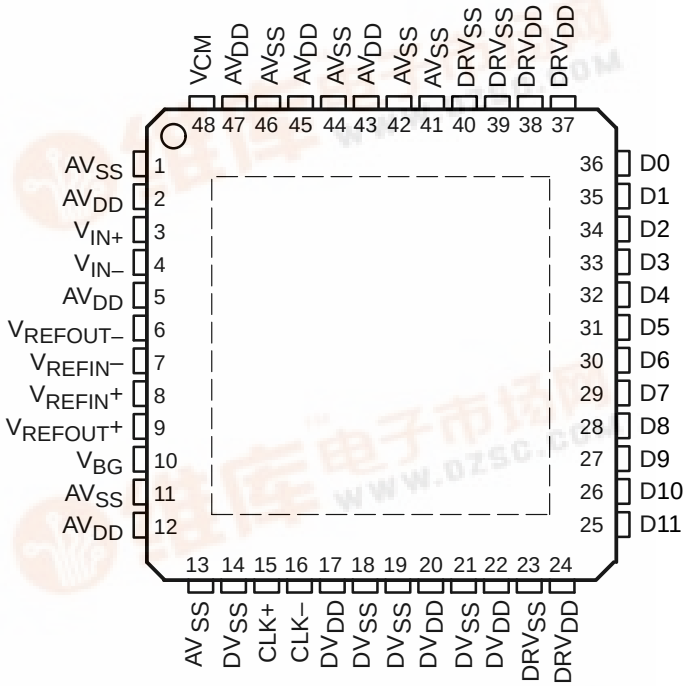
THS1240
12-BIT 40 MSPS IF SAMPLING COMMUNICATIONS ANALOG-TO-DIGITAL CONVERTER

SLAS279D – JUNE 2000 – REVISED JANUARY 2001

features

- 40-MSPS Sample Rate
- 12-Bit Resolution
- No Missing Codes
- On-Chip Sample and Hold
- 77-dB Spurious Free Dynamic Range at f_{IN} = 15.5 MHz
- 5-V Analog and Digital Supply
- 3-V and 5-V CMOS Compatible Digital Output
- 10.4 Bit ENOB at f_{IN} = 31 MHz
- 65 dB SNR at f_{IN} = 15.5 MHz
- 120-MHz Bandwidth
- Internal or External Reference
- Buffered Differential Analog Input
- 2s Complement Digital Outputs
- Typical 380 mW Power Consumption
- Single-Ended or Differential Low-Level Clock Input

48 PHP PACKAGE
(TOP VIEW)



applications

- Wireless Local Loop
- Wireless Internet Access
- Cable Modem Receivers
- Medical Ultrasound
- Magnetic Resonant Imaging

description

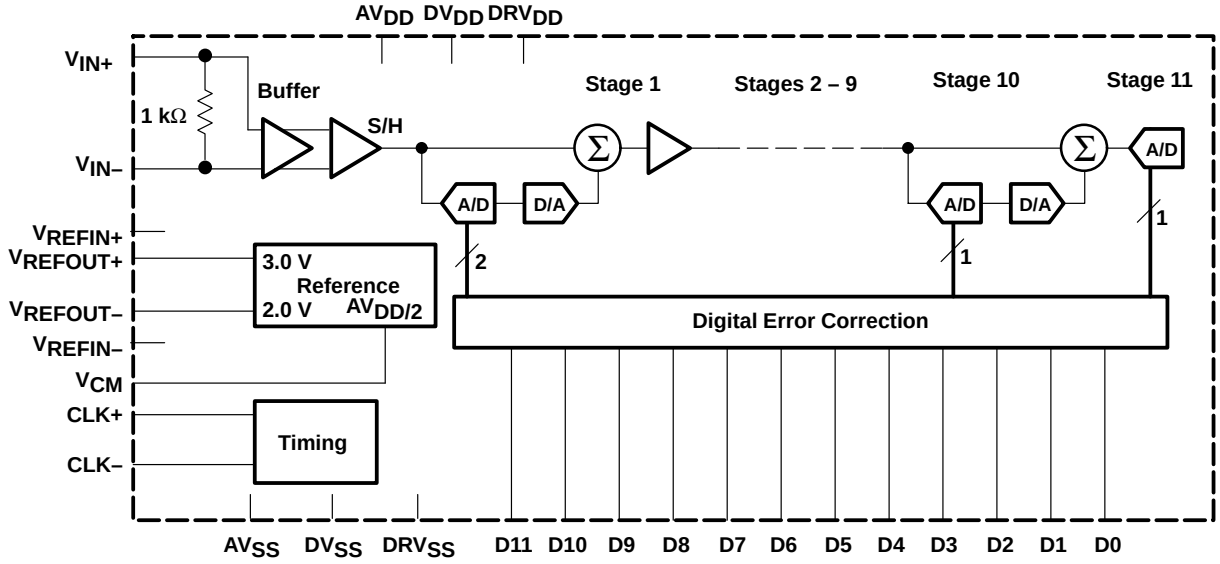
The THS1240 is a high-speed low noise 12-bit CMOS pipelined analog-to-digital converter. A differential sample and hold minimizes even order harmonics and allows for a high degree of common mode rejection at the analog input. A buffered analog input enables operation with a constant analog input impedance, and prevents transient voltage spikes from feeding backward to the analog input source. Full temperature DNL performance allows for industrial application with the assurance of no missing codes. The THS1240 can operate with either internal or external references. Internal reference usage selection is accomplished simply by externally connecting reference output terminals to reference input terminals.

AVAILABLE OPTIONS

T_A	PACKAGE
	48-TQFP (PHP)
–40°C to 85°C	THS1240I
0°C to 70°C	THS1240C

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	2, 5, 12, 43, 45, 47	I	Analog power supply
AV_{SS}	1, 11, 13, 41, 42, 44, 46	I	Analog ground return for internal analog circuitry
CLK+	15	I	Clock input
CLK–	16	I	Complementary clock input
D11–D0	25–36	O	Digital data output bits; LSB= D0, MSB = D11 (2s complement output format)
DRV_{DD}	24, 37, 38	I	Digital output driver supply
DRV_{SS}	23, 39, 40	I	Digital output driver ground return
DV_{DD}	17, 20, 22	I	Positive digital supply
DV_{SS}	18, 19, 21	I	Digital ground return
V_{BG}	10	O	Band gap reference. Bypass to ground with a 1-μF and a 0.01-μF chip capacitor.
V_{CM}	48	O	Common mode voltage output. Bypass to ground with a 0.1-μF and a 0.01-μF chip capacitor.
V_{IN+}	3	I	Analog signal input
$V_{IN–}$	4	I	Complementary analog signal input
$V_{REFIN–}$	7	I	External reference input low
V_{REFIN+}	8	I	External reference input high
$V_{REFOUT+}$	9	O	Internal reference output. Compensate with a 1-μF and a 0.01-μF chip capacitor.
$V_{REFOUT–}$	6	O	Internal reference output. Compensate with a 1-μF and a 0.01-μF chip capacitor.

functional description

The THS1240 uses a differential pipeline architecture and assures no missing codes over the full operating temperature range. The device uses a 1 bit per stage architecture in order to achieve the highest possible bandwidth. The differential analog inputs are terminated with a 1-kΩ resistor. The inputs are then fed to a unity gain buffer followed by the S/H (sample and hold) stage. This S/H stage is a switched capacitor operational amplifier-based circuit, see Figure 3. The pipeline is a typical 1 bit per stage pipeline as shown in the functional block diagram. The digital output of the 12 stages is sent to a digital correction logic block which then outputs the final 12 bits.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: AV_{DD} . . . . . –0.5 V to 7 V
DV_{DD} . . . . . –0.5 V to 7 V
DRV_{DD} . . . . . –0.5 V to 7 V
Voltage between AV_{SS} and DV_{SS} and DRV_{SS} . . . . . –0.3 V to 0.5 V
Voltage between DRV_{DD} and DV_{DD} . . . . . –0.5 V to 5 V
Voltage between AV_{DD} and DV_{DD} . . . . . –0.5 V to 5 V
Digital data output . . . . . –0.3 V to DV_{DD} +0.3 V
CLK peak input current, $I_{p(CLK)}$ . . . . . 20 mA
Peak total input current (all inputs), I_p . . . . . –30 mA
Operating free-air temperature range, T_A: THS1240C . . . . . 0°C to 70°C
THS1240I . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

† Stresses beyond those listed *under absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Sample rate		1		40	MSPS
Analog supply voltage, AV_{DD}		4.75	5	5.25	V
Digital supply voltage, DV_{DD}		4.75	5	5.25	V
Digital output driver supply voltage, DRV_{DD}		3	3.3	5.25	V
CLK + high level input voltage, V_{IH}‡		3.5	5	5.25	V
CLK + low-level input voltage, V_{IL}‡		0		1.5	V
CLK pulse-width high, $t_{p(H)}$		10	12.5		ns
CLK pulse-width low, $t_{p(L)}$		10	12.5		ns
Operating free-air temperature range, T_A	THS1240C	0		70	°C
	THS1240I	–40		85	

‡ CLK– Input tied to ground with 0.01 μF capacitor for single-ended clock source.

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 5 V, DRV_{DD} = 3.3 V, internal references, CLK = 40 MHz, single-ended clock source at 40 MHz with 50% duty cycle (unless otherwise noted)

dc accuracy

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DNL	Differential nonlinearity	f_{IN} = 15.5 MHz	–1	±0.6	1.25	LSB
	No missing codes			Assured		
INL	Integral nonlinearity	f_{IN} = 15.5 MHz		±2		LSB
E_O	Offset error	$V(V_{IN+}) = V(V_{IN}) = V_{CM}$		14	70	mV
E_G	Gain error			–7	–10	%FSR

† All typical values are at T_A = 25°C.

power supply

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I(AV_{DD})$	Analog supply current	$V(V_{IN}) = (V_{CM})$		73	110	mA
$I(DV_{DD})$	Digital supply current	$V(V_{IN}) = (V_{CM})$		2	4	mA
$I(DRV_{DD})$	Output driver supply current‡	$V(V_{IN}) = (V_{CM})$		2	7	mA
P_D	Power dissipation	$V(V_{IN}) = (V_{CM})$		380		mW

† All typical values are at T_A = 25°C.
‡ 15 pF load on digital outputs

reference

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{REFOUT-}$	Negative reference output voltage		1.9	2	2.1	V
$V_{REFOUT+}$	Positive reference output voltage		2.9	3	3.1	V
V_{REFIN-}	External reference supplied			2		V
V_{REFIN+}	External reference supplied			3		V
$V(V_{CM})$	Common mode output voltage			$AV_{DD}/2$		V
$I(V_{CM})$	Common mode output current			80		µA

† All typical values are at T_A = 25°C.

analog input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
R_I	Differential input resistance			1		kΩ
C_I	Differential input capacitance			4		pF
V_I	Analog input common mode range			V_{CM} ±0.05		V
V_{ID}	Differential input voltage range			2		Vp-p
BW	Analog input bandwidth (large signal)	–3 dB		120		MHz

† All typical values are at T_A = 25°C.

digital outputs

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –50 µA	$0.8DRV_{DD}$			V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA			$0.2DRV_{DD}$	V_{DD}
C_L	Output load capacitance				15	pF

† All typical values are at T_A = 25°C.

ac specifications over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 5 V, DRV_{DD} = 3.3 V, internal references, CLK = 40 MHz, analog input at –2 dBFS, single-ended clock source at 40 MHz with 50% duty cycle (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 2.2 MHz		64.6		dB
		f_{IN} = 15.5 MHz		64		
		f_{IN} = 15.5 MHz, $V_{(IN)}$ = –0.5 dBFS	63	65.5		
		f_{IN} = 31 MHz		64		
		f_{IN} = 70 MHz		64		
SINAD	Signal-to-noise and distortion	f_{IN} = 2.2 MHz		63.3		dB
		f_{IN} = 15.5 MHz		64		
		f_{IN} = 15.5 MHz, $V_{(IN)}$ = –0.5 dBFS	62	64.5		
		f_{IN} = 31 MHz		63.2		
		f_{IN} = 70 MHz		55.7		
ENOB	Effective number of bits	f_{IN} = 15.5 MHz		10.2		bits
		f_{IN} = 15.5 MHz, $V_{(IN)}$ = –0.5 dBFS	10	10.4		
THD	Total harmonic distortion	f_{IN} = 15.5 MHz		–72	–68	dBc
		f_{IN} = 15.5 MHz, $V_{(IN)}$ = –0.5 dBFS		–71		
SFDR	Spurious-free dynamic range	f_{IN} = 2.2 MHz		73		dBc
		f_{IN} = 15.5 MHz	70	77		
		f_{IN} = 15.5 MHz, $V_{(IN)}$ = –0.5 dBFS		72		
		f_{IN} = 31 MHz		77		
		f_{IN} = 70 MHz		59.6		
2^{nd} Harmonic	Distortion	f_{IN} = 2.2 MHz		82		dBc
		f_{IN} = 15.5 MHz		–87	–70	
		f_{IN} = 31 MHz		–77		
		f_{IN} = 70 MHz		–60.5		
3^{rd} Harmonic	Distortion	f_{IN} = 2.2 MHz		–73		dBc
		f_{IN} = 15.5 MHz		–80.4	–70	
		f_{IN} = 31 MHz		–77		
		f_{IN} = 70 MHz		–60		
Two tone SFDR		F1 = 14.9 MHz, F2 = 15.6 MHz, Analog inputs at – 8 dBFS each		72		dBc

† All typical values are at T_A = 25°C.

operating characteristics over recommended operating conditions, AV_{DD} = DV_{DD} = 5 V, DRV_{DD} = 3.3 V

switching specifications

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Aperture delay, $t_{d(A)}$			120		ps
Aperture jitter			1		ps RMS
Output delay $t_{d(O)}$, after falling edge of CLK+	Digital outputs driving a 15 pF load each			13	ns
Pipeline delay $t_{d(PIPE)}$			6.5		CLK Cycle

† All typical values are at T_A = 25°C.

definitions of specifications

analog bandwidth
The analog input frequency at which the spectral power of the fundamental frequency of a large input signal is reduced by 3 dB.

aperture delay
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

aperture uncertainity (jitter)
The sample-to-sample variation in aperture delay

differential nonlinearity
The deviation of any output code from the ideal width of 1 LSB.

integral nonlinearity
The deviation of the transfer function from an end-point adjusted reference line measured in fractions of 1 LSB. Also the integral of the DNL curve.

clock pulse width/duty cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in logic 1 state to achieve rated performance; pulse width low is the minimum time clock pulse should be left in low state. At a given clock rate, these specs define acceptable clock duty cycles.

offset error
The difference between the analog input voltage at which the ADC output changes from mid-scale to 1 LSB above mid-scale, and the ideal voltage at which this transition should occur.

gain error
The difference between the analog input voltage at which the ADC output changes from full-scale to 1 LSB below full scale, and the ideal voltage at which this transition should occur, minus the offset error

$$\text{Gain Error} = 100\% \times \frac{2 - \left(V_{IN+} - V_{IN\_}\right)}{2\ V} \text{ @Code 4096}$$

total harmonic distortion
The ratio of the power of the fundamental to a given harmonic component reported in dBc.

output delay
The delay between the 50% point of the falling edge of the clock and the time when all output data bits are within valid logic levels (not including pipeline delay).

signal-to-noise-and distortion (SINAD)
When tested with a single tone, the ratio of the signal power to the sum of the power of all other spectral components, excluding dc, referenced to full scale.

signal-to-noise ratio (SNR)
When tested with a single tone, the ratio of the signal power to the sum of the power of all other power spectral components, excluding dc and the first 9 harmonics, referenced to full scale.

effective number of bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the effective number of bits, using the following formula,

$$\text{ENOB} = \frac{(\text{SINAD} - 1.76)}{6.02}$$

spurious-free dynamic range (SFDR)
The ratio of the signal power to the power of the worst spur, excluding dc. The worst spurious component may or may not be a harmonic. The ratio is reported in dBc (that is, degrades as signal levels are lowered).

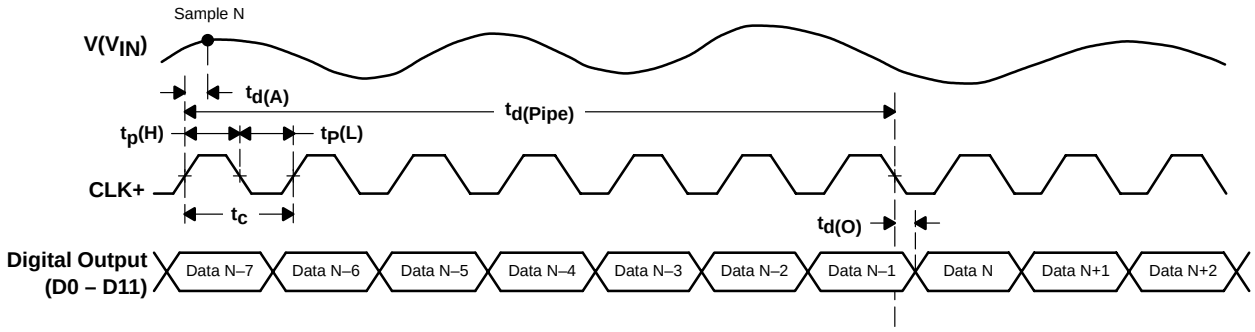


Figure 1. Timing Diagram

equivalent circuits

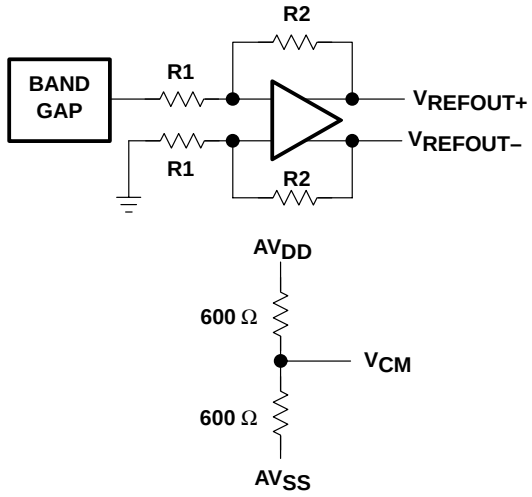


Figure 2. References

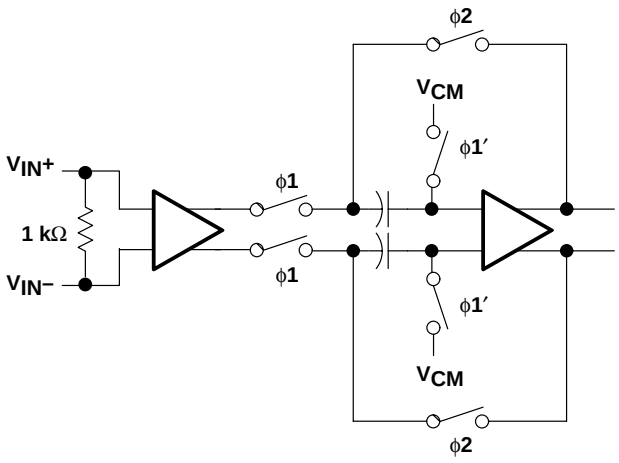


Figure 3. Analog Input Stage

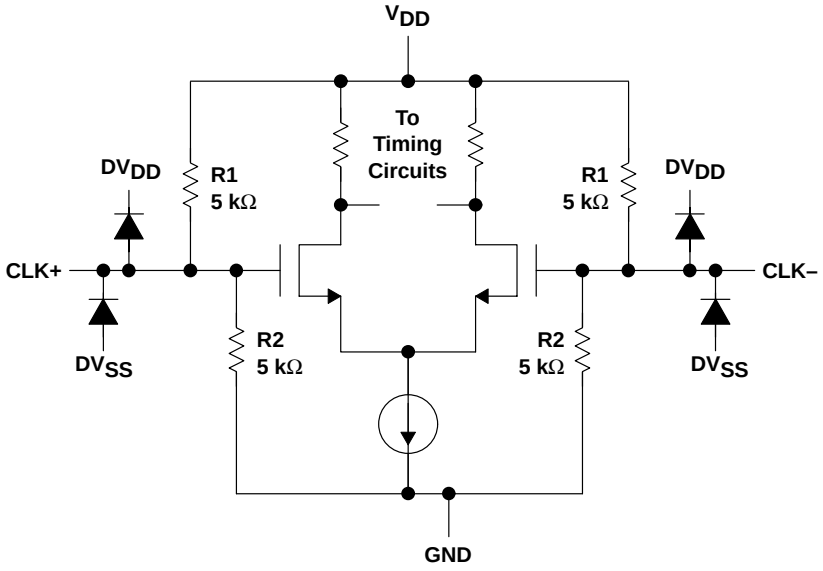


Figure 4. Clock Inputs

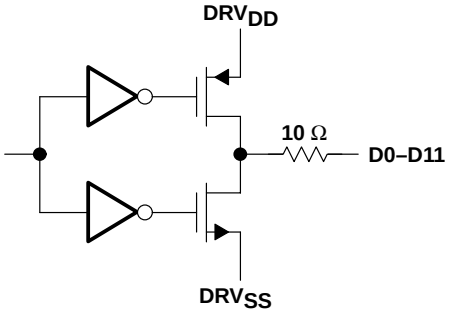


Figure 5. Digital Outputs

APPLICATION INFORMATION

using the THS1240 references

The option of internal or external reference is provided by allowing for an external connection of the internal reference to the reference inputs. This type of reference selection offers the lowest noise possible by not relying on any active switch to make the selection. Compensating each reference output with a 1-µF and 0.01-µF chip capacitor is required as shown in Figure 6. The differential analog input range is equal to 2 ($V_{REFOUT+}$ − $V_{REFOUT–}$). When using external references, it is best to decouple the reference inputs with a 0.1-µF and 0.01-µF chip capacitor as shown in Figure 7.

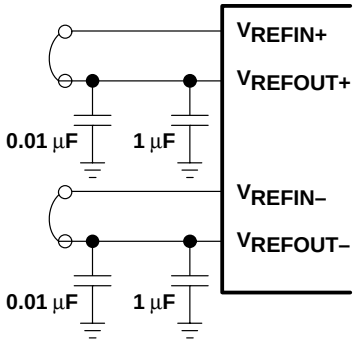


Figure 6. Internal Reference Usage

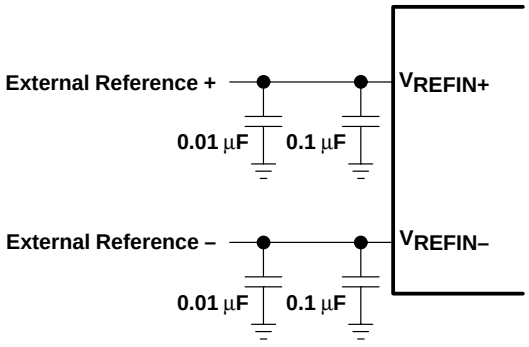


Figure 7. External Reference Usage

using the THS1240 clock input

The THS1240 clock input can be driven with either a differential clock signal or a single ended clock input with little or no difference in performance between the single-ended and differential-input configurations. The common mode of the clock inputs is set internally to $V_{DD}/2$ using 5-kΩ resistors (Figure 4).

The THS1240 clock input requires a common mode voltage or dc component of $V_{DD}/2$. It is possible for the common mode voltage of the clock source to differ from $V_{DD}/2$ by as much as 10% with little or no performance degradation. The clock input should be either a sinewave or a square wave having a 50% duty cycle.

When driven with a single-ended CMOS clock input, it is best to connect the CLK– input to ground with a 0.01 µF capacitor (see Figure 8).

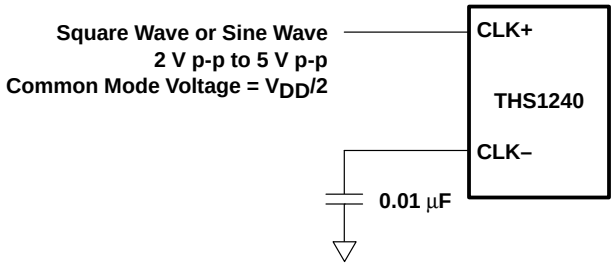


Figure 8. Driving the Clock From a Single-Ended Clock Source

APPLICATION INFORMATION

using the THS1240 clock input (continued)

If the dc component of the input clock differs from $V_{DD}/2$ by more than 10%, it is best to connect the CLK+ input to the clock source through a 0.01 μF capacitor. In this mode, the converter can operate with a clock having a peak-to-peak voltage of as little as 2 V with little or no performance degradation (see Figure 9).

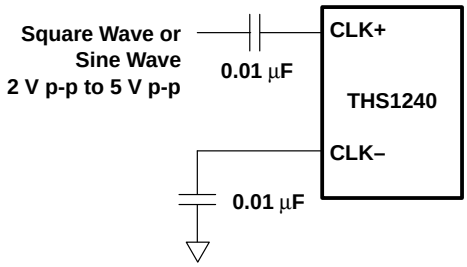


Figure 9. AC-Coupled Single-Ended Clock Input

The THS1240 clock input can also be driven differentially. If the common mode of the clock input is $V_{DD}/2$, then the clock inputs can be driven directly (see Figure 10)

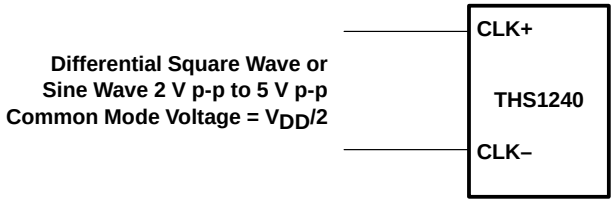


Figure 10. Differential Clock Input

If the clock input is driven differentially with a clock signal having a common mode voltage that is different from $V_{DD}/2$, then it is best to connect both clock inputs to the differential input clock signal with 0.01 μF capacitors (see Figure 11). The differential input swing can vary between 2 V and 5 V with little or no performance degradation.

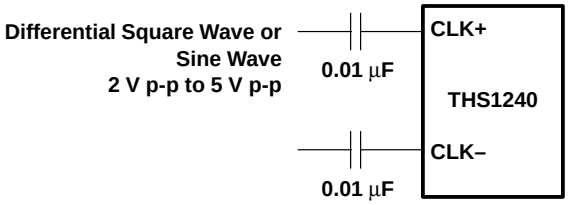


Figure 11. AC-Coupled Differential Clock Input

APPLICATION INFORMATION

using the analog input

The THS1240 obtains optimum performance when the analog signal inputs are driven differentially. The circuit below shows the optimum configuration, see Figure 12. The signal is fed to the primary of an RF transformer. Since the input signal must be biased around the common mode voltage of the internal circuitry, the common mode (V_{CM}) reference from the THS1240 is connected to the center-tap of the secondary. To ensure a steady low noise V_{CM} reference, the best performance is obtained when the V_{CM} output is connected to ground with a 0.1-μF and 0.01-μF low inductance capacitor.

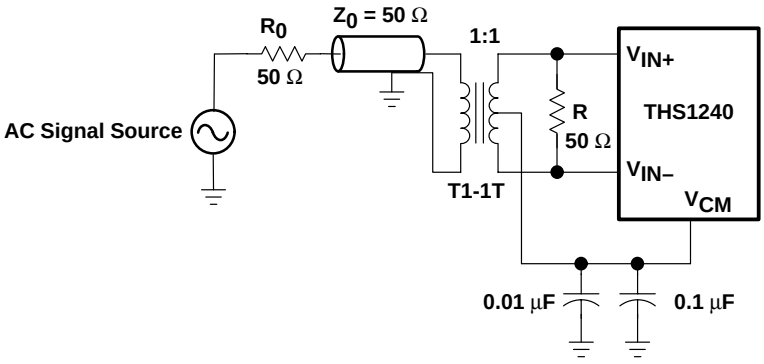


Figure 12. Driving the THS1240 Analog Input With Impedance Matched Transmission Line

When it is necessary to buffer or apply a gain to the incoming analog signal, it is also possible to combine a single-ended amplifier with an RF transformer as shown in Figure 13. For this application, a wide-band current mode feedback amplifier such as the THS3001 is best. The noninverting input to the operational amplifier is terminated with a resistor having an impedance equal to the characteristic impedance of the trace that sources the IF input signal. The single-ended output allows the use of standard passive filters between the amplifier output and the primary. In this case, the SFDR of the operational amplifier is not as critical as that of the A/D converter. While harmonics generated from within the A/D converter fold back into the first Nyquist zone, harmonics generated externally in the operational amplifier can be filtered out with passive filters.

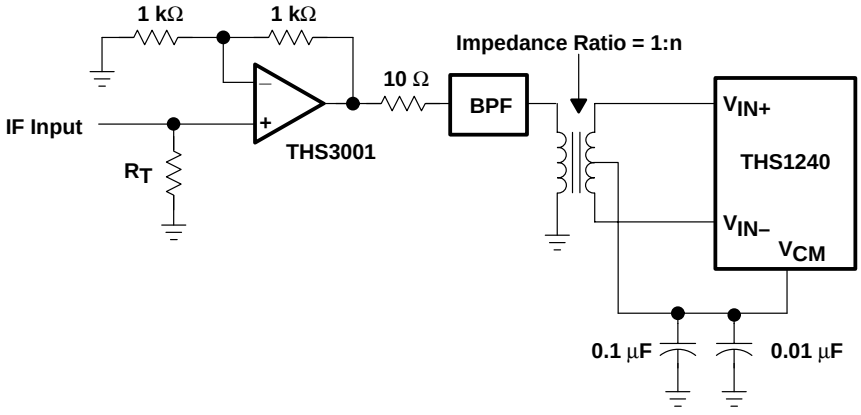


Figure 13. IF Input Buffered With THS3001 Operational Amplifier

APPLICATION INFORMATION

digital outputs

The digital outputs are in 2s complement format and can drive either TTL, 3-V CMOS, or 5-V CMOS logic. The digital output high voltage level is equal to DRV_{DD}. Table 1 shows the value of the digital output bits for full scale analog input voltage, midrange analog input voltage, and negative full scale input voltage. To reduce capacitive loading, each digital output of the THS1240 should drive only one digital input. The CMOS output drivers are capable of handling up to a 15-pF load. For better SNR performance, use 3.3 V for DRV_{DD}. Resistors of 200 Ω in series with the digital output can be used for optimizing SNR performance.

Table 1. Digital Outputs

ANALOG INPUT		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
V_{IN+}	V_{IN-}												
V_{ref+}	V_{ref-}	0	1	1	1	1	1	1	1	1	1	1	1
V_{CM}	V_{CM}	0	0	0	0	0	0	0	0	0	0	0	0
V_{ref-}	V_{ref+}	1	0	0	0	0	0	0	0	0	0	0	0

power supplies

Best performance is obtained when AV_{DD} is kept separate from DV_{DD}. Regulated or linear supplies, as opposed to switched power supplies, must be used to minimize supply noise. It is also recommended to partition the analog and digital components on the board in such a way that the analog supply plane does not overlap with the digital supply plane in order to limit dielectric coupling between the different supplies.

package

The THS1240 is packaged in a small 48-pin quad flat-pack PowerPAD™ package. The die of the THS1240 is bonded directly to copper alloy plate which is exposed on the bottom of the package. Although, the PowerPAD™ provides superior heat dissipation when soldered to a ground land, it is not necessary to solder the bottom of the PowerPAD™ to anything in order to achieve minimum performance levels indicated in this specification over the full recommended operating temperature range.

Only if the device is to be used at ambient temperatures above the recommended operating temperatures, use of the PowerPAD™ is suggested.

The copper alloy plate or PowerPAD™ is exposed on the bottom of the device package for a direct solder attachment to a PCB land or conductive pad. The land dimensions should have minimum dimensions equal to the package dimensions minus 2 mm, see Figure 14.

For a multilayer circuit board, a second land having dimensions equal to or greater than the land to which the device is soldered should be placed on the back of the circuit board (see Figure 15). A total of 9 thermal vias or plated through-holes should be used to connect the two lands to a ground plane (buried or otherwise) having a minimum total area of 3 inches square in 1 oz. copper. For the THS1240 package, the thermal via centers should be spaced at a minimum of 1 mm. The ground plane need not be directly under or centered around the device footprint if a wide ground plane thermal run having a width on the order of the device is used to channel the heat from the vias to the larger portion of the ground plane. The THS1240 package has a standoff of 0.19 mm or 7.5 mils. In order to apply the proper amount of solder paste to the land, a solder paste stencil with a 6 mils thickness is recommended for this device. Too thin a stencil may lead to an inadequate connection to the land. Too thick a stencil may lead to beading of solder in the vicinity of the pins which may lead to shorts. For more information, refer to Texas Instruments literature number SLMA002 *PowerPAD™ Thermally Enhanced Package*.

PowerPAD is a trademark of Texas Instruments.

APPLICATION INFORMATION

package (continued)

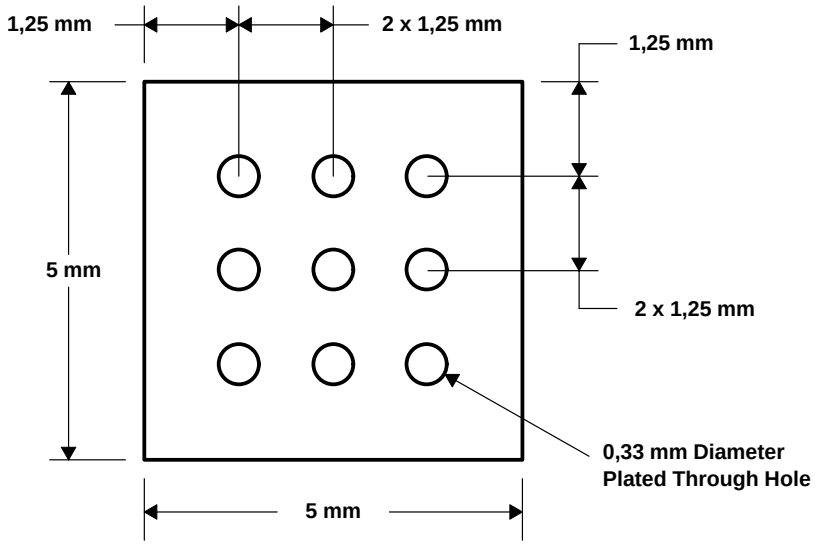


Figure 14. Thermal Land (top view)

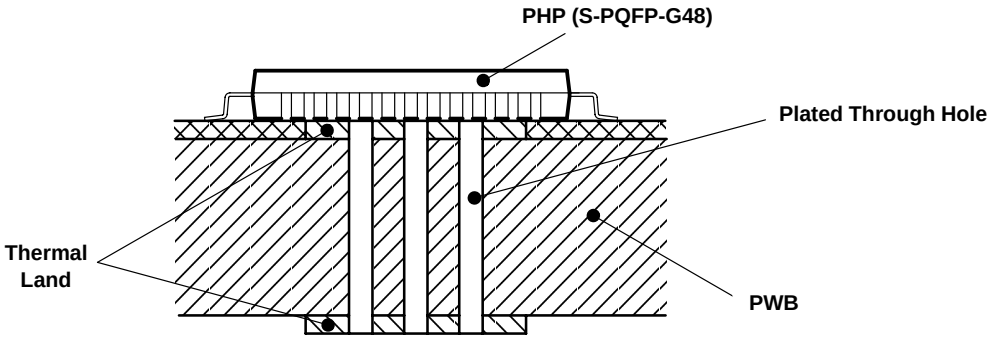


Figure 15. Top and Bottom Thermal Lands With Plated Through Holes (side view)

TYPICAL CHARACTERISTICS

OUTPUT POWER SPECTRUM

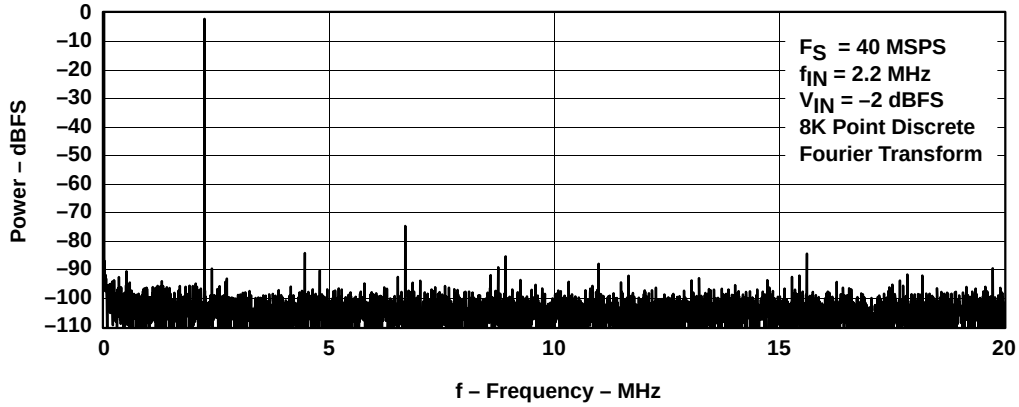


Figure 16

OUTPUT POWER SPECTRUM

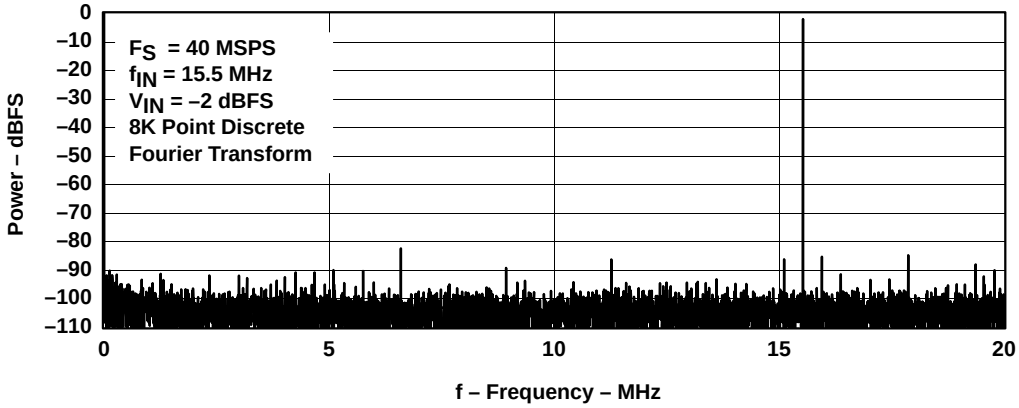


Figure 17

OUTPUT POWER SPECTRUM

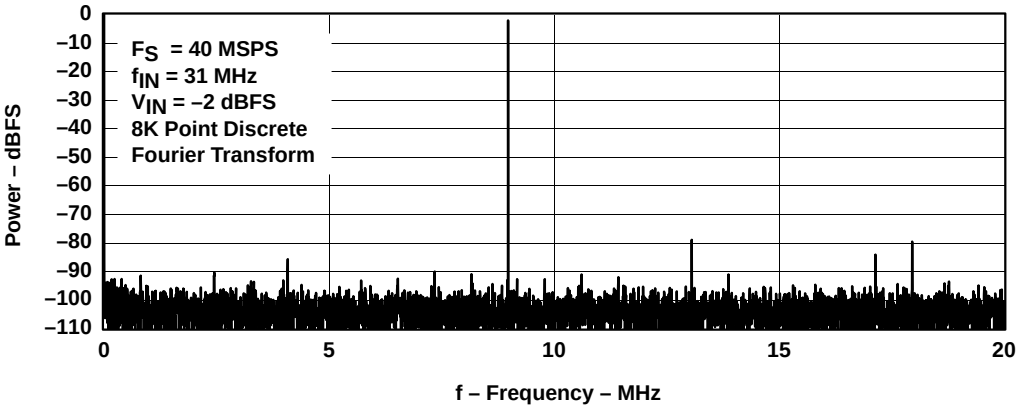


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT POWER SPECTRUM

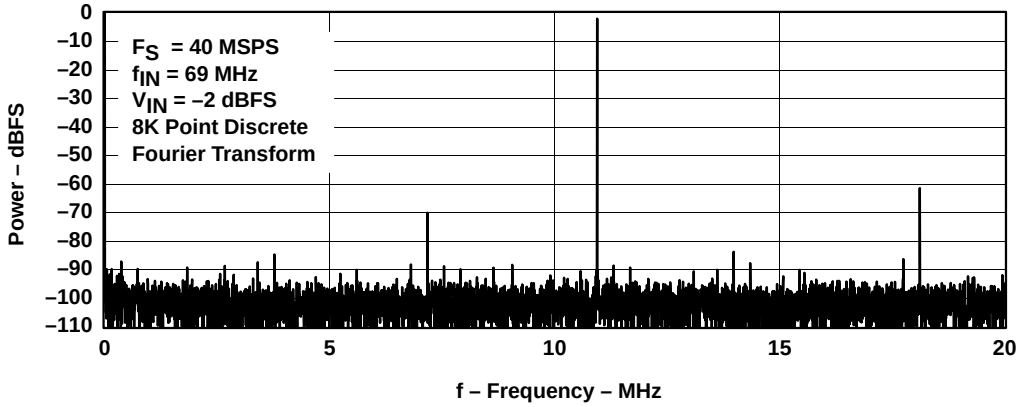


Figure 19

TWO-TONE OUTPUT POWER SPECTRUM

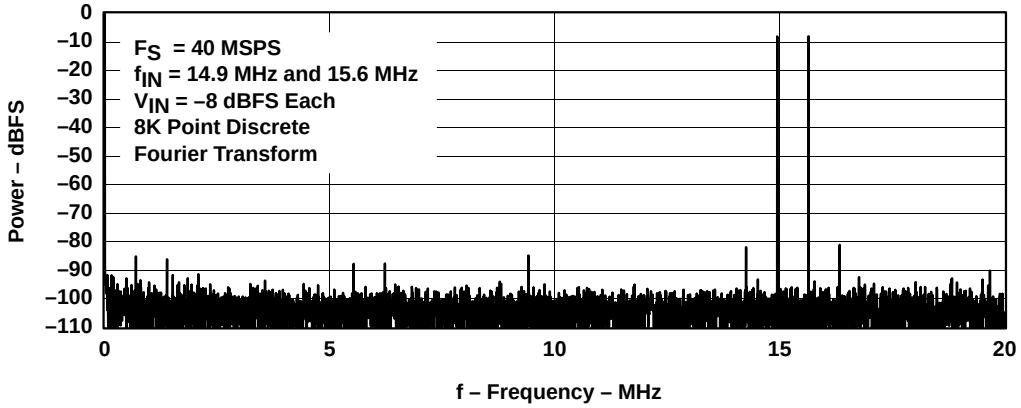


Figure 20

DYNAMIC POWER PERFORMANCE
vs
ANALOG INPUT POWER

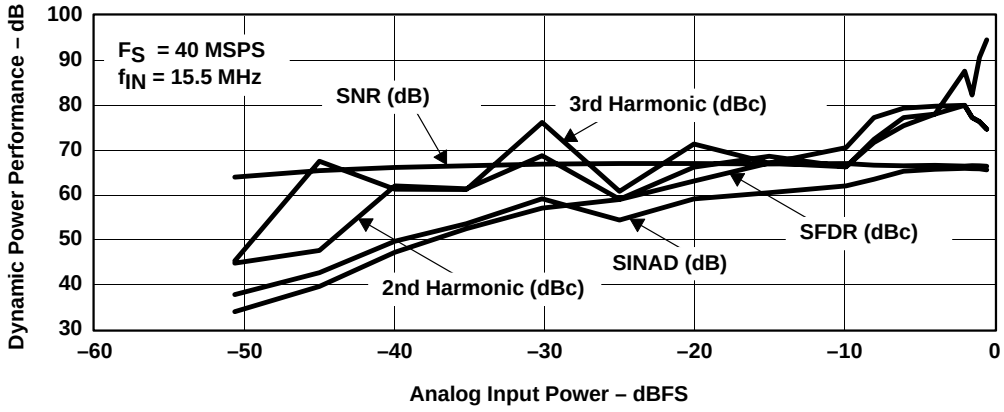


Figure 21

D

TYPICAL CHARACTERISTICS

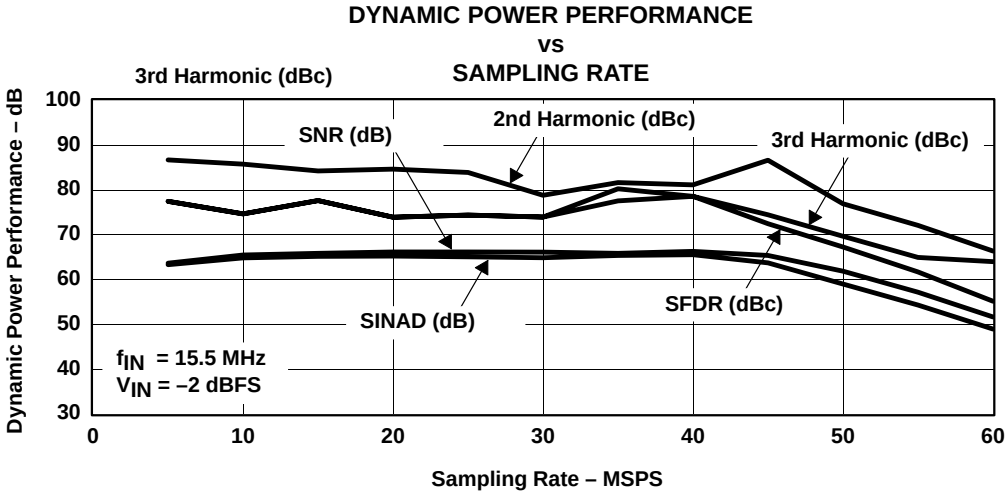


Figure 22

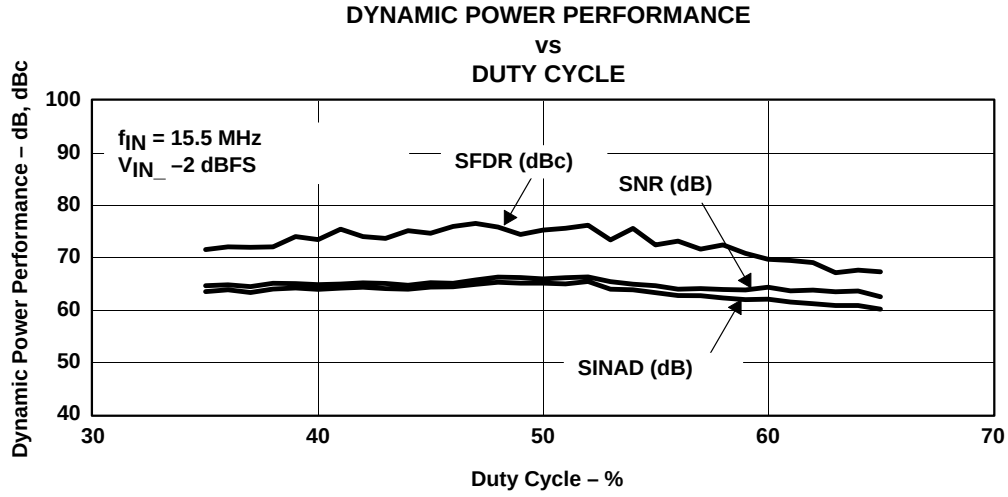


Figure 23

TYPICAL CHARACTERISTICS

DYNAMIC POWER PERFORMANCE
vs
ANALOG INPUT FREQUENCY

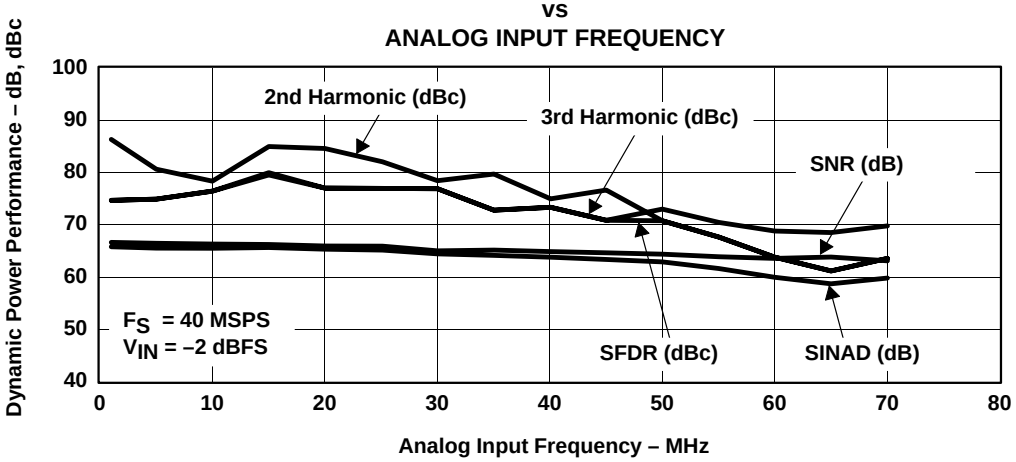


Figure 24

DIFFERENTIAL NONLINEARITY
vs
OUTPUT CODE

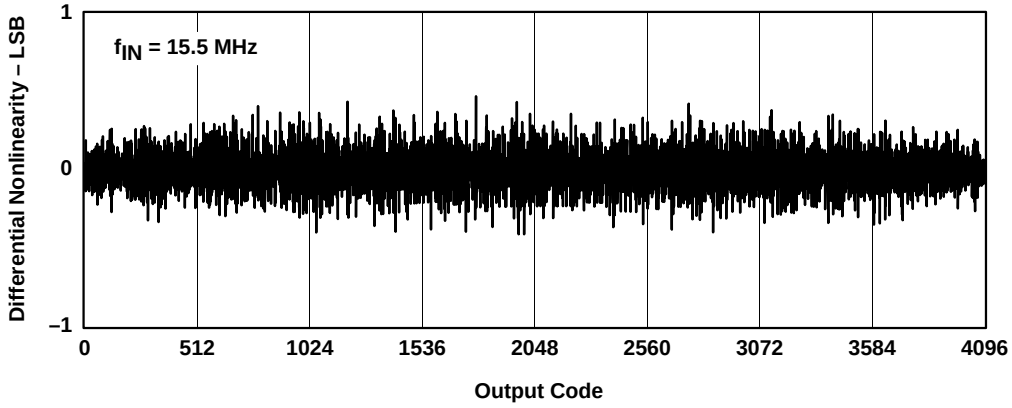


Figure 25

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs OUTPUT CODE

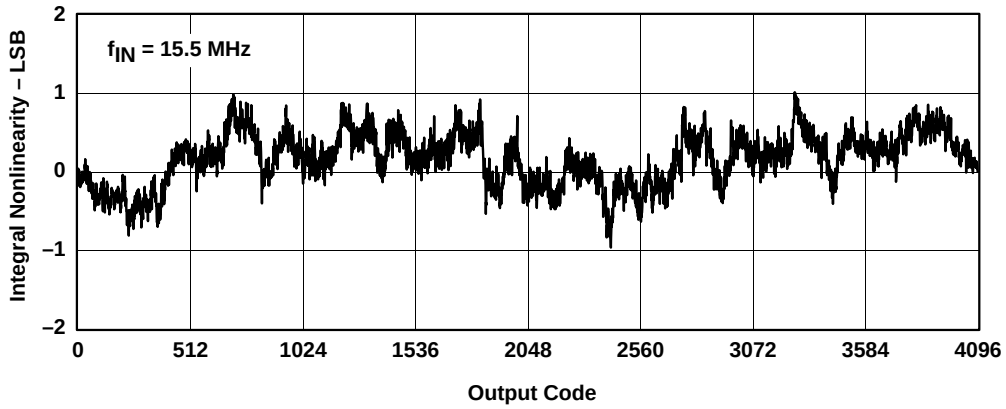


Figure 26

ANALOG INPUT POWER BANDWIDTH

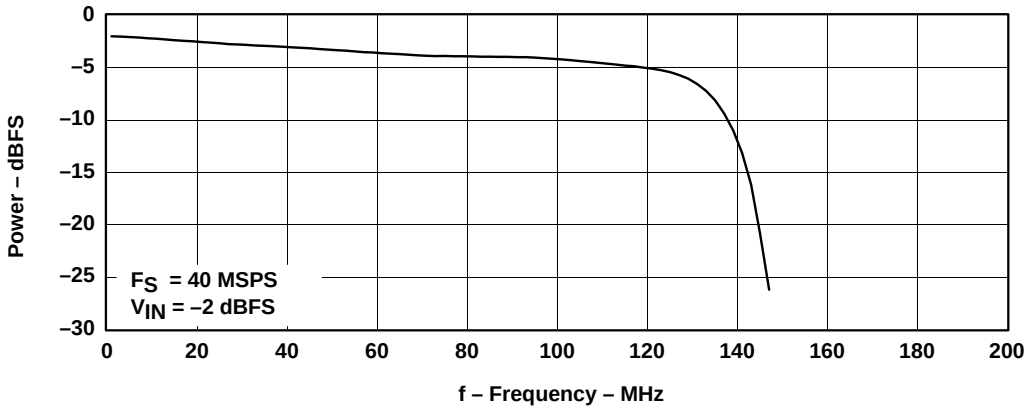
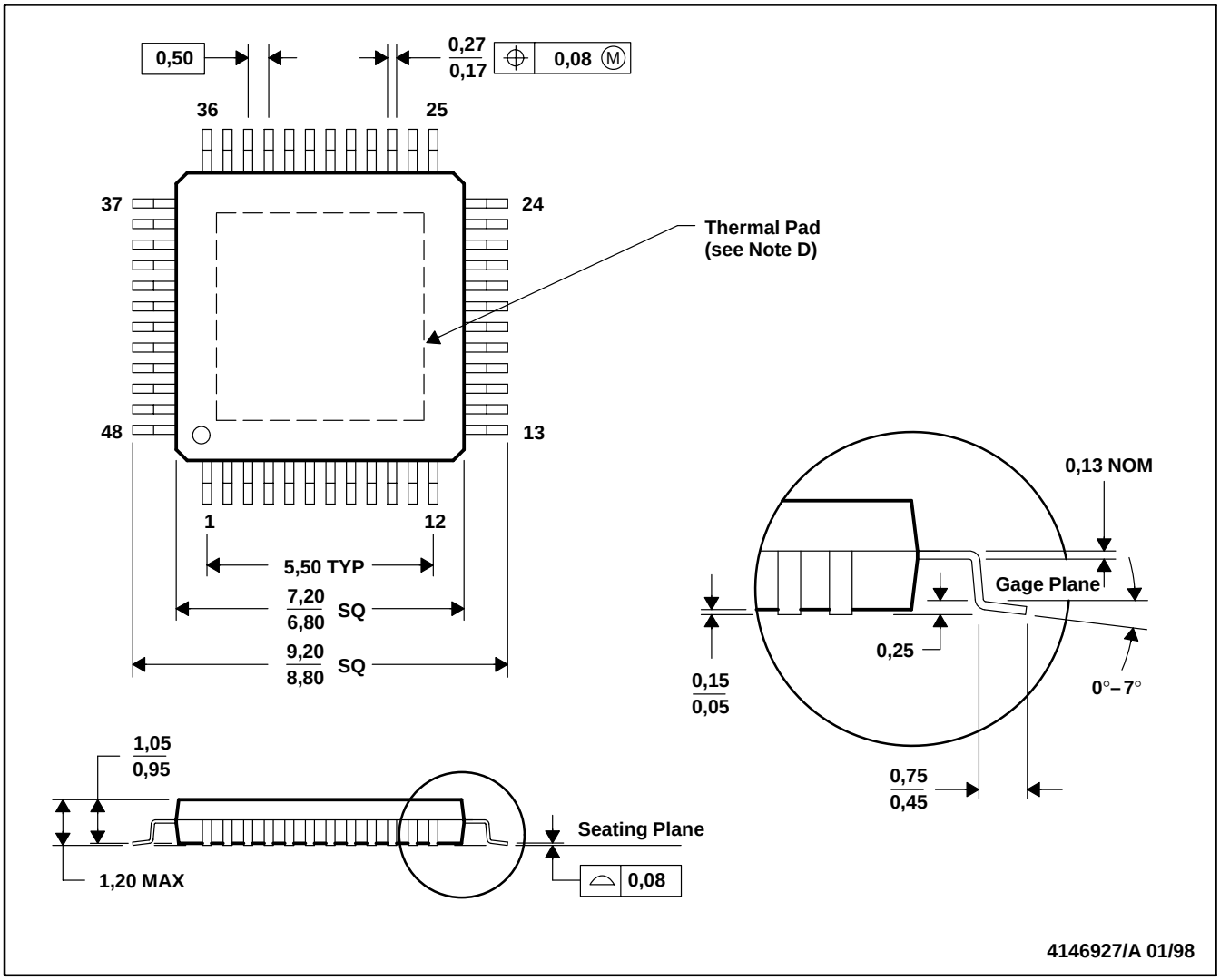


Figure 27

MECHANICAL DATA

PHP (S-PQFP-G48) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS1240CPHP	OBSOLETE	HTQFP	PHP	48		TBD	Call TI	Call TI
THS1240IPHP	OBSOLETE	HTQFP	PHP	48		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265