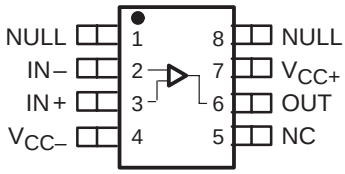
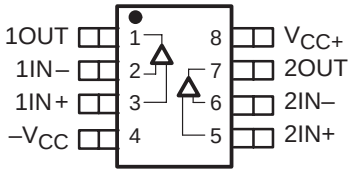
- **Ultra-low 1.6 nV/√Hz Voltage Noise**
- **High Speed**
  - **100 MHz Bandwidth (G = 2 (–1), –3 dB)**
  - **100 V/μs Slew Rate**
- **Stable in Gains of 2 (–1) or Greater**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Low 0.5 mV (Typ) Input Offset Voltage**
- **90 mA Output Current Drive (Typical)**
- **±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package**
- **Evaluation Module Available**

THS4031
D, DGN, AND JG PACKAGE
(TOP VIEW)



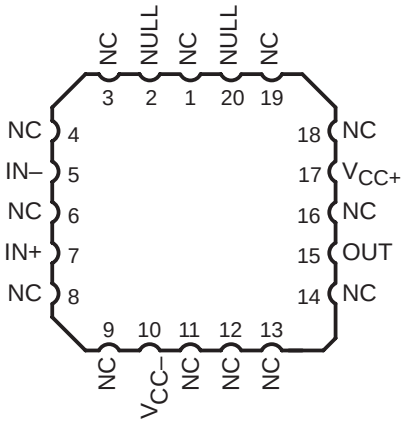
NC – No internal connection

THS4032
D AND DGN PACKAGE
(TOP VIEW)



Cross-Section View Showing
PowerPAD™ Option (DGN)

THS4031
FK PACKAGE
(TOP VIEW)



description

The THS4031 and THS4032 are ultralow-voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communication and imaging. The single-amplifier THS4031 and the dual-amplifier THS4032 offer very good ac performance with 100-MHz bandwidth, 100-V/μs slew rate, and 60-ns settling time (0.1%). The THS4031 and THS4032 are stable at gains of 2 (–1) or greater. These amplifiers have a high drive capability of 90 mA and draw only 8.5-mA supply current per channel. With total harmonic distortion (THD) of –72 dBc at f = 1 MHz, the THS4031 and THS4032 are ideally suited for applications requiring low distortion.

Related Devices

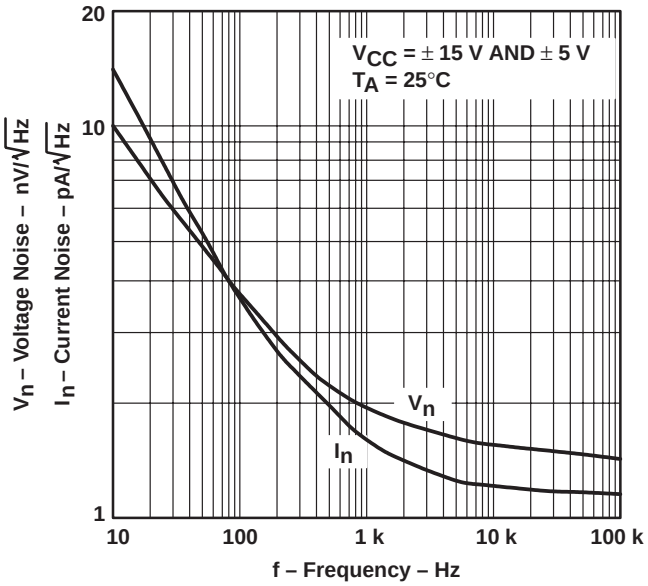
DEVICE	DESCRIPTION
THS4011/12	240-MHz Low Distortion High-Speed Amplifiers
THS4021/2	350-MHz Low Noise High-Speed Amplifiers
THS4081/2	175-MHz Low Power High-Speed Amplifiers

CAUTION: The THS4031 and THS4032 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

VOLTAGE NOISE AND CURRENT NOISE
vs
FREQUENCY



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES					EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		CERAMIC DIP (JG)	CHIP CARRIER (FK)	
			DEVICE	SYMBOL			
0°C to 70°C	1	THS4031CD	THS4031CDGN	TIACM	—	—	THS4031EVM
	2	THS4032CD	THS4032CDGN	TIABD	—	—	THS4032EVM
–40°C to 85°C	1	THS4031ID	THS4031IDGN	TIACN	—	—	—
	2	THS4032ID	THS4032IDGN	TIABG	—	—	—
–55°C to 125°C	1	—	—	—	THS4031MJG	THS4031MFK	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4031CDGNR).

functional block diagram

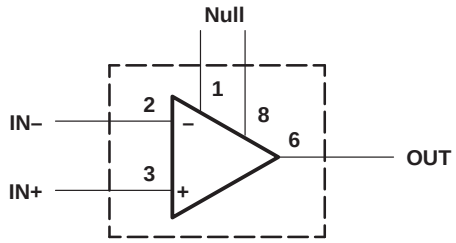


Figure 1. THS4031 – Single Channel

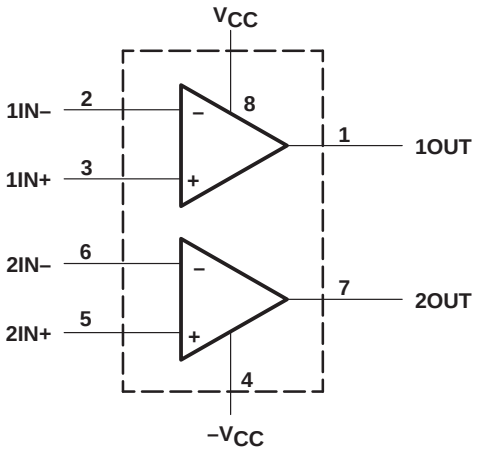


Figure 2. THS4032 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to $V_{CC–}$ . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O . . . . . 150 mA
Differential input voltage, V_{IO} . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
M-suffix . . . . . –55°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Case temperature for 60 seconds, FK package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W
JG	119	28	1050 mW
FK	87.7	20	1375 mW

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3-in. × 3-in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	
	M-suffix	–55		125	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†			THS403xC, THS403xI MIN	THS403xC, THS403xI TYP	THS403xC, THS403xI MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = –1 or 2		100		MHz
		V_{CC} = ±5 V				90		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = –1 or 2		50		MHz
		V_{CC} = ±5 V				45		
	Full power bandwidth§	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V	R_L = 1 kΩ		1.6		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			5		
SR	Slew rate‡	V_{CC} = ±15 V,	20-V step	Gain = –1		100		V/µs
		V_{CC} = ±5 V,	5-V step			80		
t_S	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V,	2.5-V step			45		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		90		ns
		V_{CC} = ±5 V,	2.5-V step			80		

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.
‡ Slew rate is measured from an output level range of 25% to 75%.
§ Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.

noise/distortion performance

PARAMETER			TEST CONDITIONS†			THS403xC, THS403xI MIN	THS403xC, THS403xI TYP	THS403xC, THS403xI MAX	UNIT
THD	Total harmonic distortion	THS4031	V_{CC} = ±5 V or ±15 V, f = 1 MHz,	$V_{O(pp)}$ = 2 V, Gain = 2	R_L = 150 Ω		–81		dBc
					R_L = 1 kΩ		–96		
		THS4032			R_L = 150 Ω		–72		
					R_L = 1 kΩ		–90		
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V,	f = 10 kHz			1.6		nV/√Hz
I_n	Input current noise		V_{CC} = ±5 V or ±15 V,	f = 10 kHz			1.2		pA/√Hz
	Differential gain error		Gain = 2, 40 IRE modulation,	NTSC and PAL, ±100 IRE ramp	V_{CC} = ±15 V		0.015%		
					V_{CC} = ±5 V		0.02%		
	Differential phase error				V_{CC} = ±15 V		0.025°		
					V_{CC} = ±5 V		0.03°		
	Channel-to-channel crosstalk (THS4032 only)		V_{CC} = ±5 V or ±15 V,	f = 1 MHz			–61		dBc

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†			THS403xC, THS403xI			UNIT
					MIN	TYP	MAX	
Open loop gain		V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±10 V	T_A = 25°C	45	75		V/mV
				T_A = full range	40			
		V_{CC} = ±5 V, R_L = 1 kΩ	V_O = ±2.5 V	T_A = 25°C	35	55		
				T_A = full range	30			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		0.5	2	mV
				T_A = full range			3	
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		3	6	µA
				T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		30	250	nA
				T_A = full range			400	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V		T_A = full range		10		µV/°C
	Input offset current drift	V_{CC} = ±5 V or ±15 V		T_A = full range		0.2		nA/°C

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

input characteristics

PARAMETER		TEST CONDITIONS†			THS403xC, THS403xI			UNIT
					MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.5	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
				T_A = full range	80			
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
				T_A = full range	85			
r_i	Input resistance					2		MΩ
C_i	Input capacitance					1.5		pF

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

output characteristics

PARAMETER		TEST CONDITIONS†		THS403xC, THS403xI			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.9		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.5		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS†		THS403xC, THS403xI			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†			THS4031M			UNIT
					MIN	TYP	MAX	
BW	Unity gain bandwidth	V_{CC} = ±15 V,	Closed loop	R_L = 1 kΩ	100§	120		MHz
	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = –1 or 2		100		MHz
		V_{CC} = ±5 V		Gain = –1 or 2		90		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = –1 or 2		50		MHz
		V_{CC} = ±5 V				45		
	Full power bandwidth‡	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V	R_L = 1 kΩ		1.6		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			5		
SR	Slew rate	V_{CC} = ±15 V		R_L = 1 kΩ	80§	100		V/µs
t_S	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V,	2.5-V step			45		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		90		ns
		V_{CC} = ±5 V,	2.5-V step			80		

† Full range = –55°C to 125°C for the THS4031M.
‡ Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.
§ This parameter is not tested.

noise/distortion performance

PARAMETER		TEST CONDITIONS†			THS4031M			UNIT
					MIN	TYP	MAX	
THD	Total harmonic distortion	V_{CC} = ±5 V or ±15 V, f = 1 MHz, Gain = 2,	$V_{O(pp)}$ = 2 V, T_A = 25°C	R_L = 150 Ω		–81		dBc
				R_L = 1 kΩ		–96		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, T_A = 25°C	f = 10 kHz,	R_L = 150 Ω		1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, T_A = 25°C	f = 10 kHz,	R_L = 150 Ω		1.2		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation, T_A = 25°C	NTSC and PAL, ±100 IRE ramp, R_L = 150 Ω	V_{CC} = ±15 V		0.015%		
				V_{CC} = ±5 V		0.02%		
	Differential phase error			V_{CC} = ±15 V		0.025°		
				V_{CC} = ±5 V		0.03°		

† Full range = –55°C to 125°C for the THS4031M.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†		THS4031M MIN	THS4031M TYP	THS4031M MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V	T_A = 25°C	45	75		V/mV
			T_A = full range	40			
		V_{CC} = ±5 V, V_O = ±2.5 V	T_A = 25°C	40	55		
			T_A = full range	35			
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		0.5	2	mV
			T_A = full range			3	
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V	T_A = full range		10		µV/°C
	Input offset current drift	V_{CC} = ±5 V or ±15 V	T_A = full range		0.2		nA/°C

† Full range = –55°C to 125°C for the THS4031M.

input characteristics

PARAMETER		TEST CONDITIONS†		THS4031M MIN	THS4031M TYP	THS4031M MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.5	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = full range	85			
r_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF

† Full range = –55°C to 125°C for the THS4031M.

output characteristics

PARAMETER		TEST CONDITIONS†		THS4031M MIN	THS4031M TYP	THS4031M MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.9		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.5		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω

† Full range = –55°C to 125°C for the THS4031M.

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS†		THS4031M			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = full range			10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			

† Full range = –55°C to 125°C for the THS4031M.

PARAMETER MEASUREMENT INFORMATION

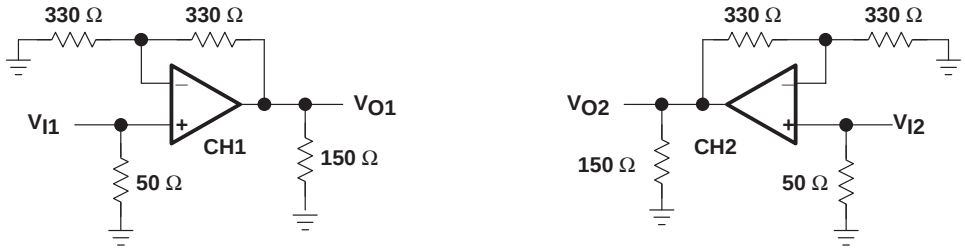


Figure 3. THS4032 Crosstalk Test Circuit

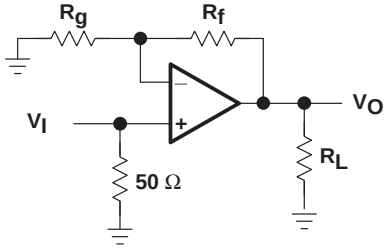


Figure 4. Step Response Test Circuit

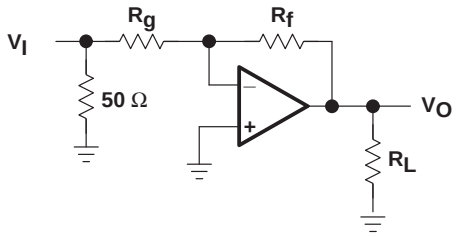


Figure 5. Step Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Input offset voltage distribution		6, 7
V_{IO}	Input offset voltage	vs Free-air temperature	8
I_{IB}	Input bias current	vs Free-air temperature	9
V_O	Output voltage swing	vs Supply voltage	10
V_{OM}	Maximum output voltage swing	vs Free-air temperature	11
I_O	Maximum output current	vs Free-air temperature	12
I_{CC}	Supply current	vs Free-air temperature	13
V_{IC}	Common-mode input voltage	vs Supply voltage	14
Z_O	Closed-loop output impedance	vs Frequency	15
	Open-loop gain		16
	Phase response		
PSRR	Power-supply rejection ratio	vs Frequency	17
CMRR	Common-mode rejection ratio	vs Frequency	18
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	1-V step response		39, 40
	4-V step response		41
	20-V step response		42

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE DISTRIBUTION

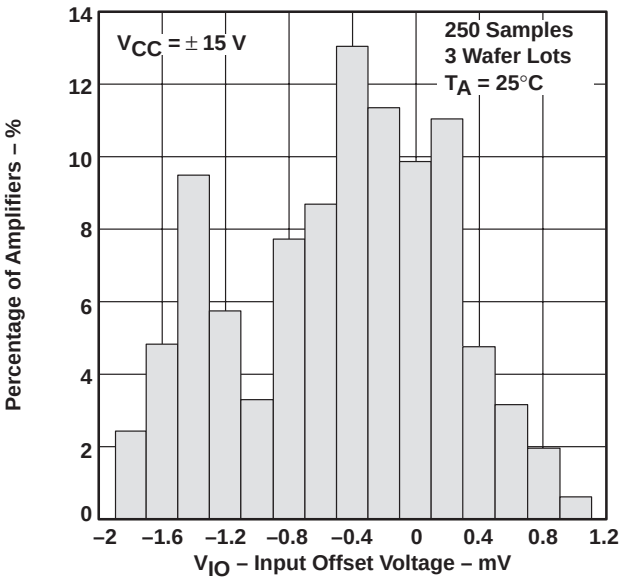


Figure 6

INPUT OFFSET VOLTAGE DISTRIBUTION

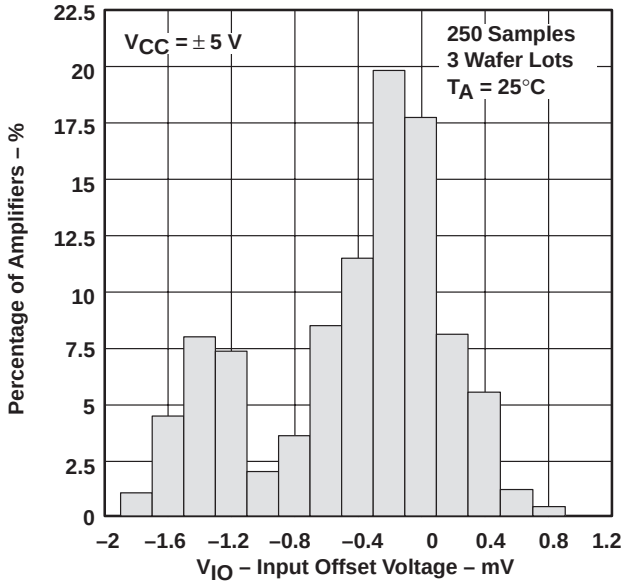


Figure 7

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

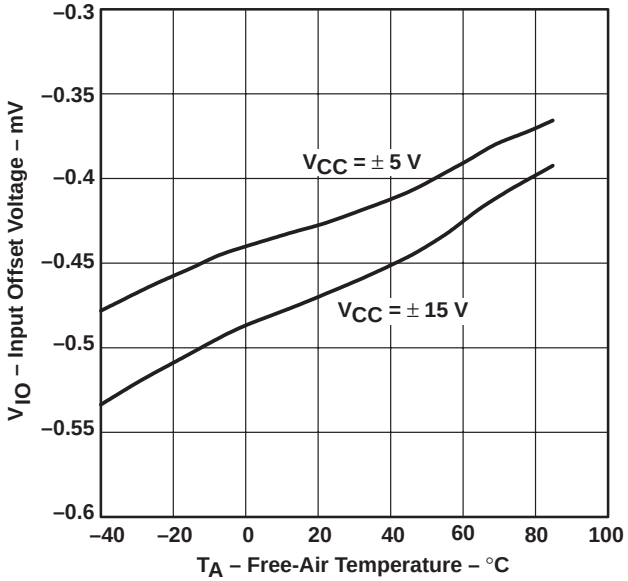


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

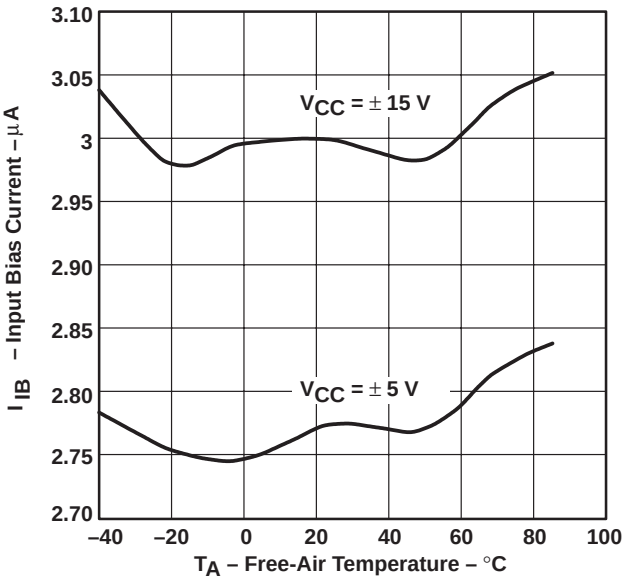


Figure 9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

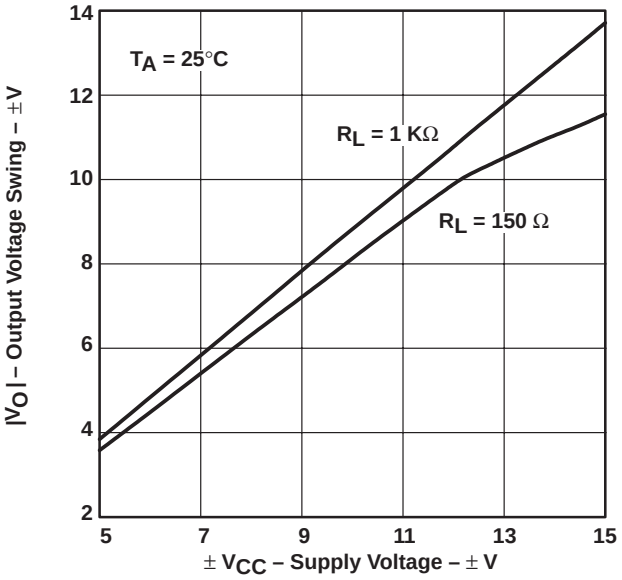


Figure 10

MAXIMUM OUTPUT VOLTAGE SWING vs FREE–AIR TEMPERATURE

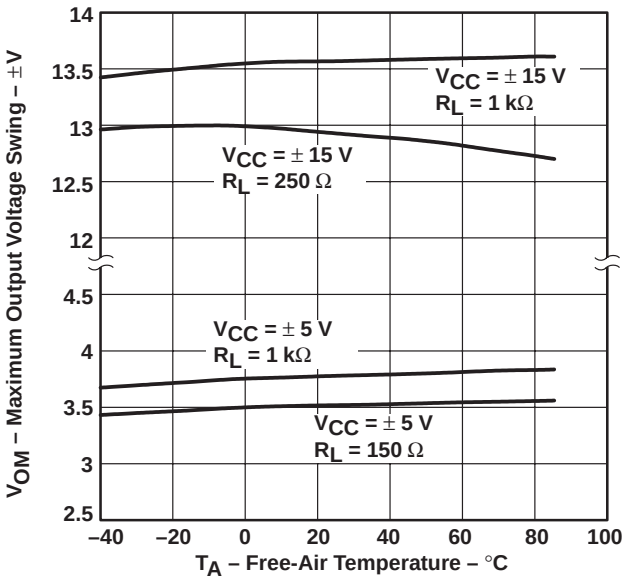


Figure 11

MAXIMUM OUTPUT CURRENT vs FREE-AIR TEMPERATURE

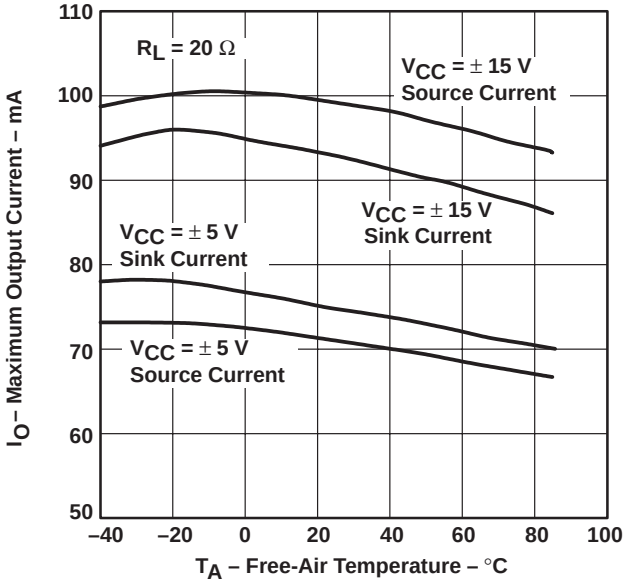


Figure 12

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

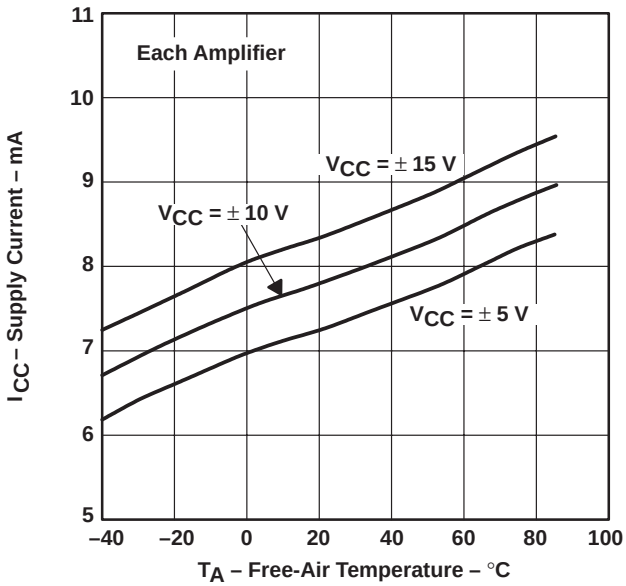


Figure 13

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

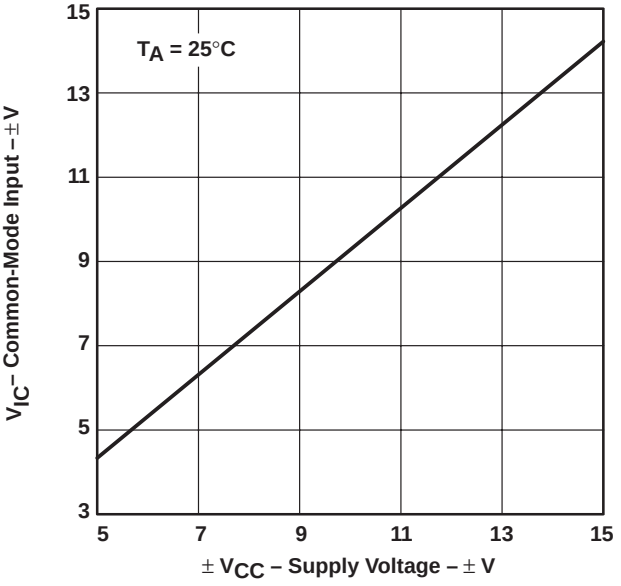


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

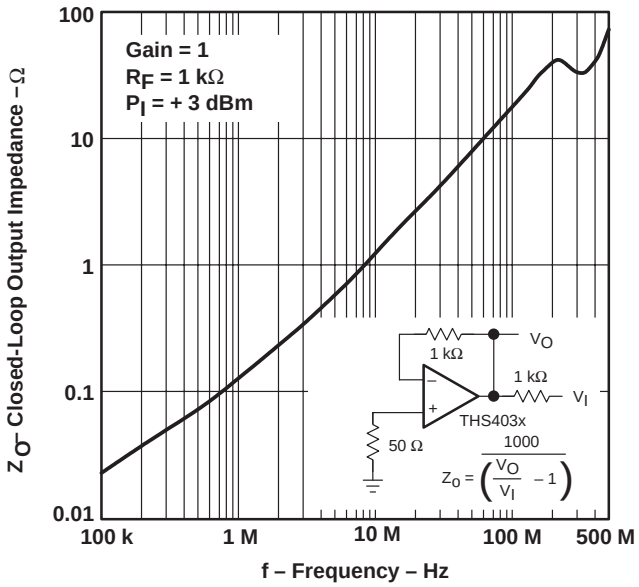


Figure 15

OPEN-LOOP GAIN AND PHASE RESPONSE

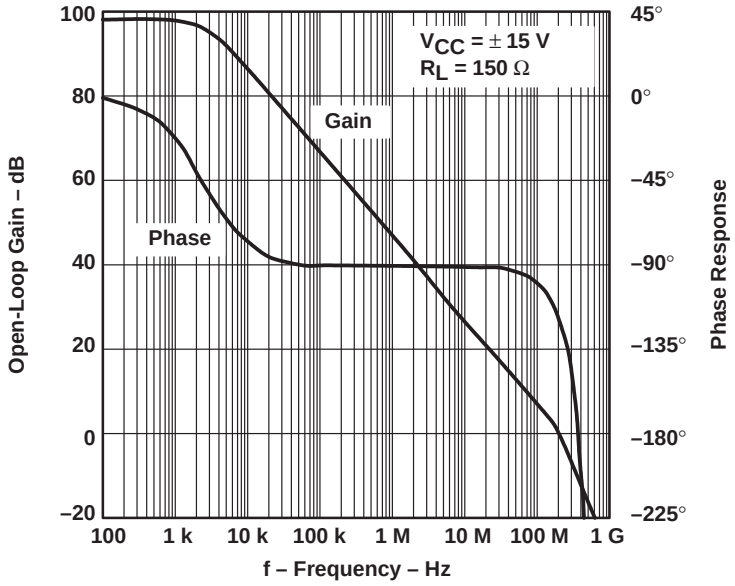


Figure 16

TYPICAL CHARACTERISTICS

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

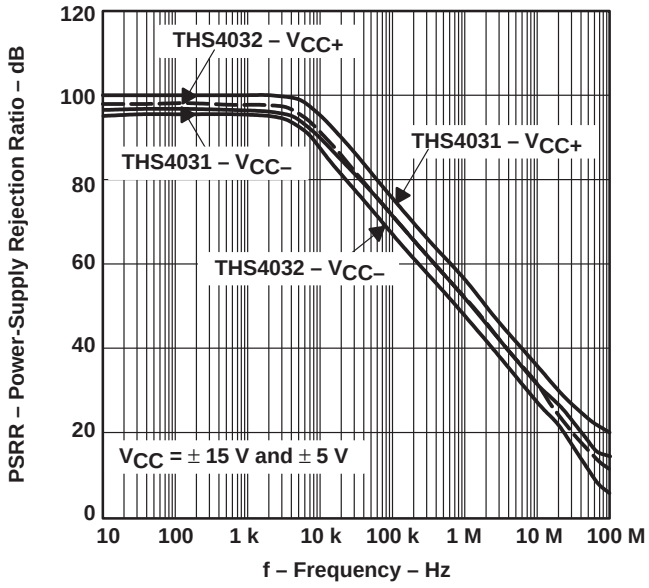


Figure 17

COMMON-MODE REJECTION RATIO vs FREQUENCY

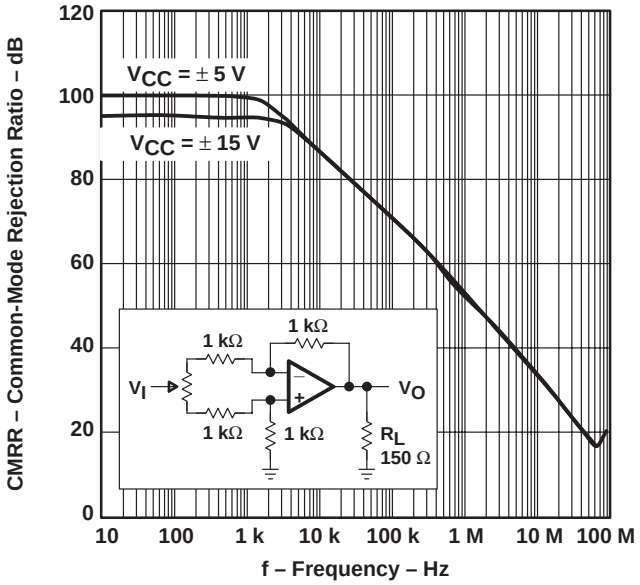


Figure 18

THS4032 CROSSTALK vs FREQUENCY

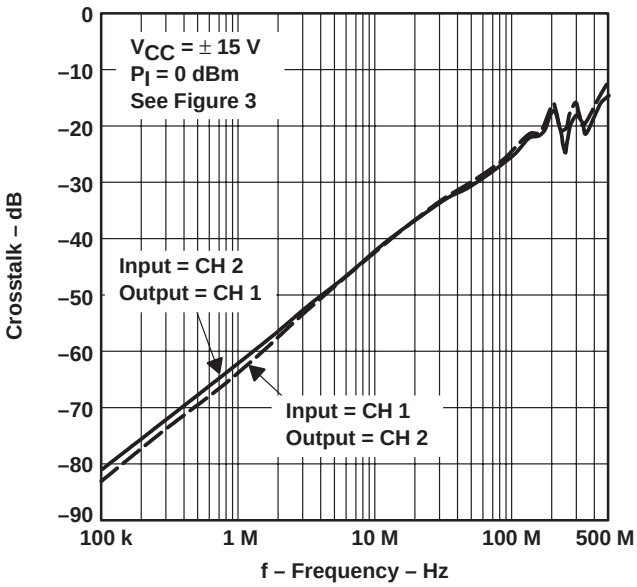


Figure 19

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION
vs
FREQUENCY

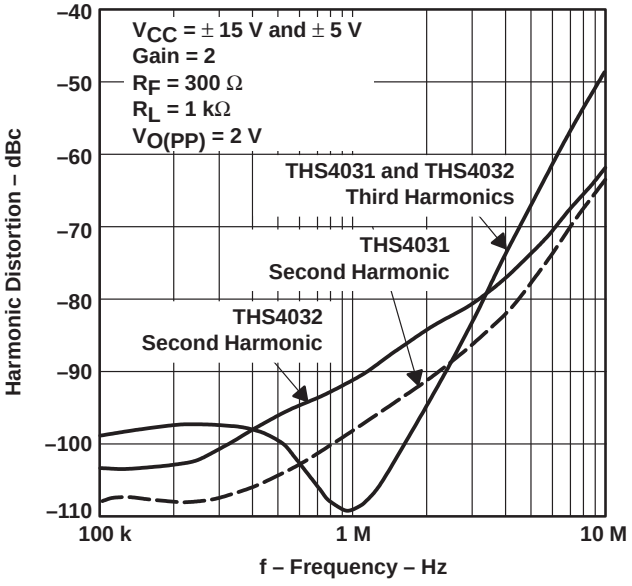


Figure 20

HARMONIC DISTORTION
vs
FREQUENCY

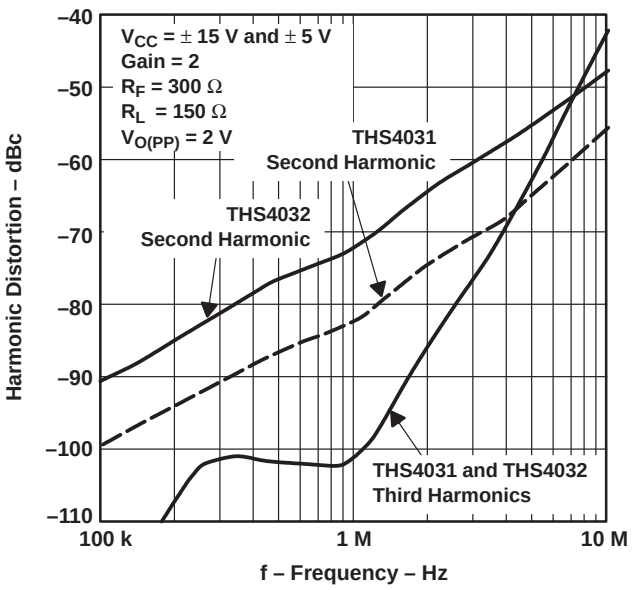


Figure 21

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

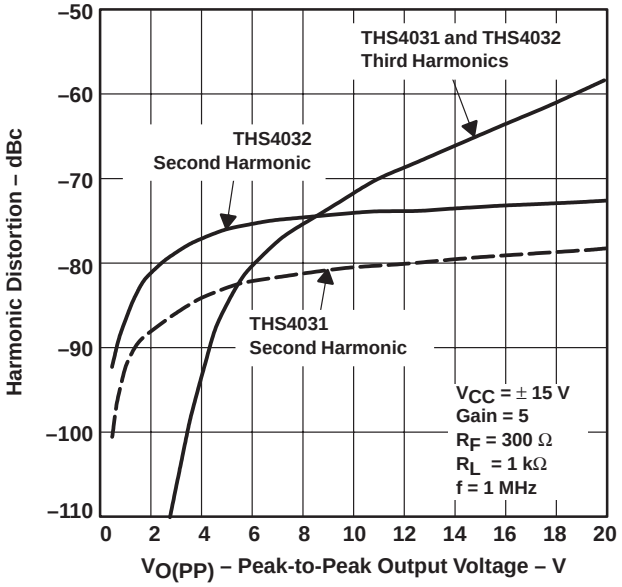


Figure 22

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

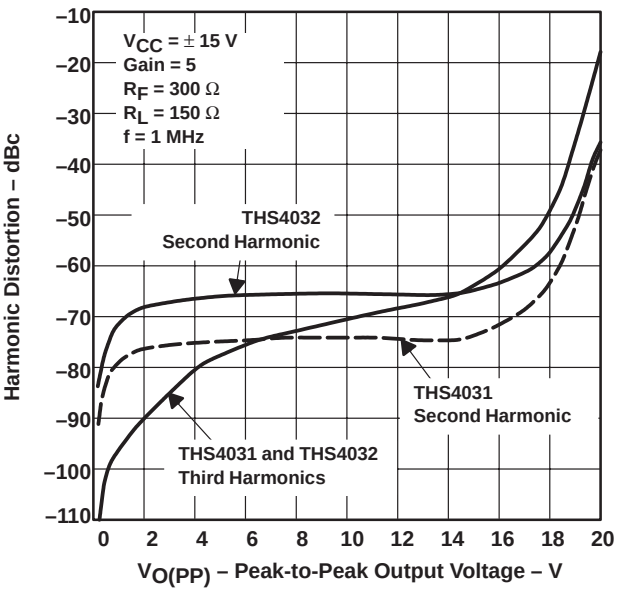


Figure 23

TYPICAL CHARACTERISTICS

SLEW RATE vs FREE-AIR TEMPERATURE

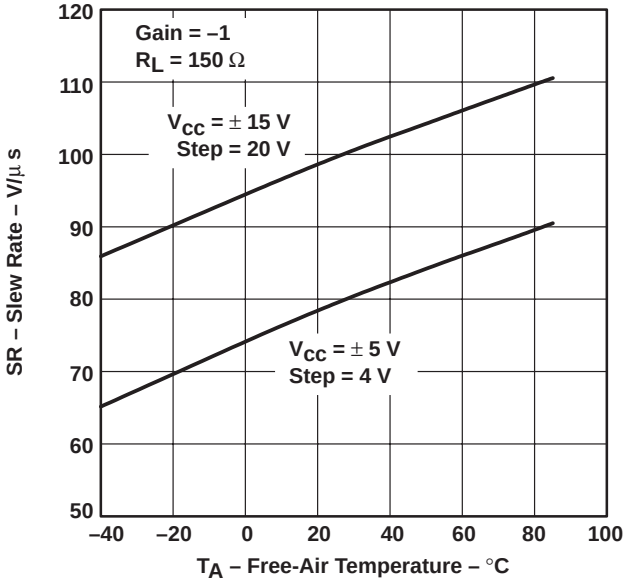


Figure 24

0.1% SETTLING TIME vs OUTPUT VOLTAGE STEP SIZE

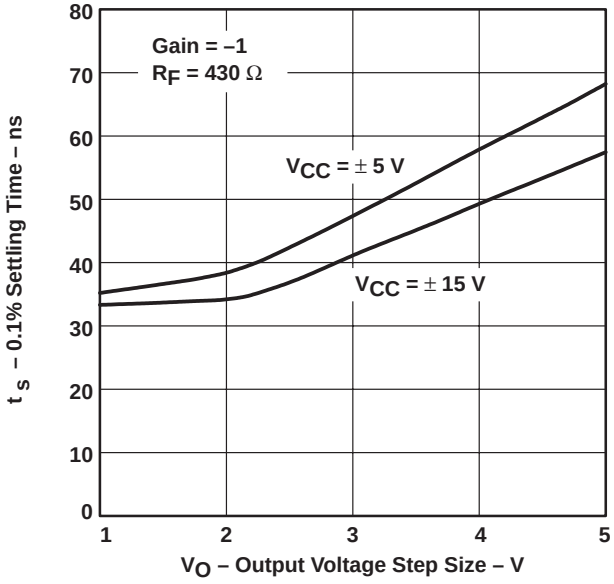


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

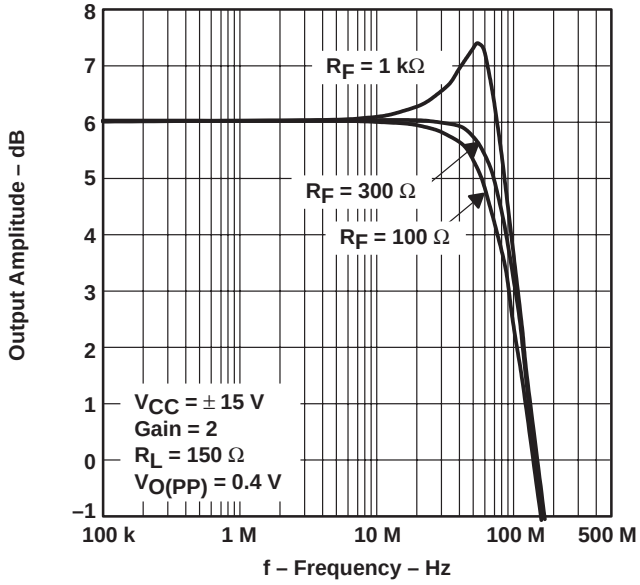


Figure 26

OUTPUT AMPLITUDE vs FREQUENCY

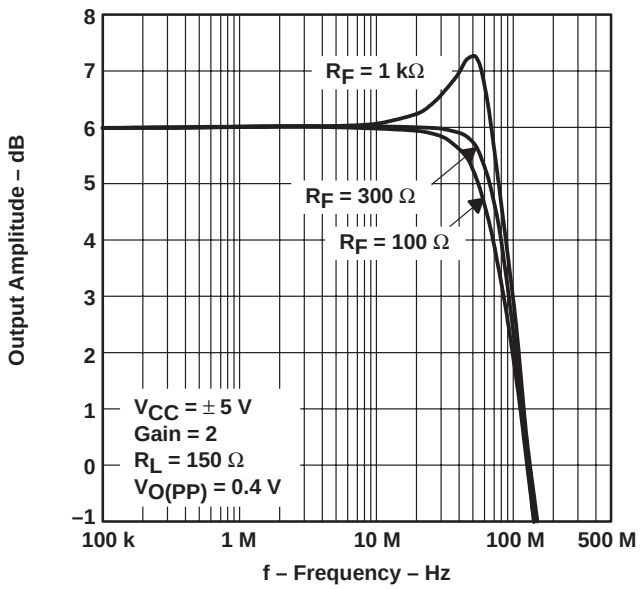


Figure 27

TYPICAL CHARACTERISTICS

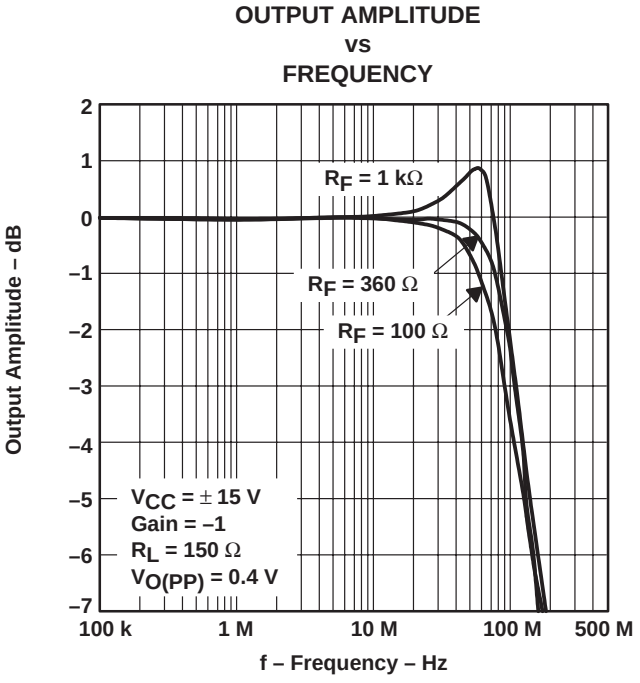


Figure 28

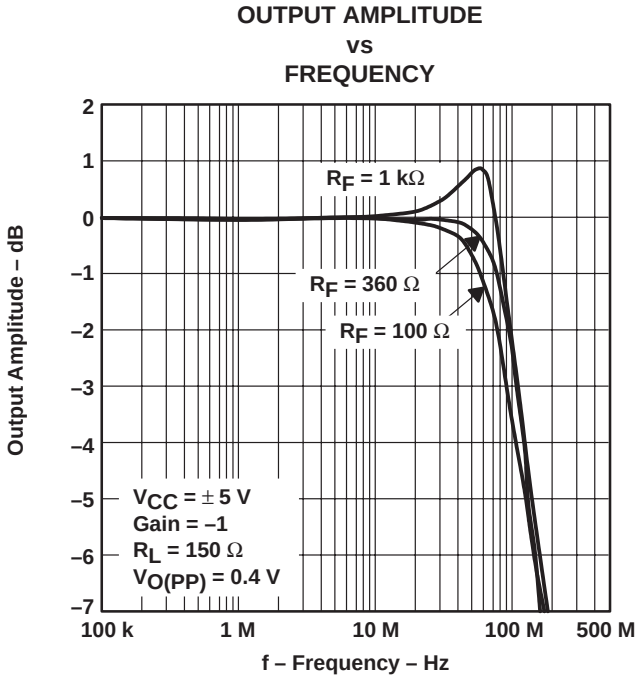


Figure 29

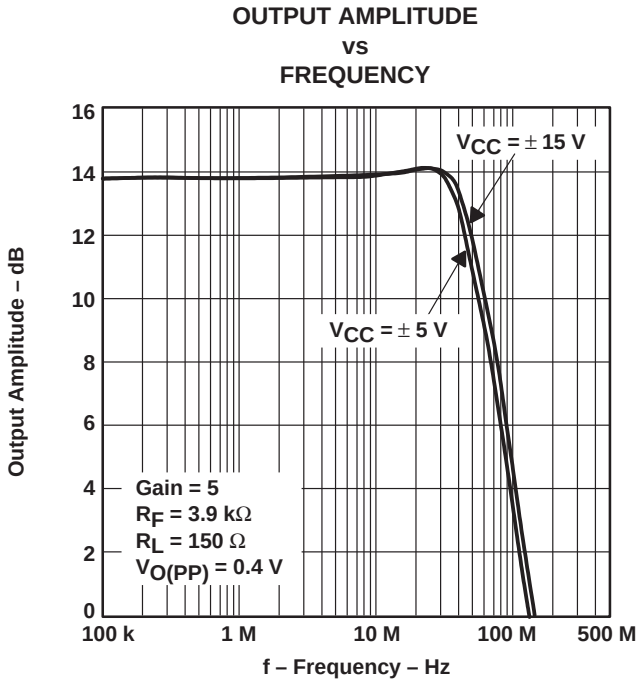


Figure 30

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

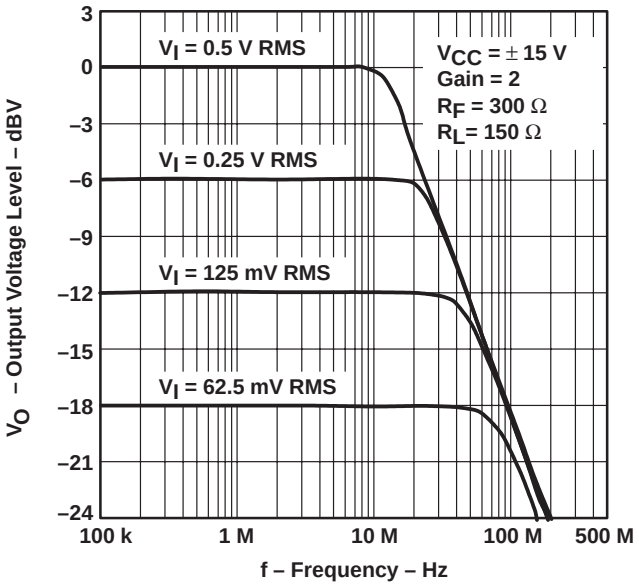


Figure 31

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

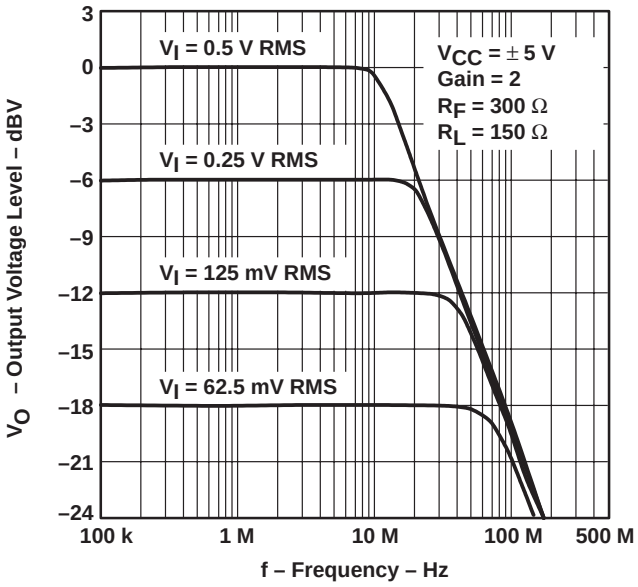


Figure 32

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

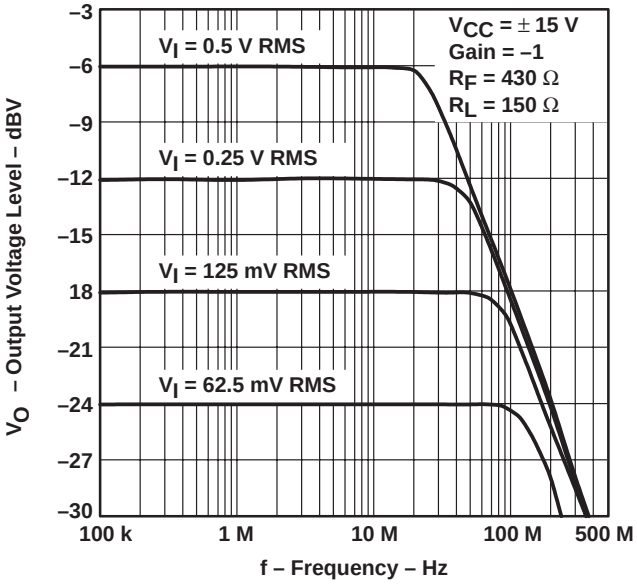


Figure 33

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

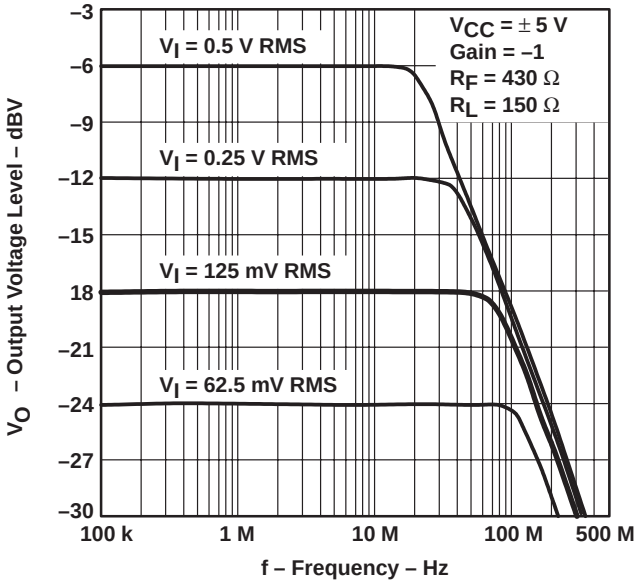


Figure 34

TYPICAL CHARACTERISTICS

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

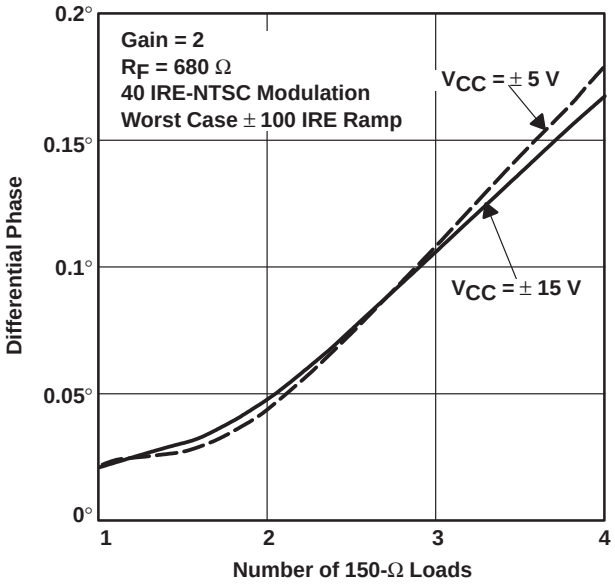


Figure 35

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

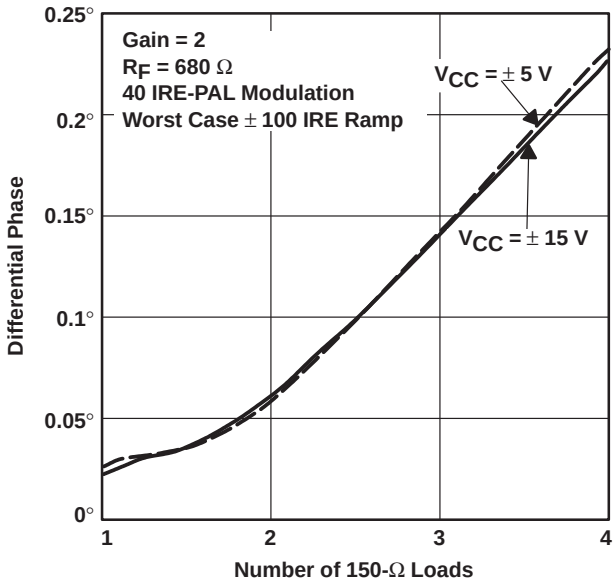


Figure 36

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

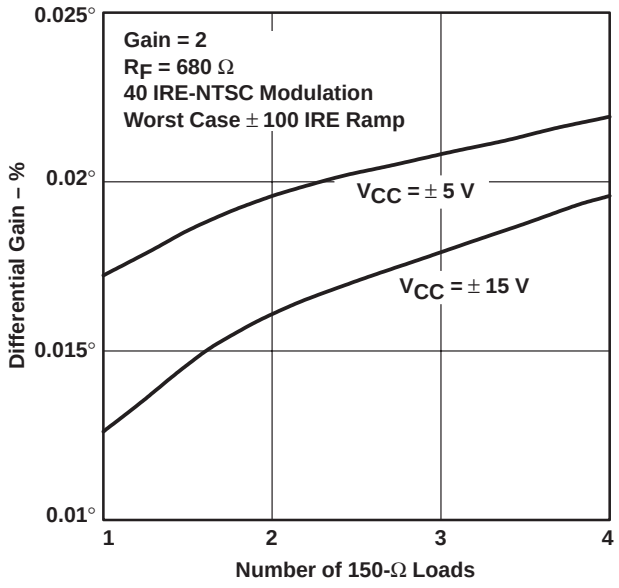


Figure 37

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

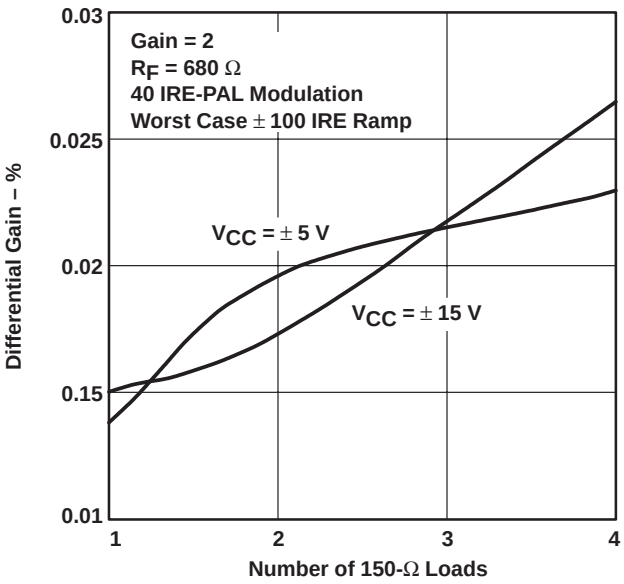


Figure 38

TYPICAL CHARACTERISTICS

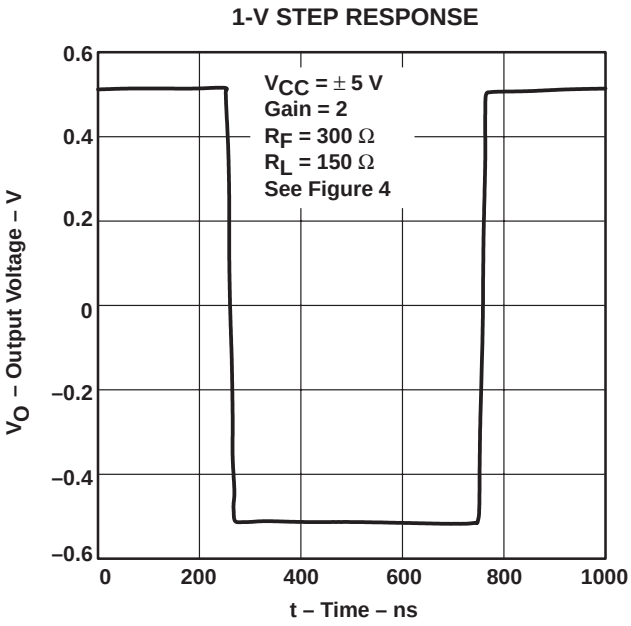


Figure 39

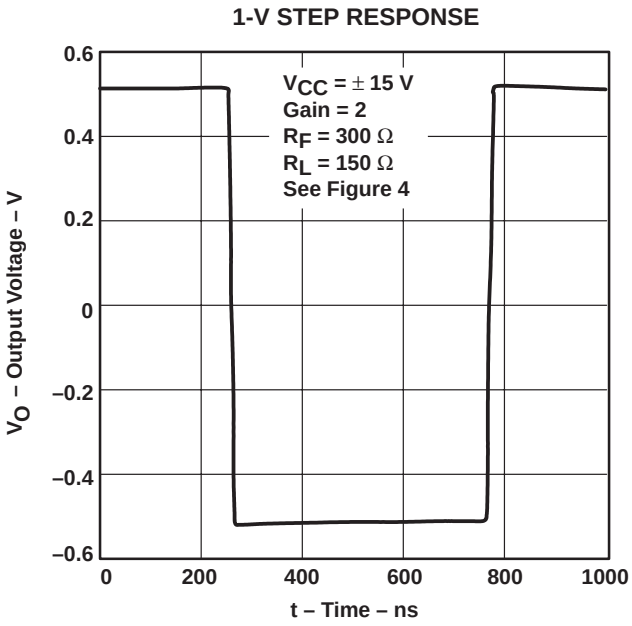


Figure 40

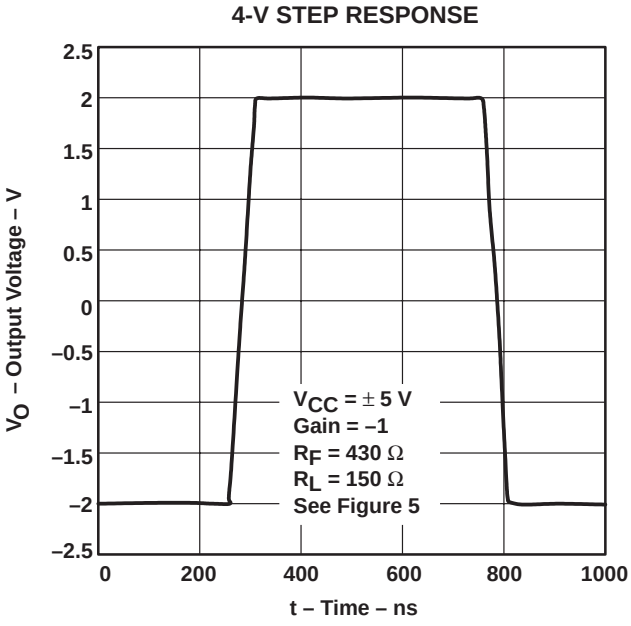


Figure 41

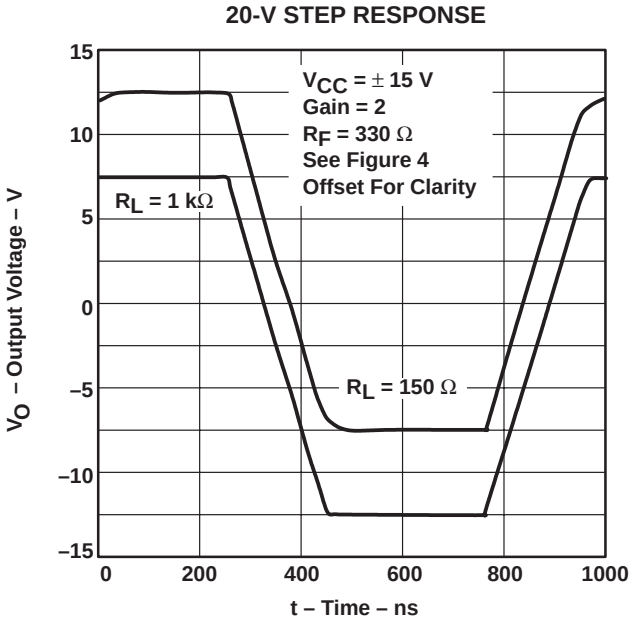


Figure 42

APPLICATION INFORMATION

theory of operation

The THS403x is a high-speed operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 43.

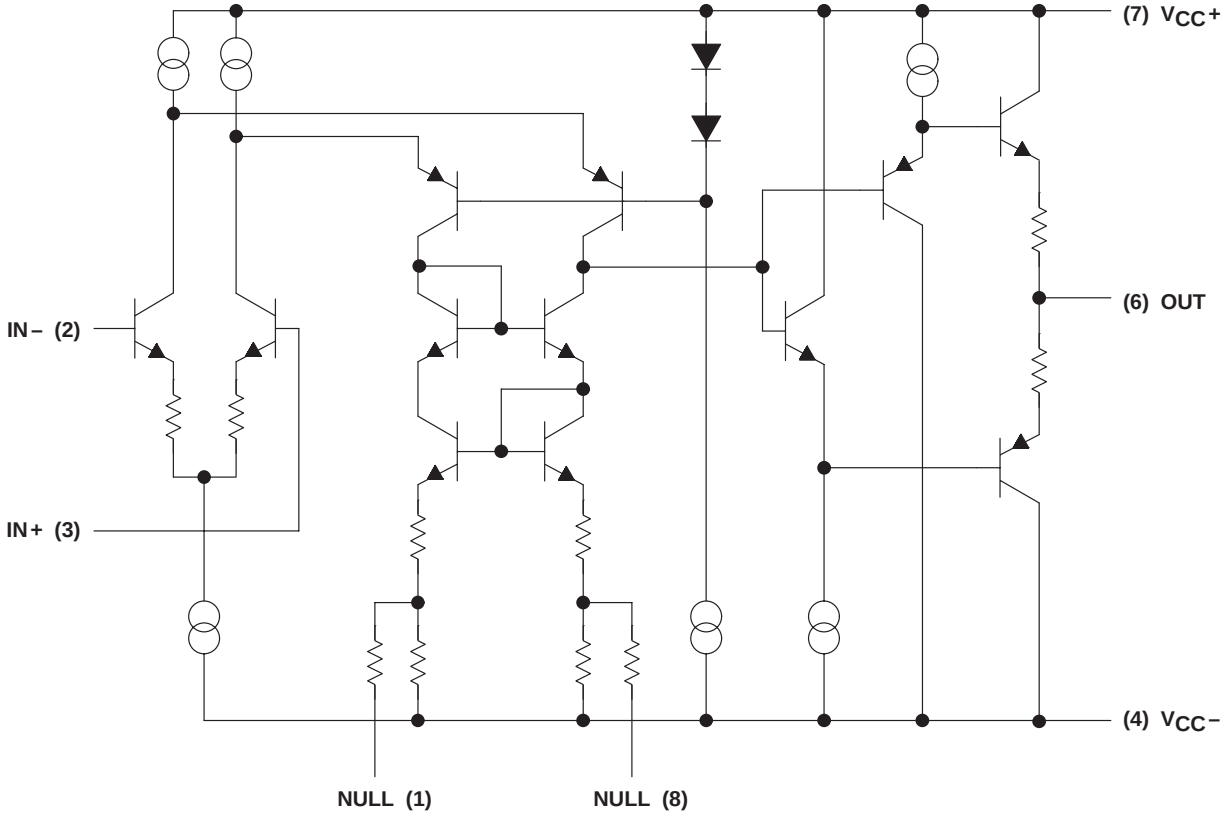


Figure 43. THS4031 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals. The noise model for the THS403x, shown in Figure 44, includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

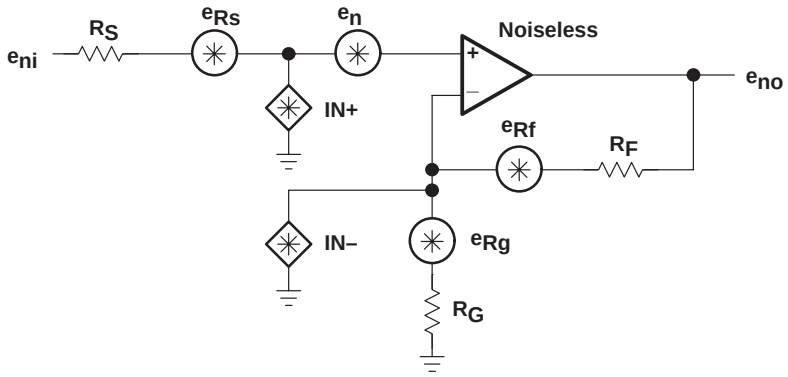


Figure 44. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This advantage can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 45 shows the noise figure graph for the THS403x.

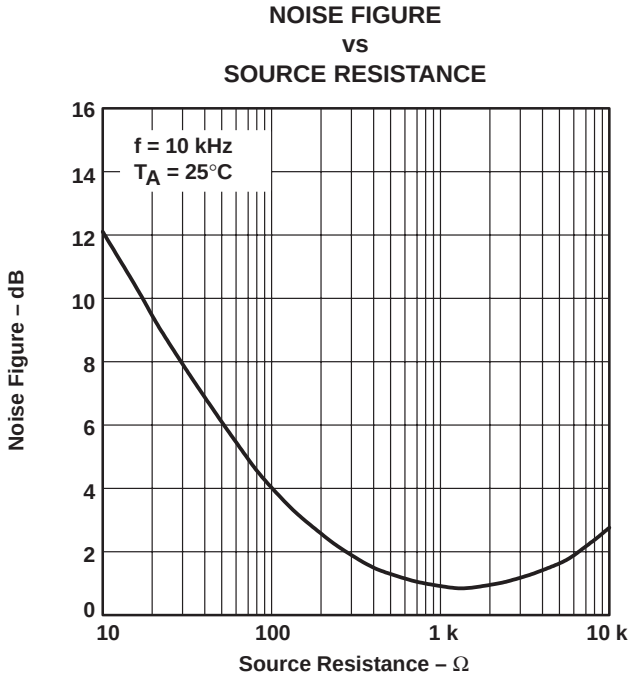


Figure 45. Noise Figure vs Source Resistance

APPLICATION INFORMATION

optimizing frequency response

Internal frequency compensation of the THS403x was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the THS403x must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response (see Figure 46 and Figure 47). Two things can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier, including the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possible oscillations will then occur if this happens.

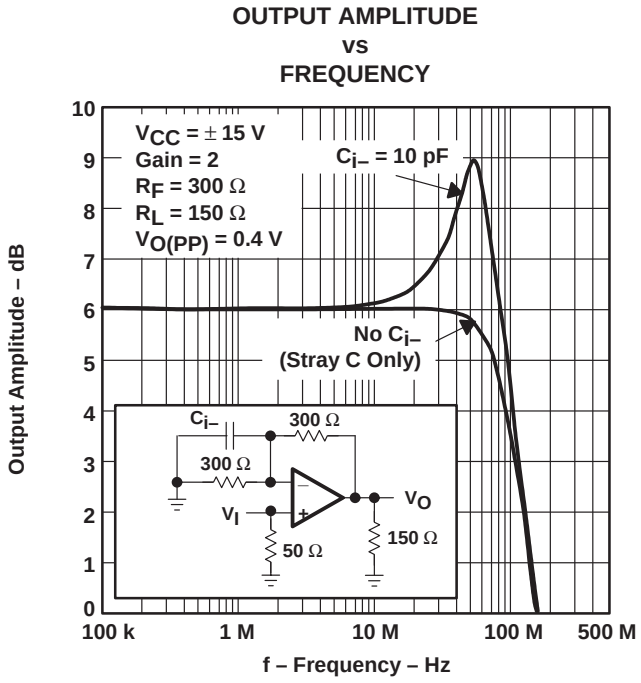


Figure 46

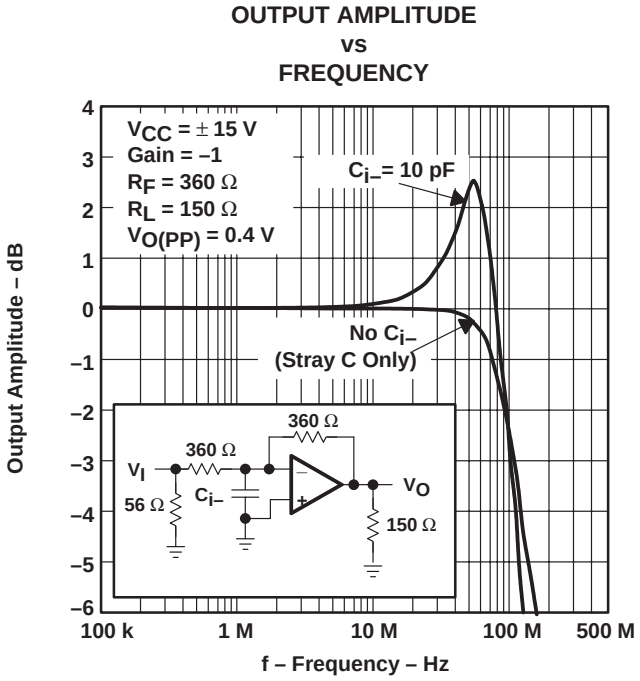


Figure 47

The second precaution to help maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in Figure 30, a feedback resistor of 3.9 kΩ with a gain resistor of 1 kΩ only shows a small peaking in the frequency response. The parallel resistance is only 800 Ω. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this peaking out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 26 – 29, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS403x.

APPLICATION INFORMATION

optimizing frequency response (continued)

Table 1. Recommended Feedback Resistors

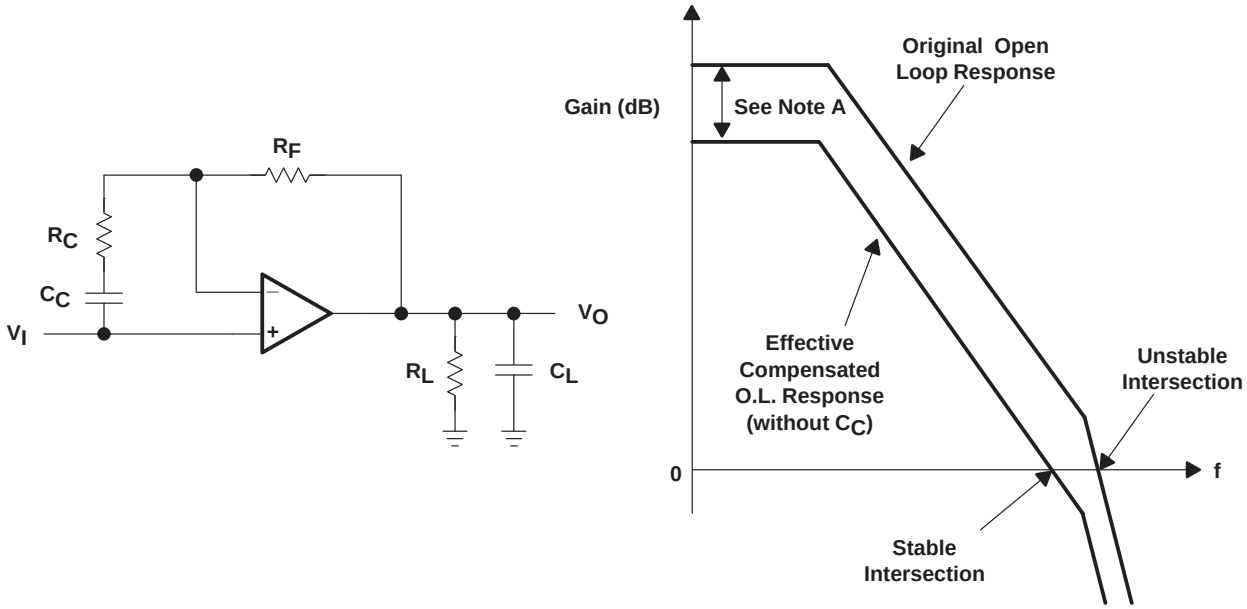
GAIN	R_f for V_{CC} = ±15 V and ± 5 V
2	300 Ω
–1	360 Ω
5	3.3 kΩ (low stray-c PCB only)

unity-gain concerns

THS403x was designed for extremely low noise with a minimum gain of 2 (–1). If the amplifier were to be configured for unity gain, the output would tend to oscillate because the open-loop intersection on a Bode diagram is at a –40 dB/decade slope instead of the –20 dB/decade slope required for stable operation. But, it is sometimes desirable to have a low-noise unity gain buffer. There is a way to accomplish this feat with the THS403x with some added complexity (see Figure 48). The lag compensation circuit shown in Figure 48 increases the noise gain of the amplifier without increasing the signal gain. Another way to look at this is that the open-loop gain is effectively reduced by the $1 + R_F/R_C$ gain. This reduction causes the –40 dB/decade pole to be shifted down into an open-loop gain of less than 1. The drawbacks of this circuit are the decreased frequency response, the increased noise, and the increased output offset voltage (V_{OO}). One way to eliminate the V_{OO} increase is to add a capacitor (C_C) in series with R_C, with the added requirement that the time constant of C_C and R_C be set low enough for the Bode plot intersection to be at a –20 dB/decade slope. Typically, a $1 + R_F/R_C$ gain of 2 to 3 yields a smooth frequency response for the THS403x. If C_C is used, it is desirable to have the $1/(2\pi R_C C_C)$ frequency 5 to 10 times lower than the amplifier's natural bandwidth. One additional advantage this circuit provides is that it makes driving capacitive loads much easier. A capacitive load causes the –40 dB/decade intersection (because of the phase lag), to be above unity gain, the same as described previously. In general, this R_C and C_C modification can be used in both an inverting and noninverting configuration with the same results.

APPLICATION INFORMATION

unity-gain concerns (continued)



NOTE A: The difference is due to $1+R_F/R_C$ noise gain.

Figure 48. Unity Gain Compensation

driving a capacitive load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS403x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the phase margin of the device leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

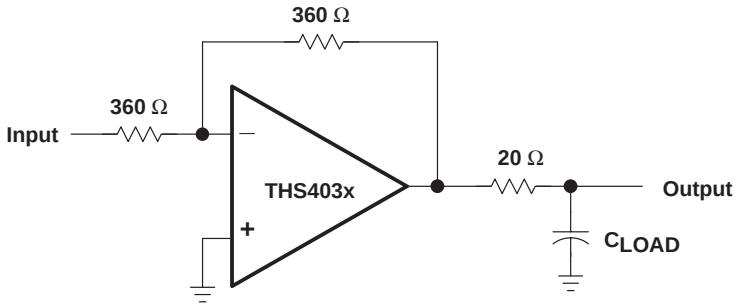


Figure 49. Driving a Capacitive Load

APPLICATION INFORMATION

offset nulling

The THS403x has very low input offset voltage for a high speed amplifier. However, if additional correction is required, the designer can make use of an offset nulling function provided on the THS4031. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 50.

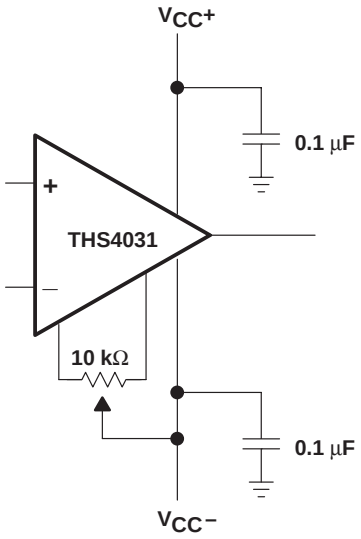
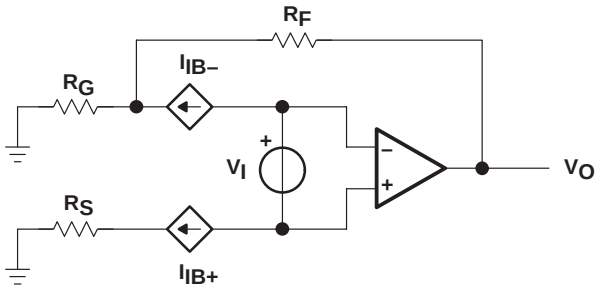


Figure 50. Offset Nulling Schematic

offset voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left[1 + \left(\frac{R_F}{R_G}\right)\right] \pm I_{IB+}\, R_S\left[1 + \left(\frac{R_F}{R_G}\right)\right] \pm I_{IB-}\, R_F$$

Figure 51. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 52).

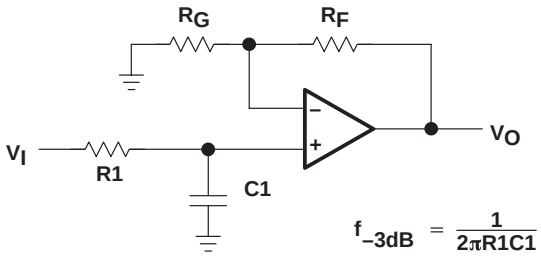


Figure 52. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Otherwise, phase shift of the amplifier can occur.

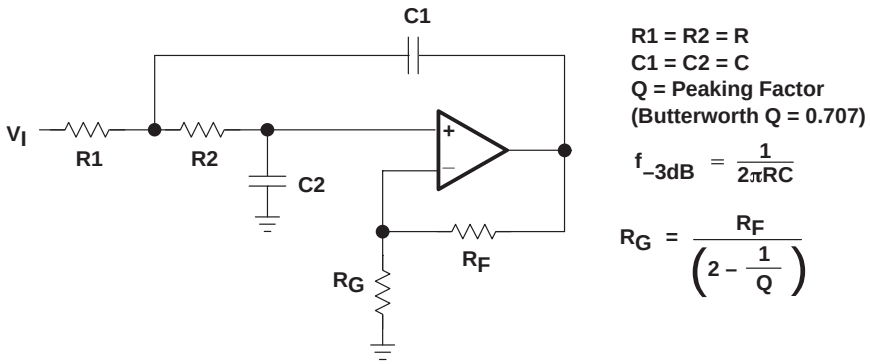


Figure 53. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit-layout considerations

In order to achieve the levels of high-frequency performance of the THS403x, it is essential that proper printed-circuit board high-frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD™ design considerations

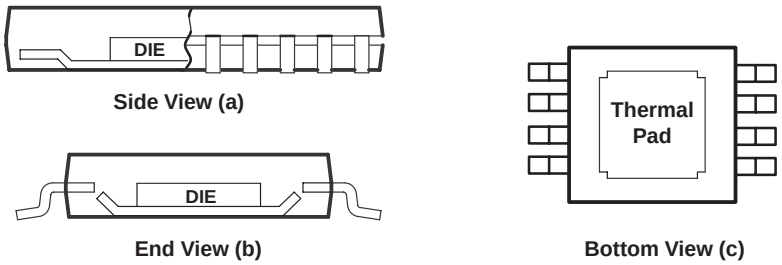
The THS403x is available in a thermally enhanced DGN package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 54(a) and Figure 54(b)]. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package [see Figure 54(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)



NOTE B: The thermal pad is electrically isolated from all terminals in the package.

Figure 54. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

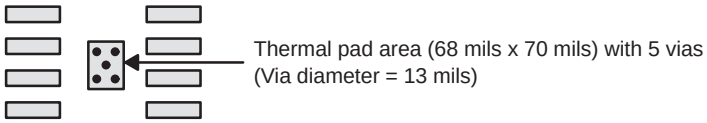


Figure 55. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in Figure 55. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS403xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403xDGN package should connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area, which prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the IC terminals.
8. With these preparatory steps in place, the THS403xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

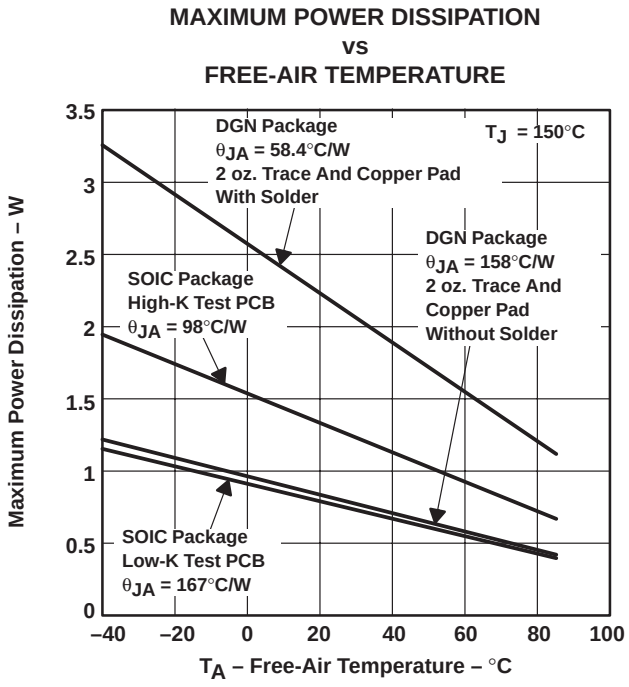
general PowerPAD™ design considerations (continued)

The actual thermal performance achieved with the THS403xDGN in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD™ version of the THS403x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 56 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS403x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and PCB size = 3”× 3”

Figure 56. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD™ installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD™ Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD™. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

The next thing to be considered is package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 57 to Figure 60 shows this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using V_{CC} = ±5 V, heat is generally not a problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD™. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4032), the sum of the RMS output currents and voltages should be used to choose the proper package.

THS4031
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

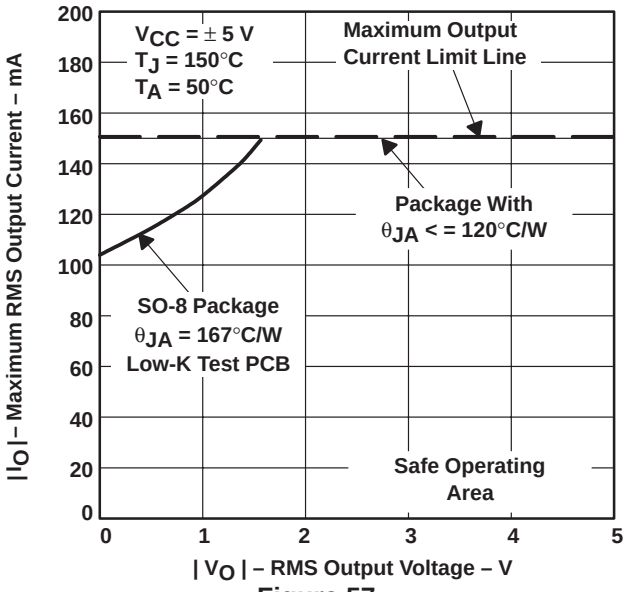


Figure 57

THS4031
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

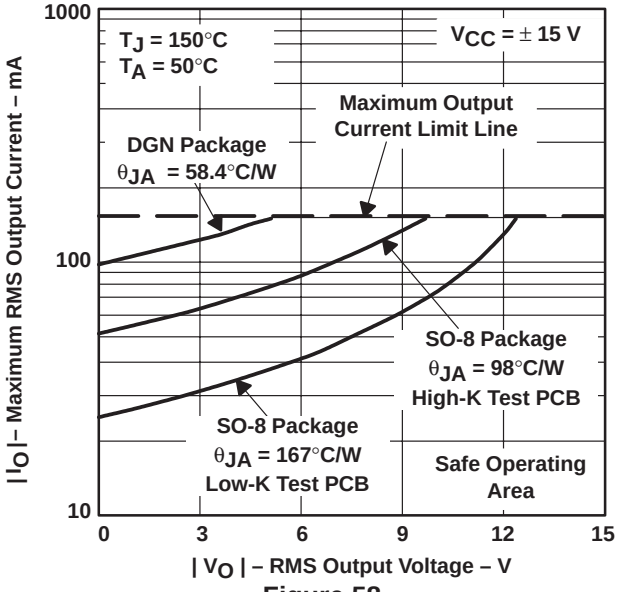


Figure 58

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

THS4032
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

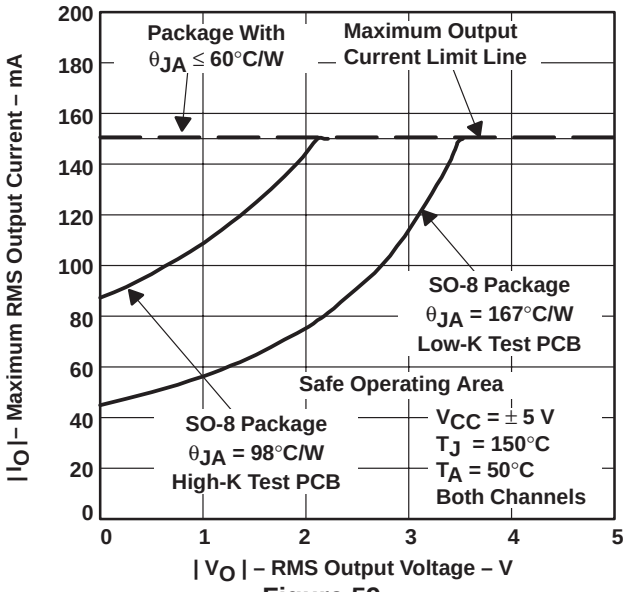


Figure 59

THS4032
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

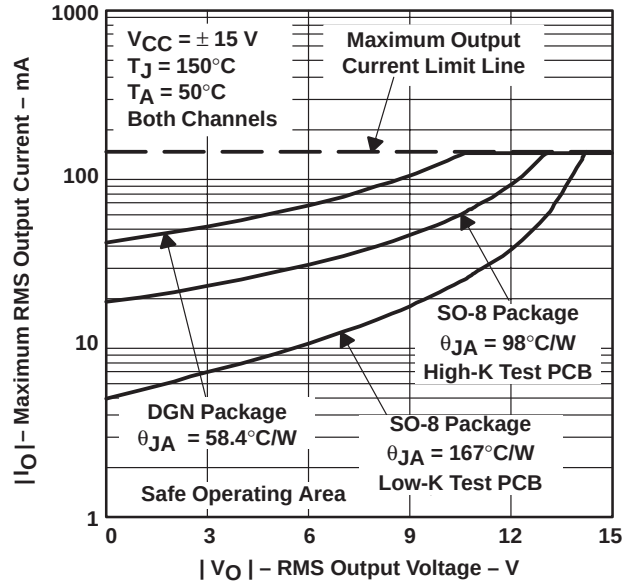


Figure 60

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4031 (literature number SLOP203) and THS4032 (literature Number SLOP135). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 61. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4031 EVM User's Guide* (literature number SLOU038) or the *THS4032 EVM User's Guide* (literature number SLOU039). To order the evaluation board, contact your local TI sales office or distributor.

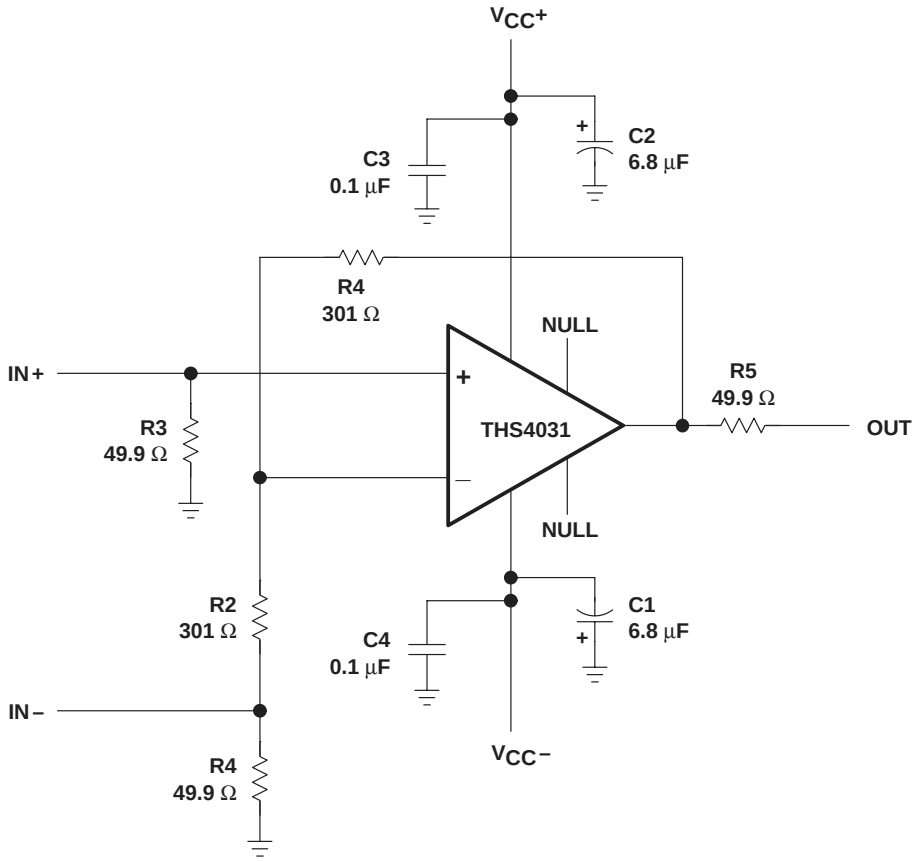
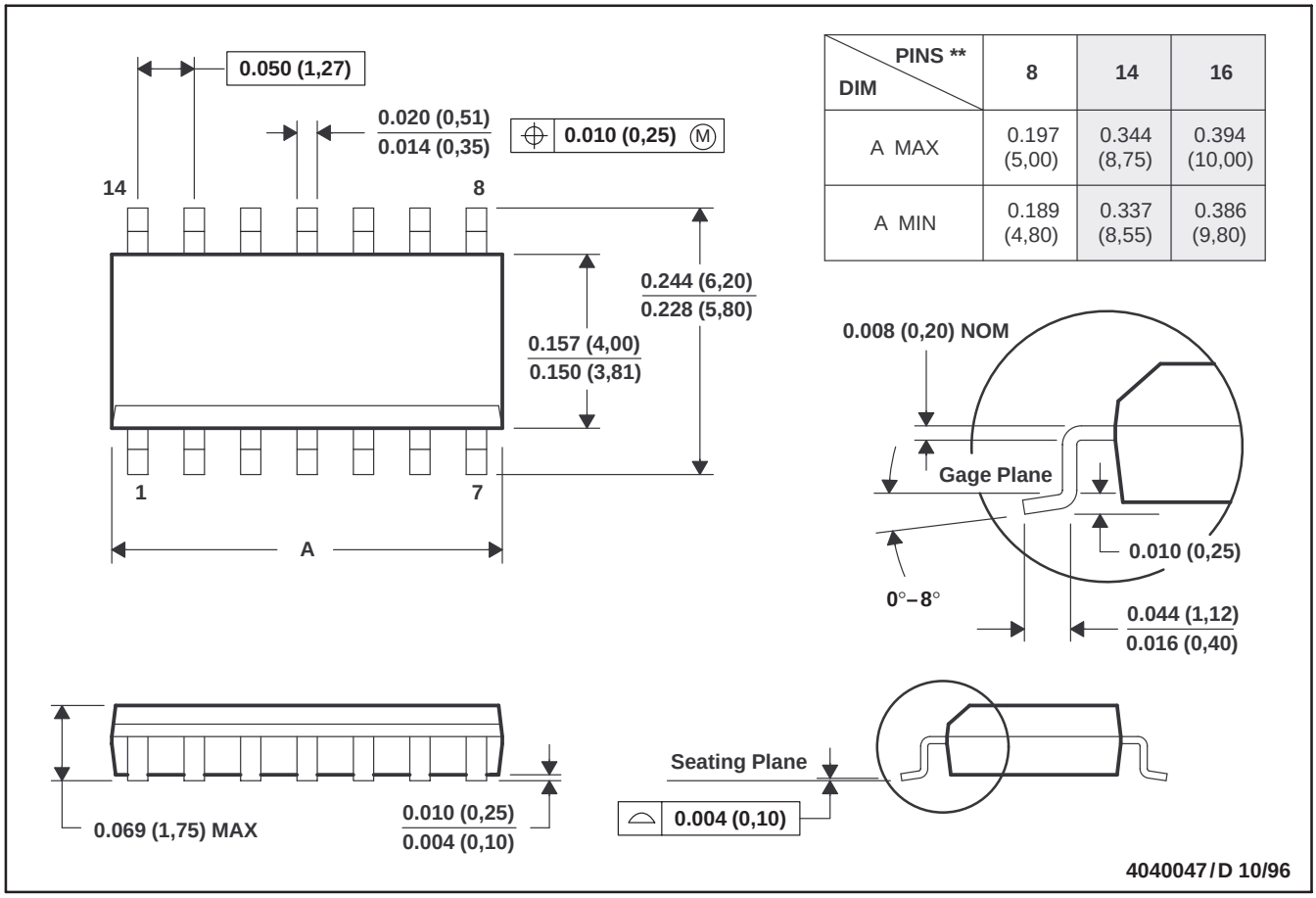


Figure 61. THS4031 Evaluation Board

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

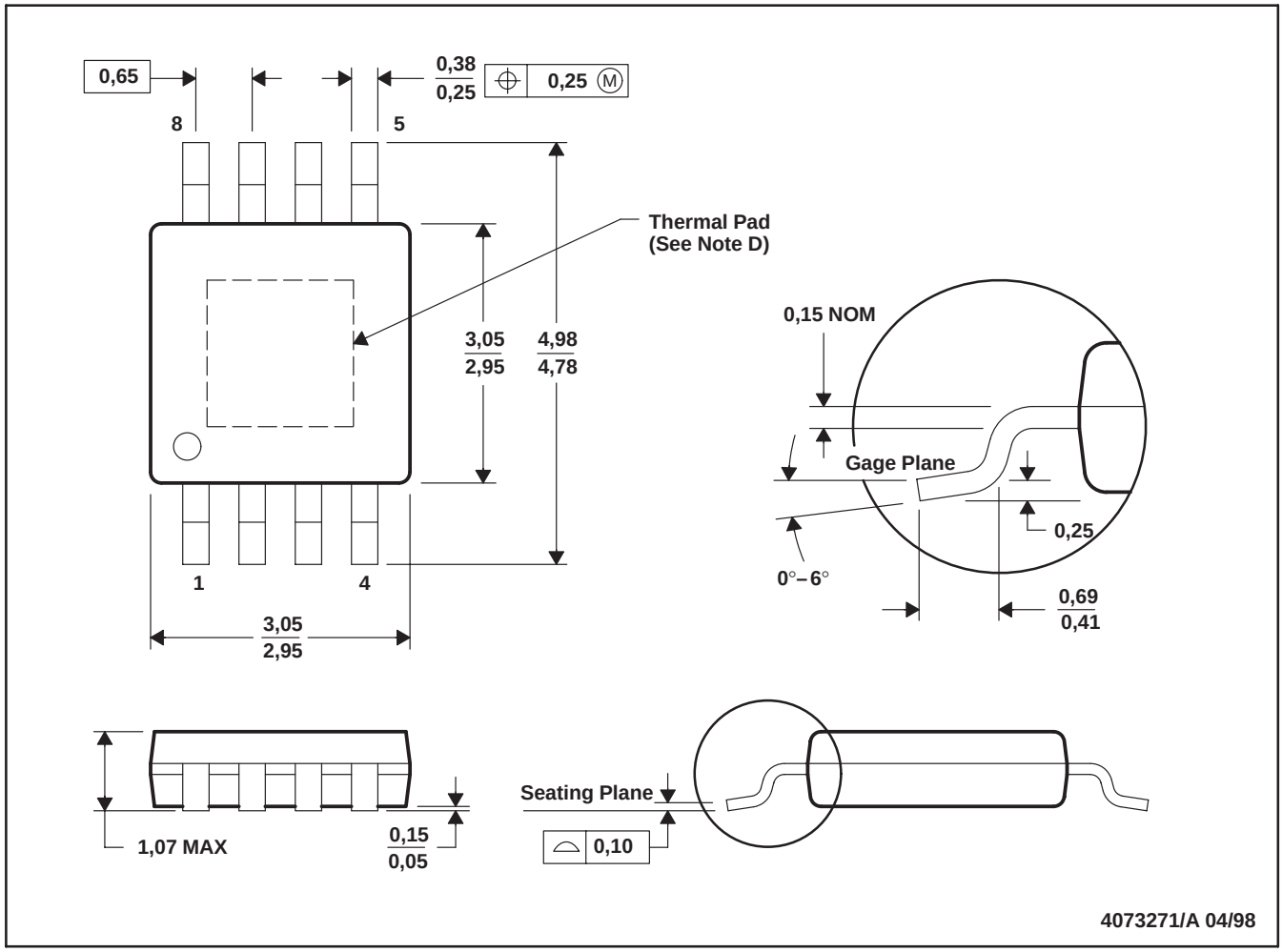


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



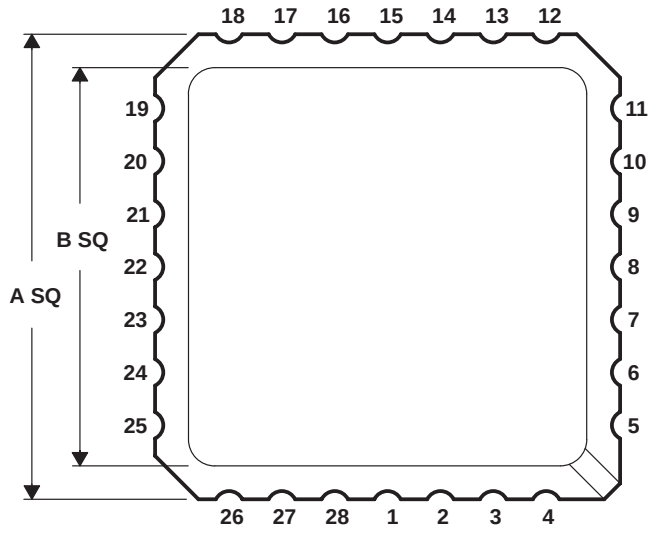
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.

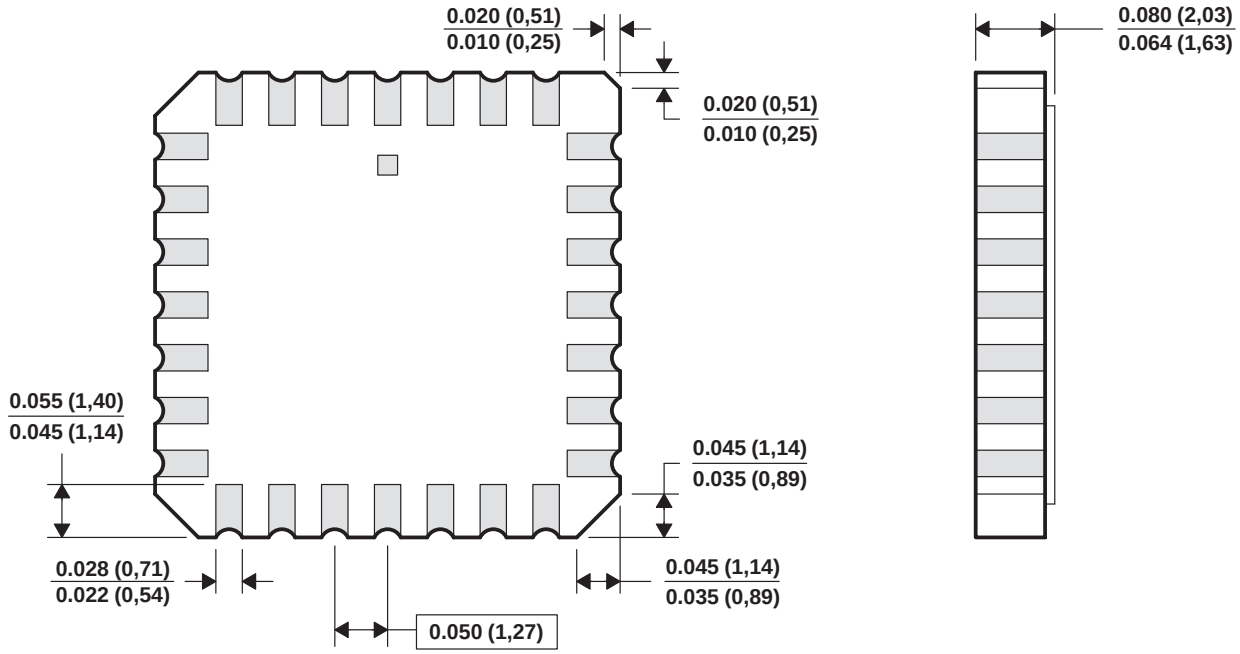
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

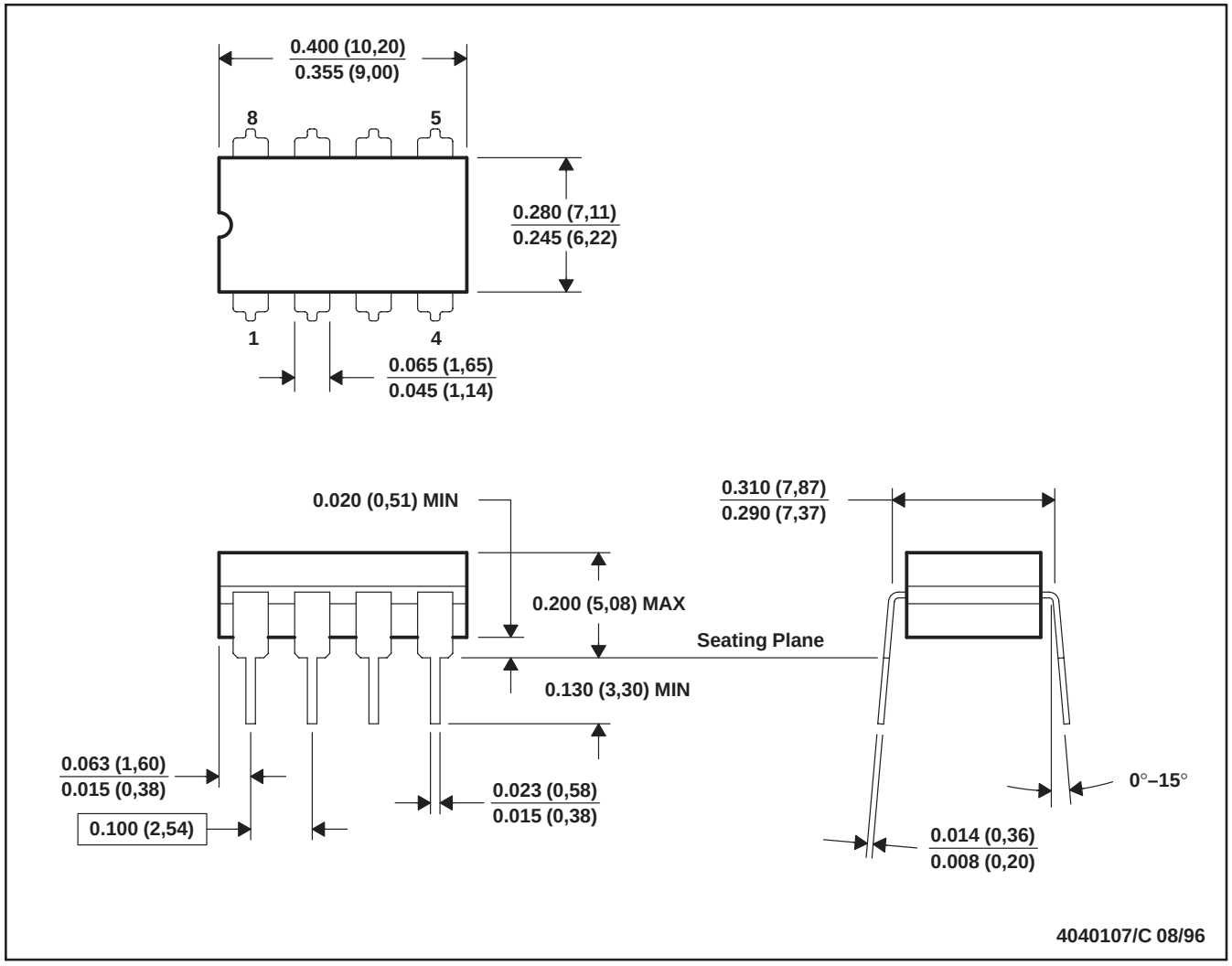


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

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