TM124BBJ32F, TM124BBJ32U 1048576 BY 32-BIT DYNAMIC RAM MODULE
TM248CBJ32F, TM248CBJ32U 2097152 BY 32-BIT DYNAMIC RAM MODULE

SMMS661 – JANUARY 1996

- **Organization**
  TM124BBJ32F . . . 1 048 576 × 32
  TM248CBJ32F . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Socket**
- **TM124BBJ32F – Utilizes Two 16-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBJ32F – Utilizes Four 16-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
’124BBJ32F-60	60 ns	30 ns	15 ns	110 ns
’124BBJ32F-70	70 ns	35 ns	18 ns	130 ns
’124BBJ32F-80	80 ns	40 ns	20 ns	150 ns
’248CBJ32F-60	60 ns	30 ns	15 ns	110 ns
’248CBJ32F-70	70 ns	35 ns	18 ns	130 ns
’248CBJ32F-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:**†
  TM124BBJ32F
  TM248CBJ32F
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM124BBJ32U
  TM248CBJ32U

description

TM124BBJ32F

The TM124BBJ32F is a 4-MByte dynamic random-access memory (DRAM) organized as four times 1048576 × 8 in a 72-pin SIMM. The SIMM is composed of two TMS418160DZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ is described in the TMS418160 data sheet. The TM124BBJ32F SIMM is available in the single-sided BJ-leadless module for use with sockets.

TM248CBJ32F

The TM248CBJ32F is an 8-MByte DRAM organized as four times 2 097 152 × 8 in a 72-pin SIMM. The SIMM is composed of four TMS418160DZ, 1048576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160DZ is described in the TMS418160 data sheet. The TM248CBJ32F SIMM is available in the double-sided BJ-leadless module for use with sockets.

operation

The TM124BBJ32F operates as two TMS418160DZs connected as shown in the functional block diagram and Table 1. The TM248CBJ32F operates as four TMS418160DZs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

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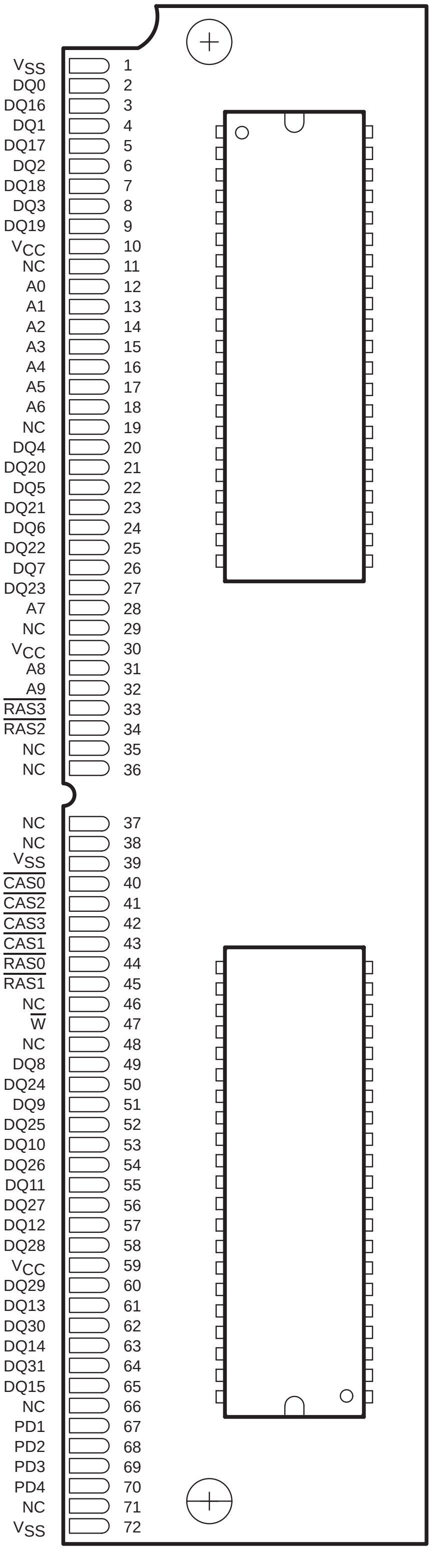
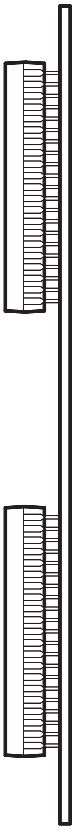
† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

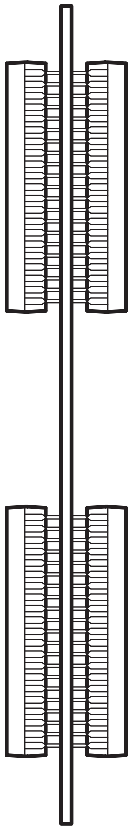
BJ SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124BBJ32F
(SIDE VIEW)



TM248CBJ32F
(SIDE VIEW)



PIN NOMENCLATURE	
A0 – A9	Address Inputs
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column-Address Strobe
DQ0 – DQ31	Data In/Data Out
NC	No Connection
PD1 – PD4	Presence Detects
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBJ32F	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248CBJ32F	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

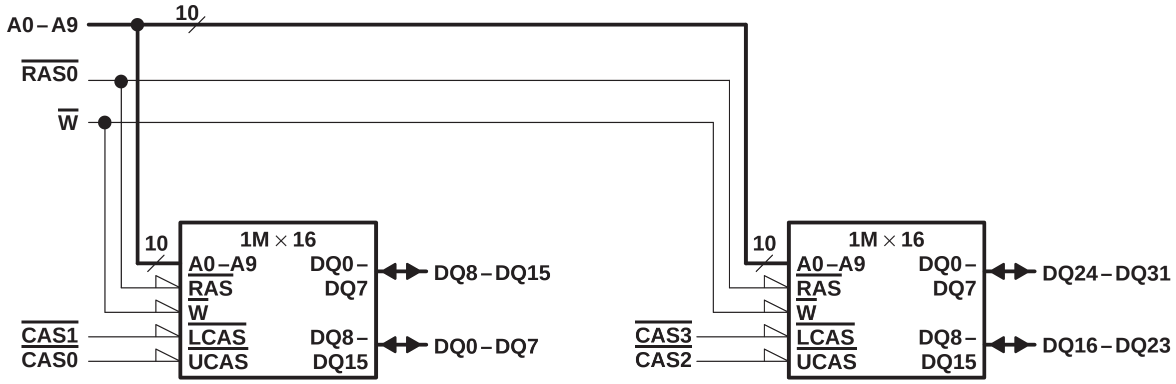
DATA BLOCK	$\overline{\mathrm{RAS}}$x		$\overline{\mathrm{CAS}}$x
	SIDE 1	SIDE 2[†]	
DQ0 – DQ7	$\overline{\mathrm{RAS0}}$	$\overline{\mathrm{RAS1}}$	$\overline{\mathrm{CAS0}}$
DQ8 – DQ15	$\overline{\mathrm{RAS0}}$	$\overline{\mathrm{RAS1}}$	$\overline{\mathrm{CAS1}}$
DQ16 – DQ23	$\overline{\mathrm{RAS2}}$	$\overline{\mathrm{RAS3}}$	$\overline{\mathrm{CAS2}}$
DQ24 – DQ31	$\overline{\mathrm{RAS2}}$	$\overline{\mathrm{RAS3}}$	$\overline{\mathrm{CAS3}}$

[†] Side 2 applies to the TM248CBJ32F only.

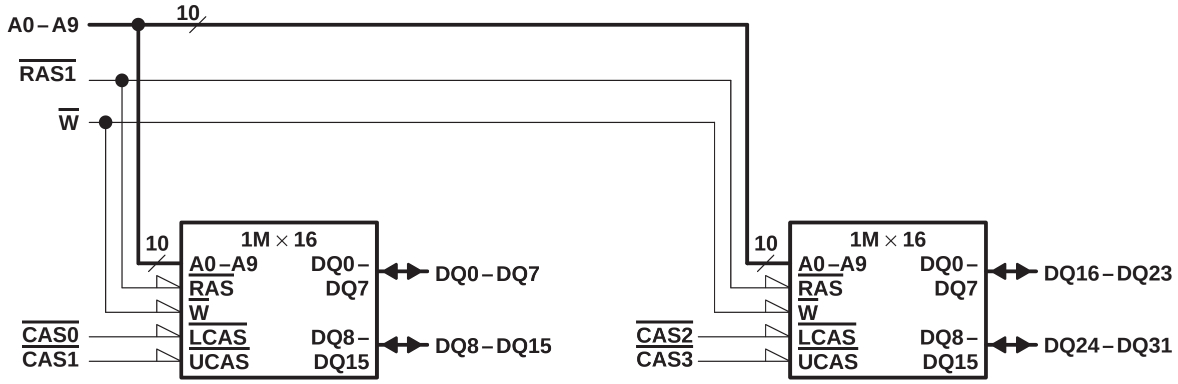
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124BBJ32F and TM248CBJ32F: Nickel plate and gold plate over copper
Contact area for TM124BBJ32U and TM248CBJ32U: Nickel plate and tin/lead over copper

functional block diagram (TM124BBJ32F and TM248CBJ32F, side 1)



functional block diagram (TM248CBJ32F, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		– 1 V to 7 V
Voltage range on any pin (see Note 1)		– 1 V to 7 V
Short-circuit output current		50 mA
Power dissipation:	TM124BBJ32F, TM124BBJ32U	2 W
	TM248CBJ32F, TM248CBJ32U	4 W
Operating free-air temperature range, T_A		0°C to 70°C
Storage temperature range, T_{stg}		– 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	’124BBJ32F-60		’124BBJ32F-70		’124BBJ32F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{\text{CAS}}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		380		360		340	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		4		4		4	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{\text{RAS}}$ only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)		380		360		340	mA
I_{CC4}	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling		200		180		160	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		’248CBJ32F-60		’248CBJ32F-70		’248CBJ32F-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}	V_I = 0 V to 6.5 V,		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC},	$\overline{\text{CAS}}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V,	Minimum cycle		384		364		344	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			8		8		8	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			4		4		4	mA
I_{CC3}	Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)	Minimum cycle,		760		720		680	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $\overline{\text{RAS}}$ low,	t_{PC} = MIN, $\overline{\text{CAS}}$ cycling		204		184		164	mA

† For test conditions shown as MIN / MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		’124BBJ32F		’248CBJ32F		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0 – A9		17		27	pF
$C_{i(R)}$	Input capacitance, $\overline{\text{RAS}}$ inputs		10		10	pF
$C_{i(C)}$	Input capacitance, $\overline{\text{CAS}}$ inputs		12		19	pF
$C_{i(W)}$	Input capacitance, $\overline{\text{W}}$		21		35	pF
$C_{o(DQ)}$	Output capacitance on DQ0 – DQ31		10		17	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’124BBJ32F-60 ’248CBJ32F-60		’124BBJ32F-70 ’248CBJ32F-70		’124BBJ32F-80 ’248CBJ32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{\text{CAS}}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{\text{CAS}}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’124BBJ32F-60 ’248CBJ32F-60		’124BBJ32F-70 ’248CBJ32F-70		’124BBJ32F-80 ’248CBJ32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{\text{RAS}}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{\text{CAS}}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{\text{RAS}}$ high from $\overline{\text{CAS}}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{\text{CAS}}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns

NOTES: 7. All cycles assume $t_T = 5$ ns.
8. To assure t_{PC} min, t_{ASC} should be $\geq t_{CP}$.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

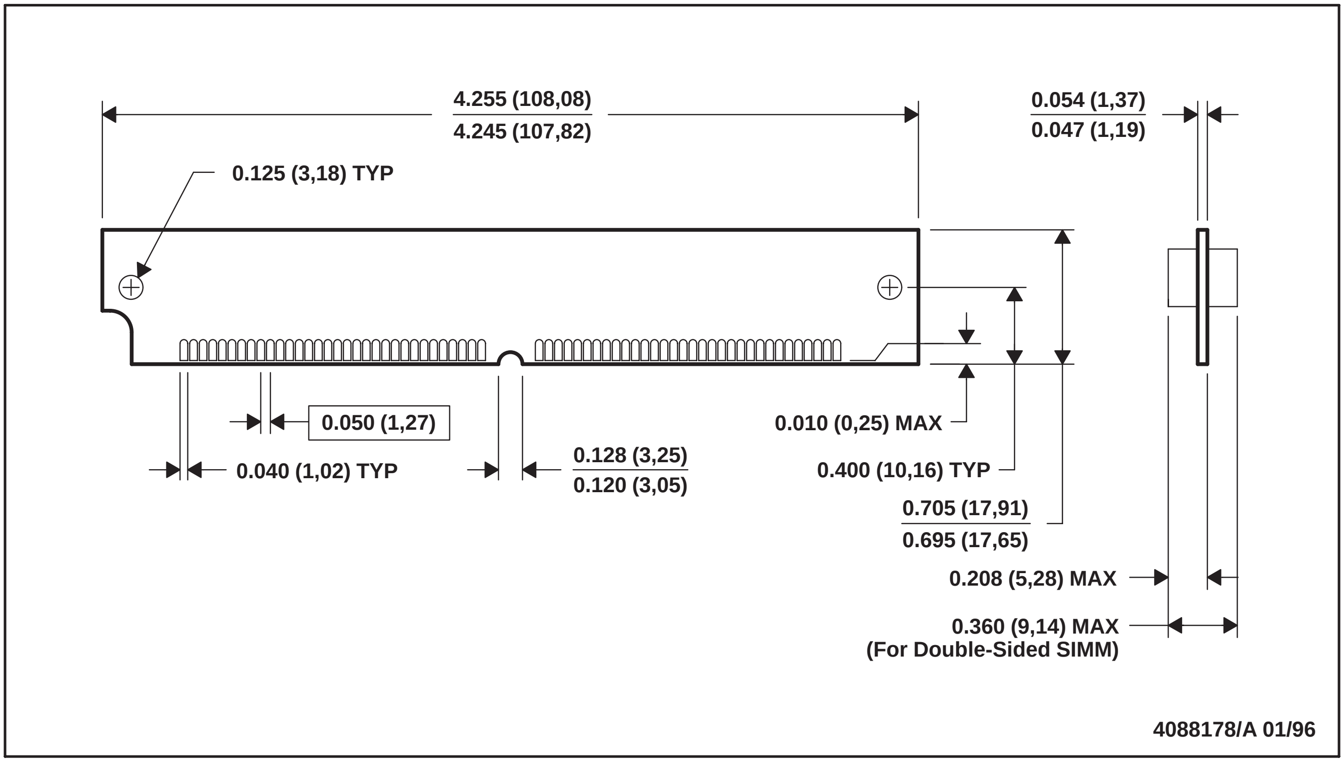
timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’124BBJ32F-60 ’248CBJ32F-60		**’124BBJ32F-70 ’248CBJ32F-70**		**’124BBJ32F-80 ’248CBJ32F-80**		**UNIT**
		MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
t_{WCH}	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low	10		15		15		ns
t_{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

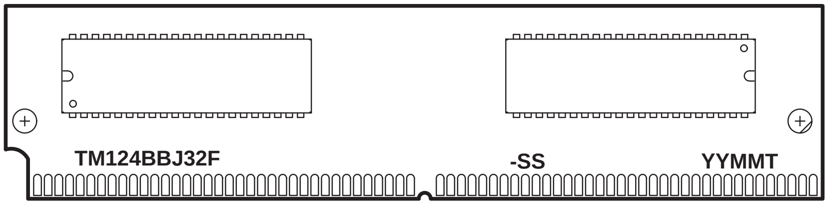
MECHANICAL DATA

BJ (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization (TM124BBJ32F illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

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