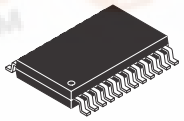
TEXAS INSTRUMENTS



SLOS398A – DECEMBER 2002 – REVISED APRIL 2003

20-W MONO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- 20 W Into 8-Ω Load From 18-V Supply (10% THD+N)
- Short Circuit Protection (Short to V_{CC}, Short to GND, Short Between Outputs)
- Third-Generation Modulation Technique:
  - Replaces Large LC Filter With Small, Low-Cost Ferrite Bead Filter in Most Applications
  - Improved Efficiency
  - Improved SNR
- Low Supply Current . . . 8 mA Typ at 12 V
- Shutdown Control . . . <1 μA Typ
- Space-Saving, Thermally-Enhanced PowerPAD™ Packaging

APPLICATIONS

- LCD Monitors/TVs
- Hands-Free Car Kits
- Powered Speakers

DESCRIPTION

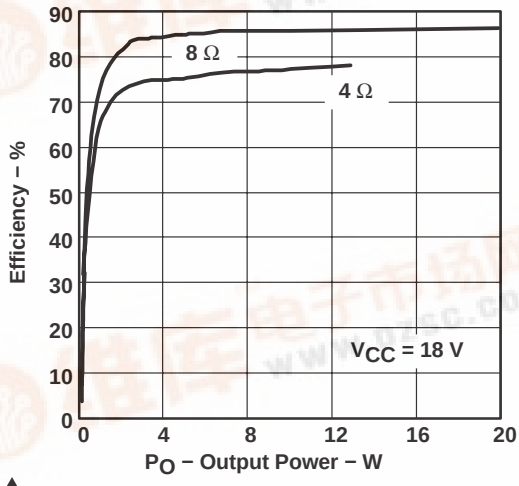
The TPA3001D1 is a 20-W mono bridge-tied load (BTL) class-D audio power amplifier with high efficiency, eliminating the need for heat sinks. The TPA3001D1 can drive 4-Ω or 8-Ω speakers with only a ferrite bead filter required to reduce EMI.

The gain of the amplifier is controlled by two input terminals, GAIN1 and GAIN0. This allows the amplifier to be configured for a gain of 12, 18, 23.6, and 36 dB. The differential input stage provides high common mode rejection and improved power supply rejection.

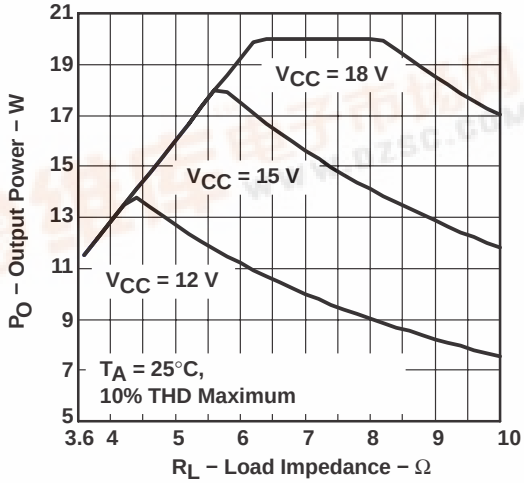
The amplifier also includes depop circuitry to reduce the amount of pop at power-up and when cycling SHUTDOWN.

The TPA3001D1 is available in the 24-pin thermally enhanced TSSOP package (PWP) which eliminates the need for an external heat sink.

EFFICIENCY vs OUTPUT POWER



MAXIMUM OUTPUT POWER vs LOAD IMPEDANCE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

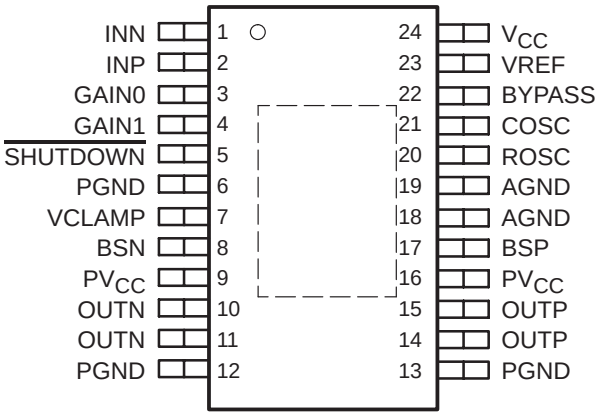
PowerPAD is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PWP)†
−40°C to 85°C	TPA3001D1PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3001D1PWPR).

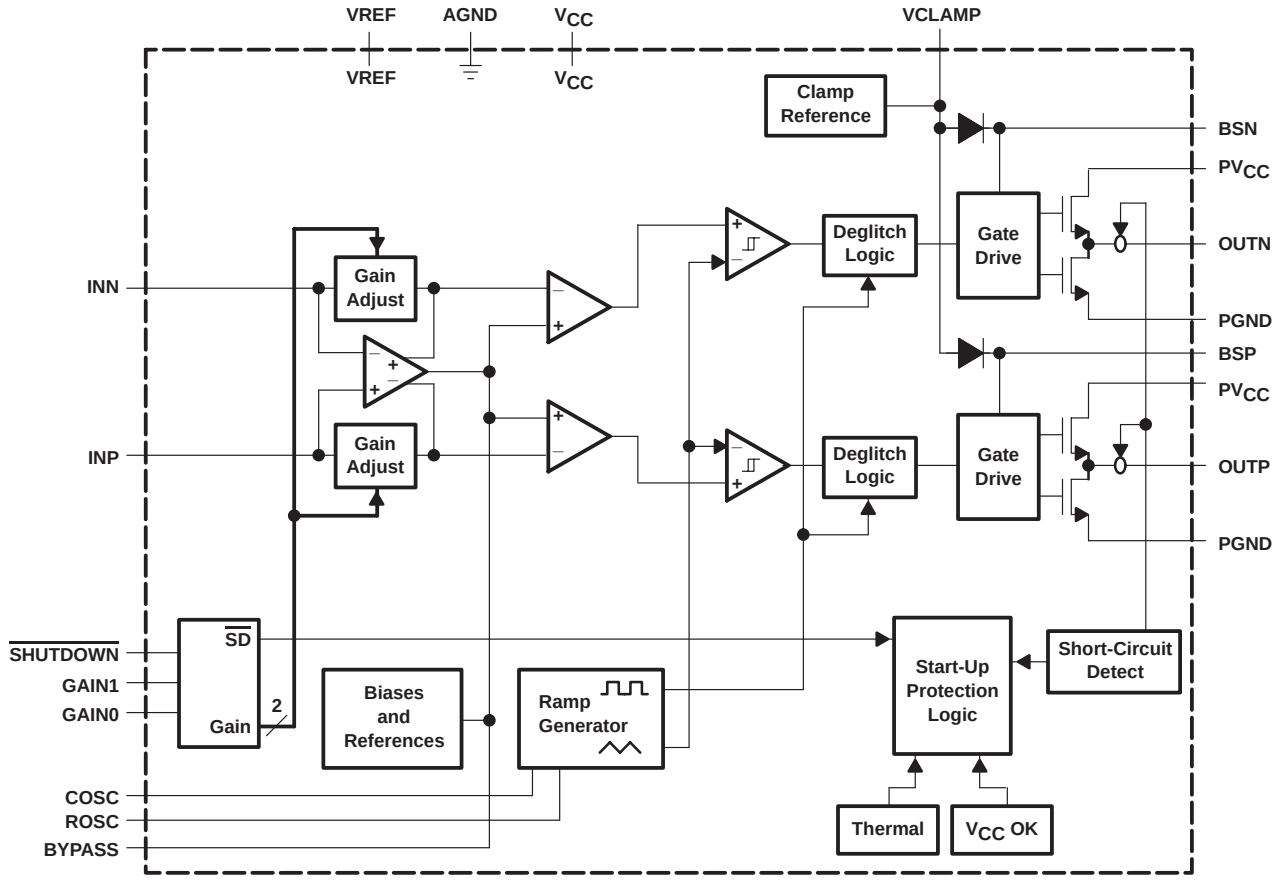
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	18, 19		Analog ground terminal
BSN	8	I	Bootstrap terminal for high-side gate drive of negative BTL output (connect a 0.22-µF capacitor with a 51-Ω resistor in series from OUTN to BSN)
BSP	17	I	Bootstrap terminal for high-side gate drive of positive BTL output (connect a 0.22-µF capacitor with a 51-Ω resistor in series from OUTP to BSP)
BYPASS	22	I	Connect 1-µF capacitor to ground for BYPASS voltage filtering
COSC	21	I	Connect a 220-pF capacitor to ground to set oscillation frequency
GAIN0	3	I	Bit 0 of gain control (see Table 1 for gain settings)
GAIN1	4	I	Bit 1 of gain control (see Table 1 for gain settings)
INN	1	I	Negative differential input
INP	2	I	Positive differential input
OUTN	10, 11	O	Negative BTL output, connect Schottky diode from PGND to OUTN for short-circuit protection
OUTP	14, 15	O	Positive BTL output, connect Schottky diode from PGND to OUTP for short-circuit protection
PGND	6, 12, 13		Power ground
PV_{CC}	9, 16	I	High-voltage power supply (for output stages)
ROSC	20	I	Connect 120 kΩ resistor to ground to set oscillation frequency
$\overline{\text{SHUTDOWN}}$	5	I	Shutdown terminal (negative logic), TTL compatible, 21-V compliant
V_{CC}	24	I	Analog high-voltage power supply
VCLAMP	7	O	Connect 1-µF capacitor to ground to provide reference voltage for H-bridge gates
VREF	23	O	5-V internal regulator for control circuitry (connect a 0.1-µF to 1-µF capacitor to ground)

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC}, PV_{CC} . . . . . −0.3 V to 21 V
Load impedance, R_L . . . . . ≥3.6 Ω
Input voltage: $\overline{SHUTDOWN}$ . . . . . −0.3 V to V_{CC} + 0.3 V
GAIN0, GAIN1 . . . . . −0.3 V to 5.5 V
INN, INP . . . . . −0.3 V to 7 V
Continuous total power dissipation . . . . . (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Operating junction temperature range, T_J . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	4.16 W	33.33 mW/°C‡	2.67 W	2.16 W

‡ The PowerPAD must be soldered to a thermal land on the printed circuit board. Please refer to the *PowerPAD Thermally Enhanced Package* application note (SLMA002).

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}, PV_{CC}	$R_L \geq 3.6\ \Omega$†	8	18	V
Load impedance, R_L		3.6		Ω
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$		0.8	V
Operating free-air temperature, T_A		−40	85	°C

† The TPA3001D1 must not be used with any speaker or load (including speaker with output filter) that could vary below 3.6 Ω over the audio frequency band.

electrical characteristics at T_A = 25°C, PV_{CC} = V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0 V,	A_V = 12 dB, 18, 23.6 dB			50	mV
		V_I = 0 V,	A_V = 36 dB			100	
PSRR	Power supply rejection ratio	PV_{CC} = 11.5 V to 12.5 V			−73		dB
$\lvert I_{IH}\rvert$	High-level input current	PV_{CC} = 12 V,	$V_I = PV_{CC}$			1	µA
$\lvert I_{IL}\rvert$	Low-level input current	PV_{CC} = 12 V,	V_I = 0 V			1	µA
I_{CC}	Supply current	$\overline{\text{SHUTDOWN}}$ = 2.0 V, No load			8	15	mA
		$\overline{\text{SHUTDOWN}}$ = V_{CC}, V_{CC} = 18 V, P_O = 20 W, R_L = 8 Ω			1.3		A
$I_{CC(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0.8 V			1	2	µA
f_s	Switching frequency	R_{OSC} = 120 kΩ,	C_{OSC} = 220 pF		250		kHz
$r_{ds(on)}$	Output transistor on resistance (total)	I_O = 1 A, T_J = 25°C		0.2	0.3	0.7	Ω
G	Gain	GAIN1 = 0.8 V, GAIN0 = 0.8 V		10.9	12	12.8	dB
		GAIN1 = 0.8 V, GAIN0 = 2 V		17.1	18	18.5	dB
		GAIN1 = 2 V, GAIN0 = 0.8 V		23	23.6	24.3	dB
		GAIN1 = 2 V, GAIN0 = 2 V		33.9	36	36.5	dB

operating characteristics, PV_{CC} = V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Continuous output power at 10% THD+N	f = 1 kHz,	R_L = 4 Ω		12.8		W
		f = 1 kHz,	R_L = 8 Ω		9		
	Continuous output power at 1% THD+N	f = 1 kHz,	R_L = 4 Ω		10.3		
		f = 1 kHz,	R_L = 8 Ω		7.2		
THD + N	Total harmonic distortion plus noise	P_O = 10 W, R_L = 4 Ω,	f = 20 Hz to 20 kHz		0.2%		
B_{OM}	Maximum output power bandwidth	THD = 1%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	$C_{(BYPASS)}$ = 1 µF		−70		dB
SNR	Signal-to-noise ratio	P_O = 10 W, R_L = 4 Ω			95		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 1 µF, No weighting filter used,	f = 20 Hz to 22 kHz, Gain = 12 dB		86		µV(rms)
					−81		dBV
		$C_{(BYPASS)}$ = 1 µF, A-weighted filter,	f = 20 Hz to 22 kHz, Gain = 12 dB		66		µV(rms)
					−84		dBV
Z_i	Input impedance	See Table 1, page 21			>23		kΩ

operating characteristics, $PV_{CC} = V_{CC} = 18$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power at 10% THD+N	f = 1 kHz,	$R_L = 4\ \Omega$		12.8		W
		f = 1 kHz,	$R_L = 8\ \Omega$		20		
	Output power at 1% THD+N	f = 1 kHz,	$R_L = 4\ \Omega$		10.3		
		f = 1 kHz,	$R_L = 8\ \Omega$		16		
THD + N	Total harmonic distortion plus noise	P_O = 15 W, $R_L = 8\ \Omega$	f = 20 Hz to 20 kHz		1%		
		P_O = 2 W, $R_L = 8\ \Omega$	f = 20 Hz to 20 kHz		0.3%		
B_{OM}	Maximum output power bandwidth	THD = 1%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	C_{BYPASS} = 1 µF		−70		dB
SNR	Signal-to-noise ratio	P_O = 15 W, $R_L = 8\ \Omega$			102		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 1 µF, No weighting filter used,	f = 20 Hz to 20 kHz, Gain = 12 dB		86		µV(rms)
					−81		dBV
		$C_{(BYPASS)}$ = 1 µF, A-weighted filter,	f = 20 Hz to 22 kHz, Gain = 12 dB		66		µV(rms)
					−84		dBV
Z_i	Input impedance	See Table 1, page 21			>23		kΩ

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Output power	1
P_O	Output power	vs Load Impedance	2, 3, 4
I_{CC}	Supply current	vs Supply voltage	5
$I_{CC(SD)}$	Shutdown current		6
THD+N	Total harmonic distortion + noise	vs Output power	7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18
		vs Frequency	19, 20, 21, 22, 23, 24, 25
k_{SVR}	Supply voltage rejection ratio	vs Frequency	26
	Gain and phase		27
CMRR	Common-mode rejection ratio		28
V_{IO}	Input offset voltage	vs Common-mode input voltage	29

TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT POWER

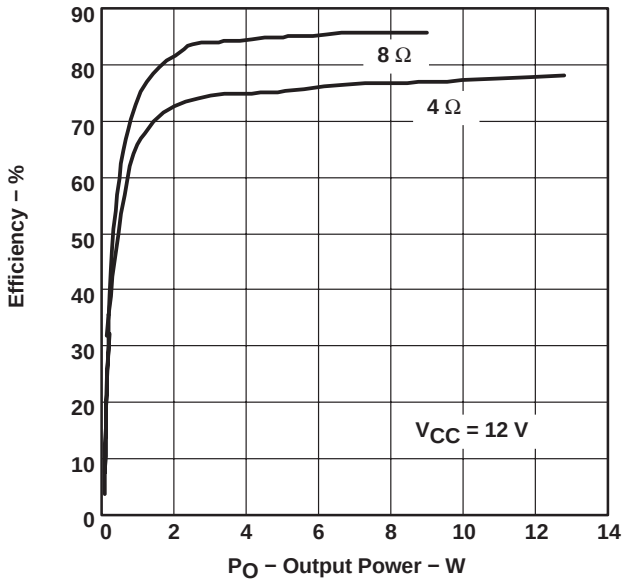


Figure 1

MAXIMUM OUTPUT POWER vs LOAD IMPEDANCE

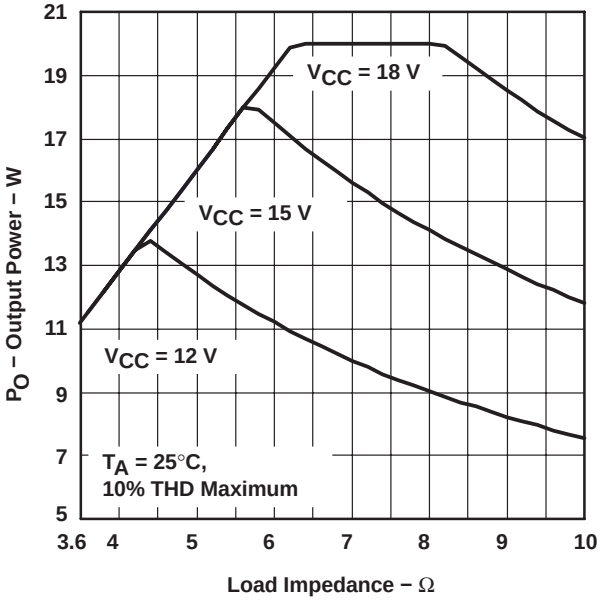


Figure 2

MAXIMUM OUTPUT POWER vs LOAD IMPEDANCE

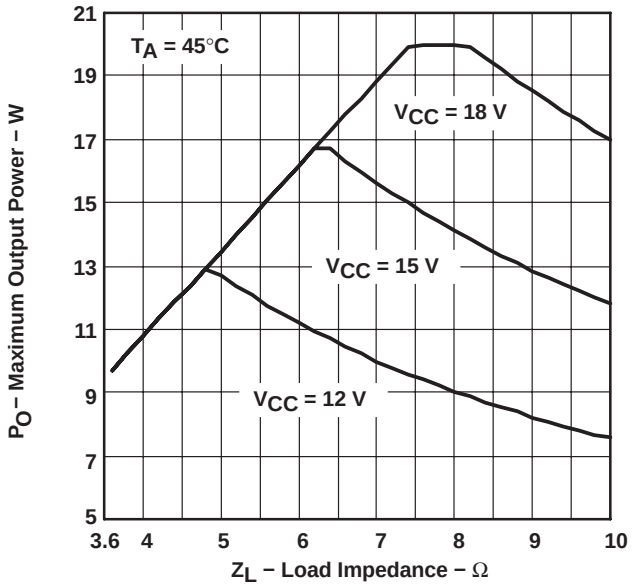


Figure 3

MAXIMUM OUTPUT POWER vs LOAD IMPEDANCE

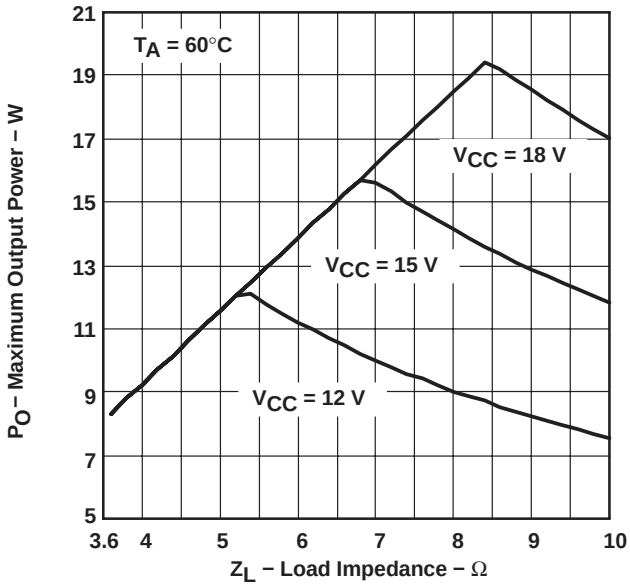


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

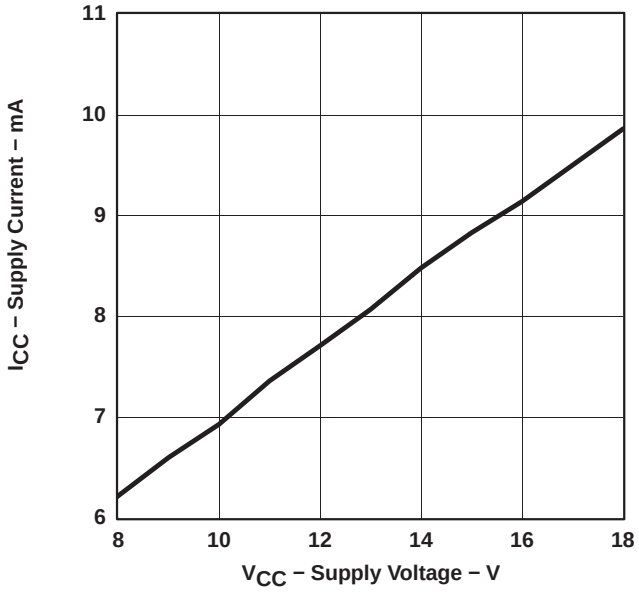


Figure 5

SHUTDOWN CURRENT vs SUPPLY VOLTAGE

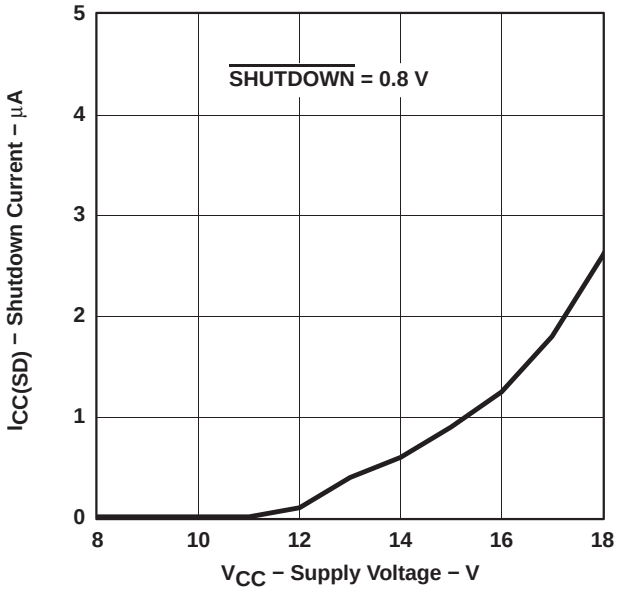


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

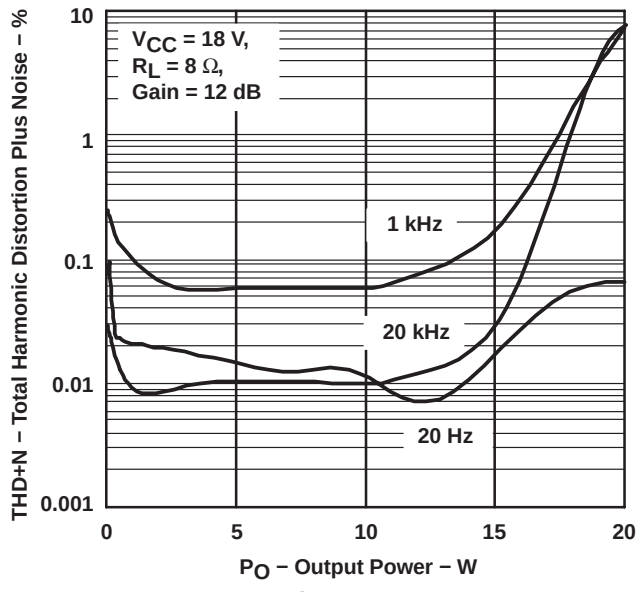


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

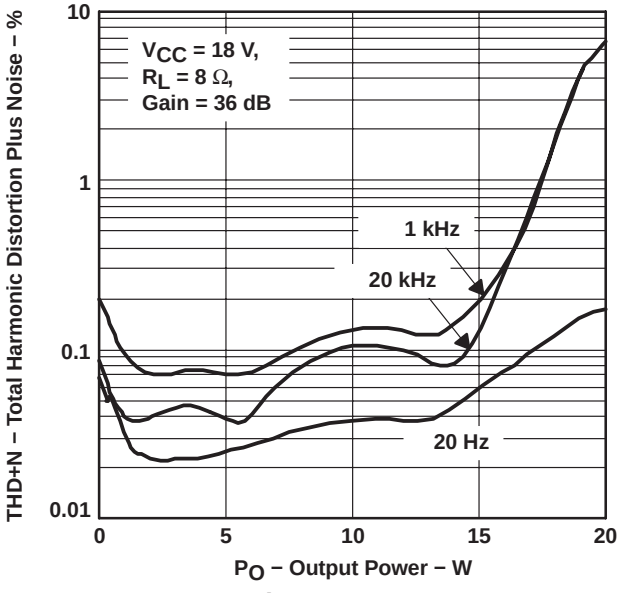


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

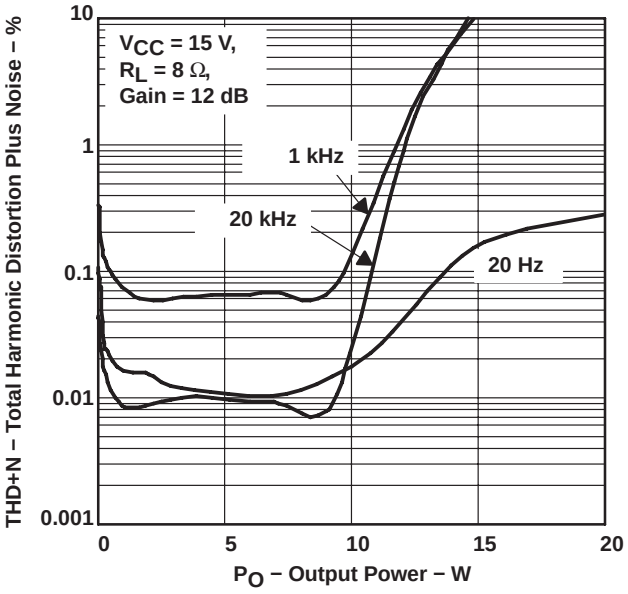


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

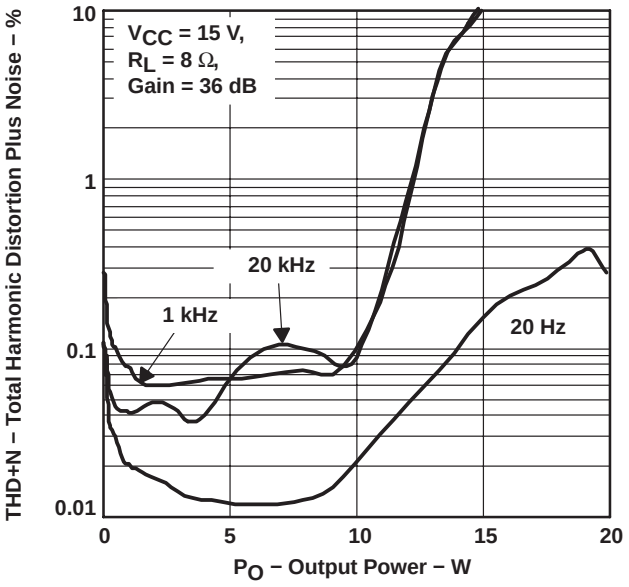


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

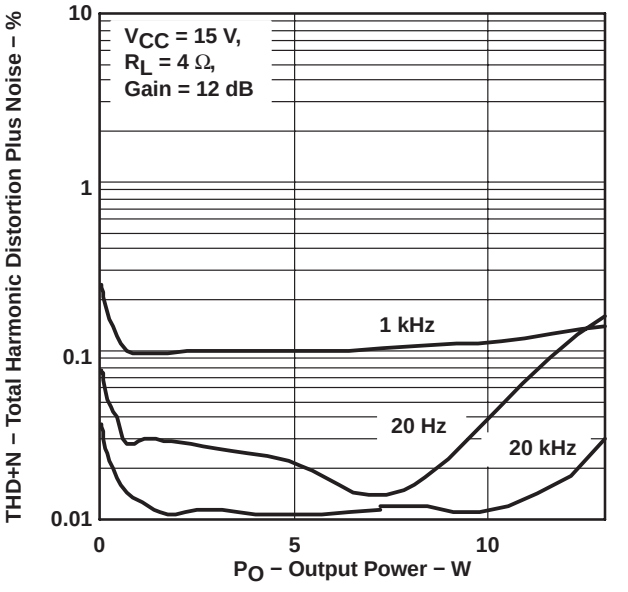


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

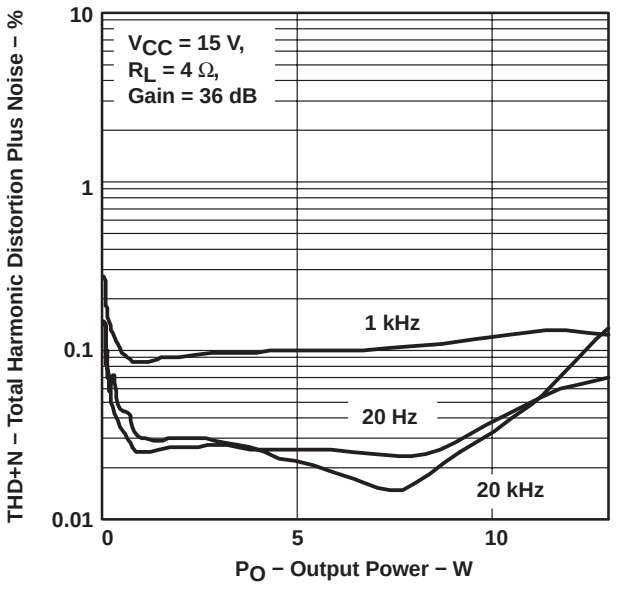


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

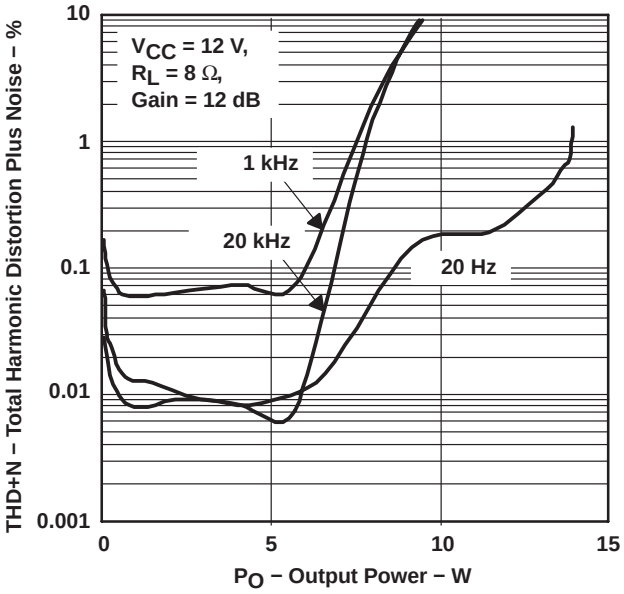


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

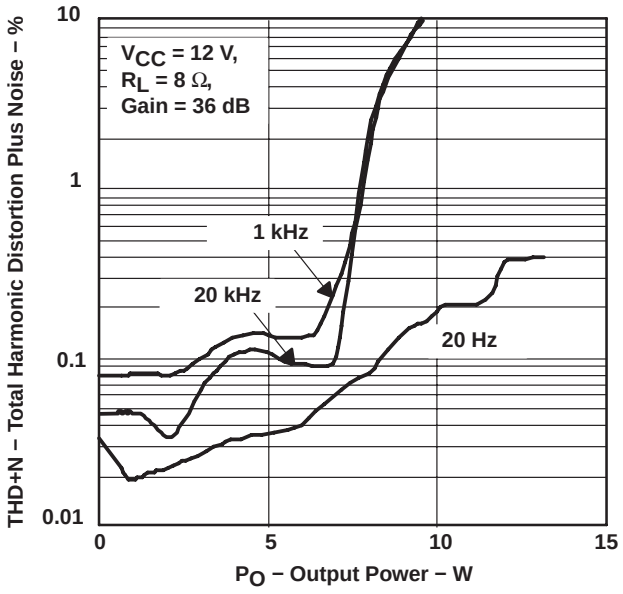


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

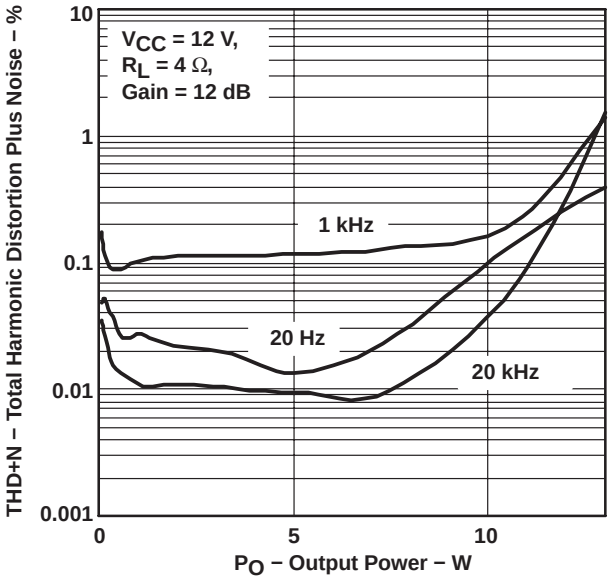


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

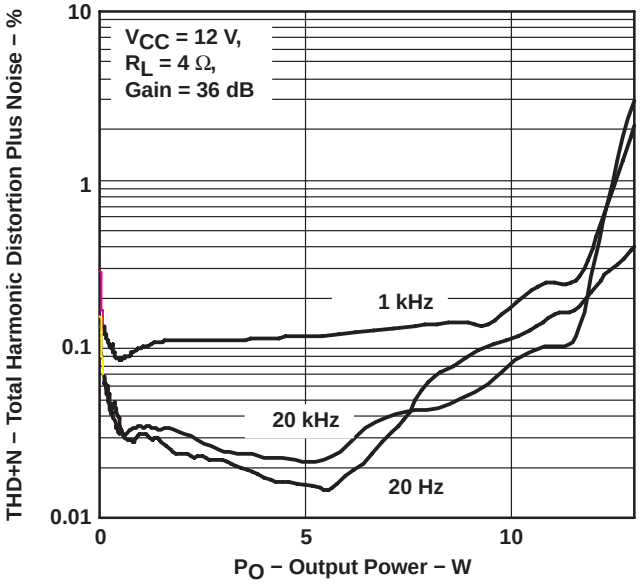


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

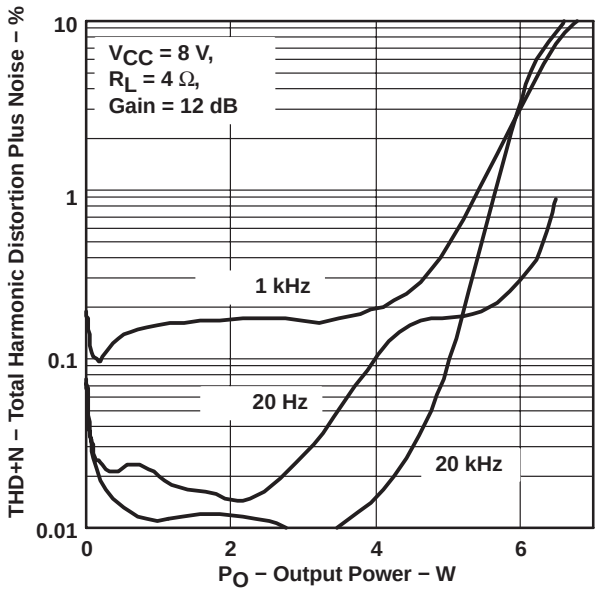


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

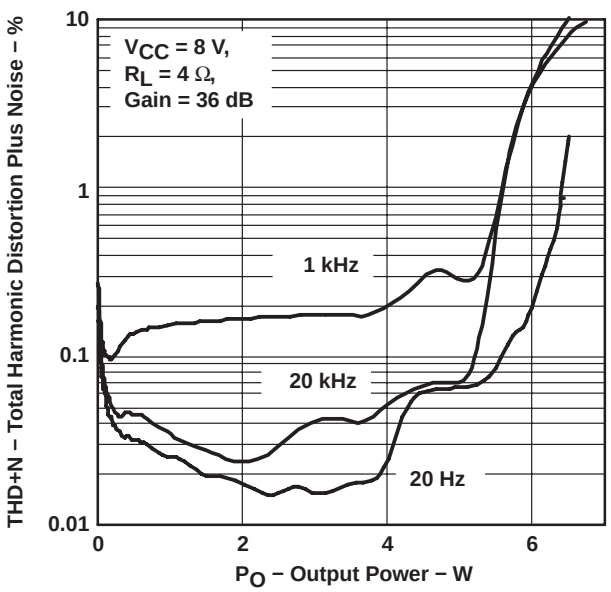


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

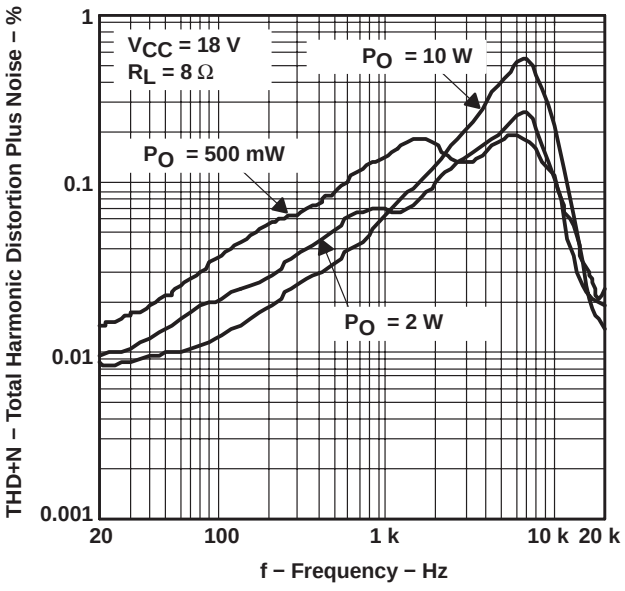


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

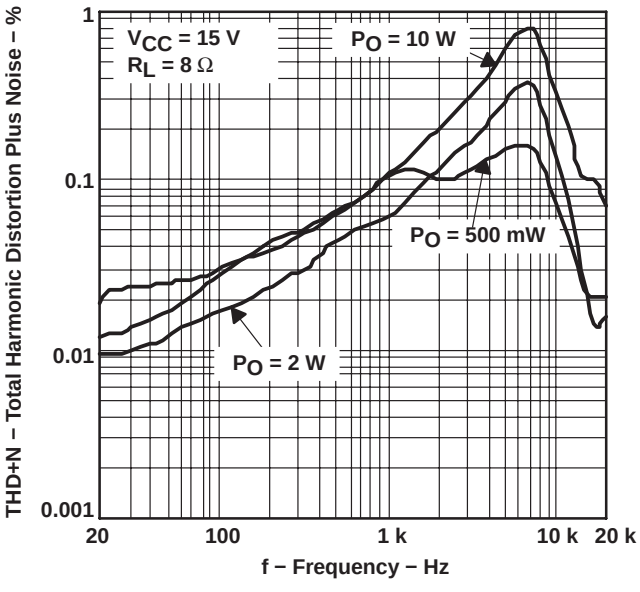


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

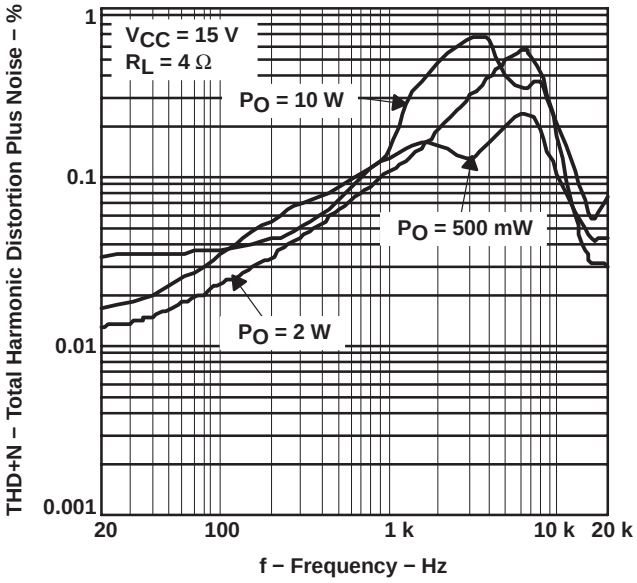


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

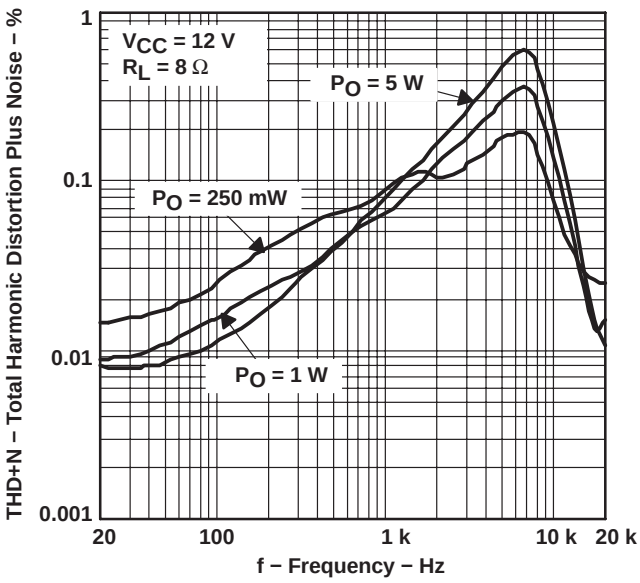


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

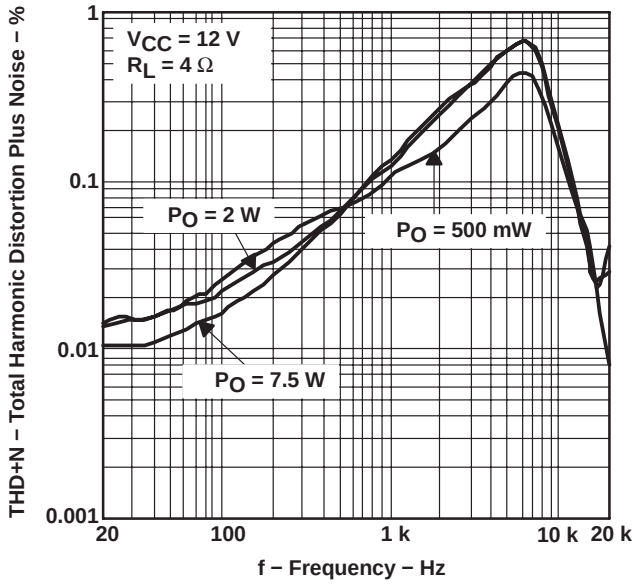


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

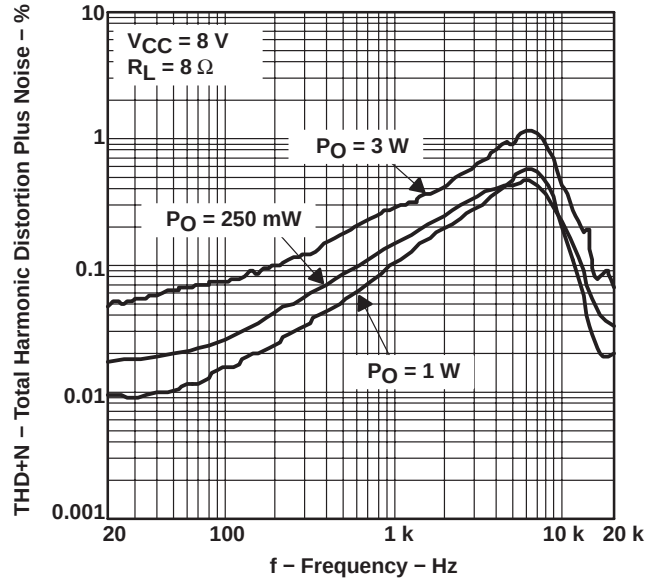


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

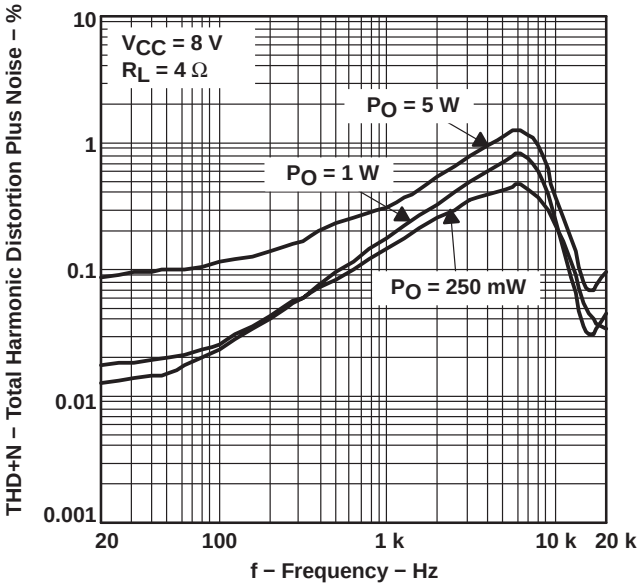


Figure 25

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

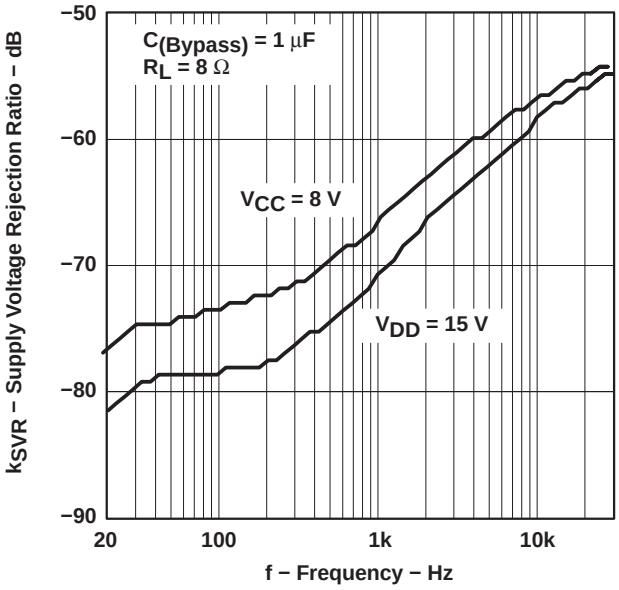


Figure 26

GAIN and PHASE vs FREQUENCY

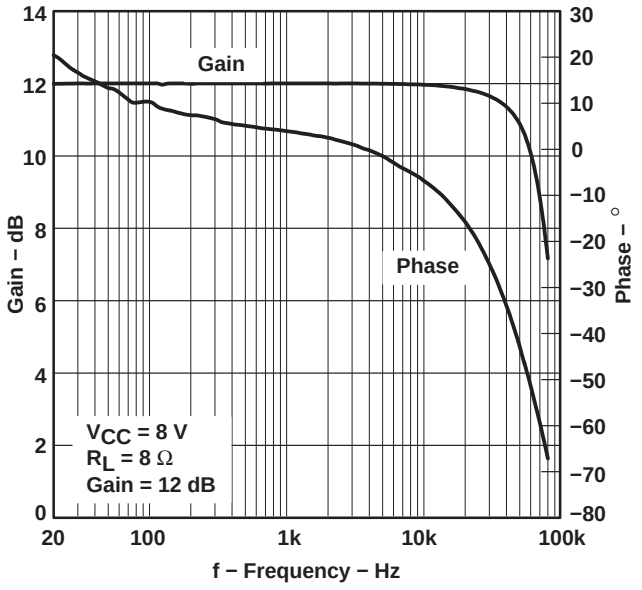


Figure 27

COMMON-MODE REJECTION RATIO vs FREQUENCY

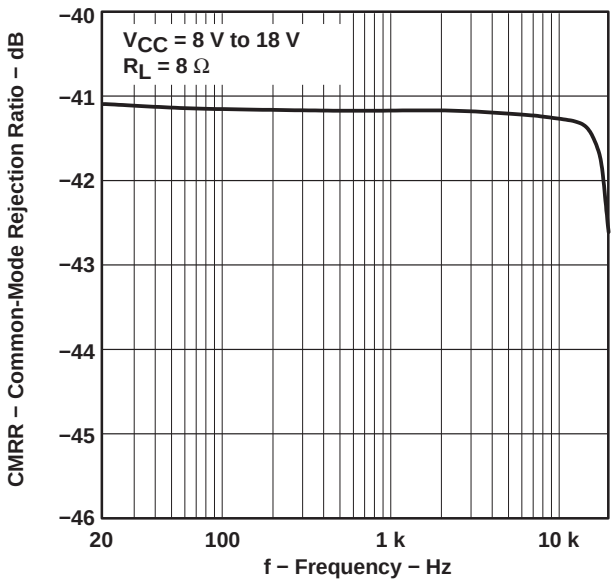


Figure 28

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

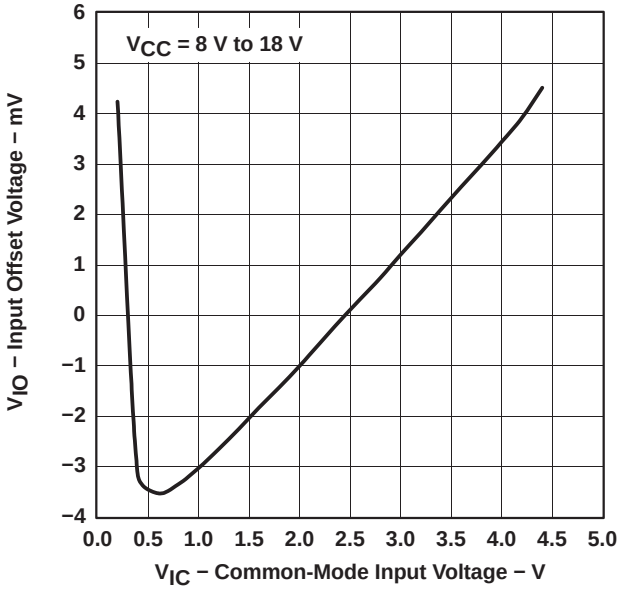


Figure 29

APPLICATION INFORMATION

application circuit

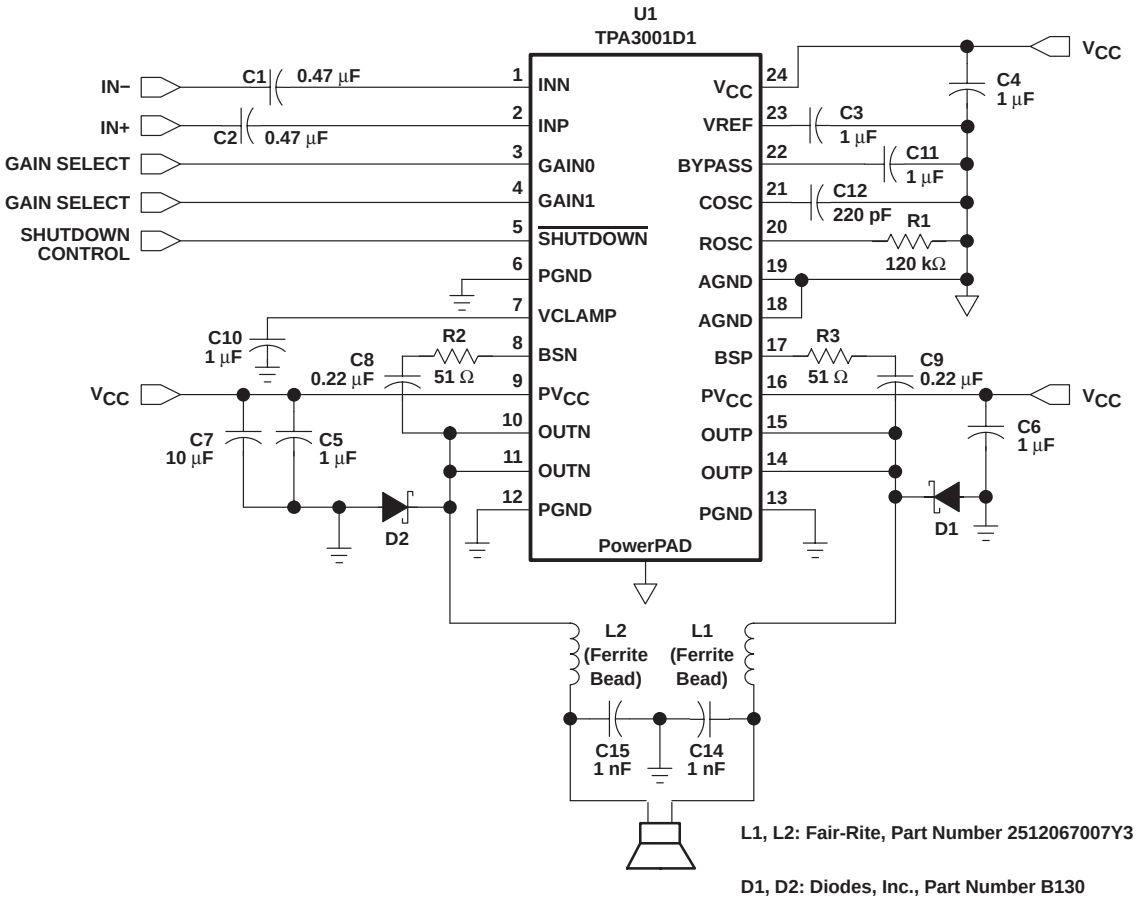


Figure 30. Typical Application Circuit

APPLICATION INFORMATION

class-D operation

This section focuses on the class-D operation of the TPA3001D1.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 31. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

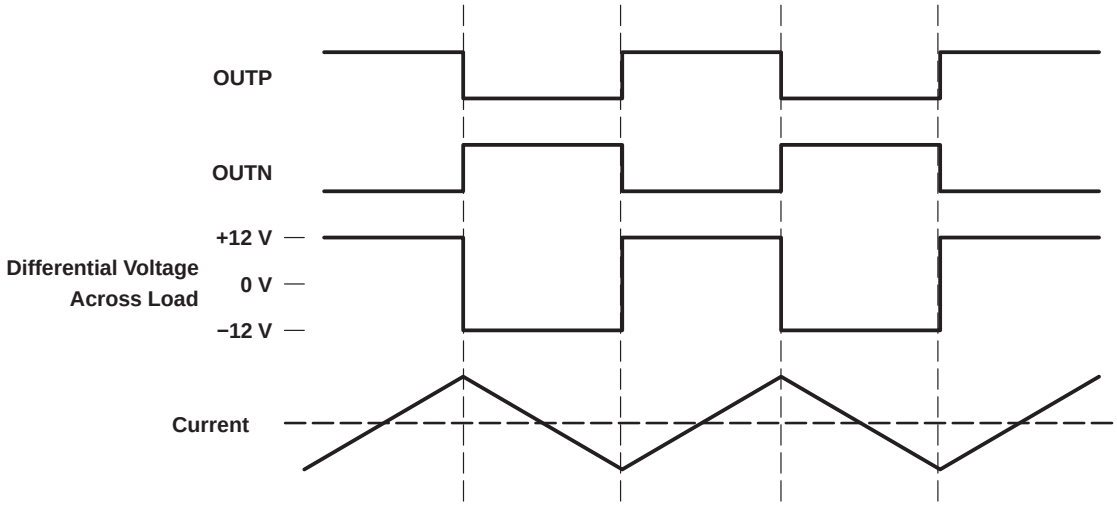


Figure 31. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3001D1 modulation scheme

The TPA3001D1 uses a modulation scheme that still has each output switching from ground to V_{CC}. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load is 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load. (See Figure 32 on the following page.)

APPLICATION INFORMATION

TPA3001D1 modulation scheme (continued)

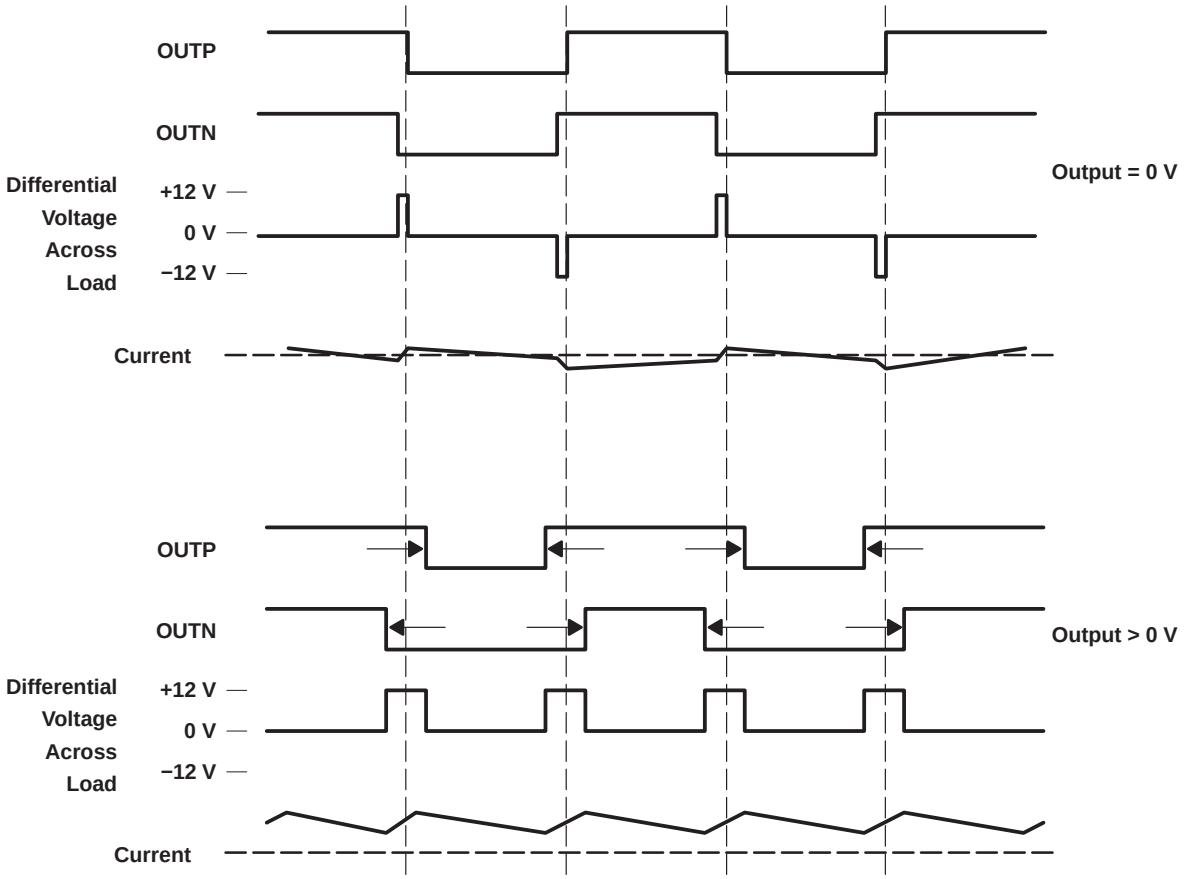


Figure 32. The TPA3001D1 Output Voltage and Current Waveforms Into an Inductive Load

APPLICATION INFORMATION

maximum allowable output power (safe operating area)

The TPA3001D1 can drive load impedances as low as 3.6 Ω from power supply voltages ranging from 8 V to 18 V. To prevent device failure, however, the output power of the TPA3001D1 must be limited. Figure 33 shows the maximum allowable output power versus load impedance for three power supply voltages at an ambient temperature of 25°C. (For ambient temperatures of 45°C and 60°C, see Figures 3 and 4 on page 6.)

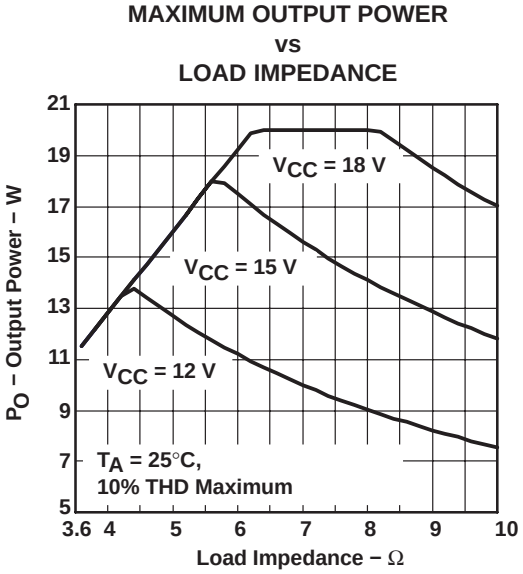


Figure 33. Output Power

driving a low-impedance load from a high power supply voltage

When driving low-impedance loads (e.g., a 4-Ω speaker), the output power can be limited by reducing the maximum audio input signal level or by reducing the gain of the TPA3001D1. The maximum input voltage may be calculated with equation 1.

$$V_{in(pp),max} = \frac{\sqrt{8 P_{O(avg),max} \times R_L}}{A_V} \quad (1)$$

where

$P_{O(avg),\,max}$ = maximum continuous output power (W)
R_L = load impedance (Ω)

A_V = voltage gain (V/V) = $10^{\left(\frac{G(dB)}{20}\right)}$

For example, consider an application in which the TPA3001D1 drives a 4-Ω speaker from an 18-V power supply. The gain is selected to be 18 dB. The maximum allowable output power for a 4-Ω load impedance is 12.8 W. From equation 1, the input voltage must not exceed 2.54 V_{pp}.

In this same example, however, if the maximum output voltage of audio signal source is 5 V_{pp}, then the gain of the TPA3001D1 should be reduced to 12 dB to eliminate the need for limiting the input signal.

APPLICATION INFORMATION

The input voltage may be limited using a variety of methods, depending on what is known about the audio signal source. If the maximum output voltage of the source is known, a resistive voltage divider in conjunction with proper TPA3001D1 gain selection may be used to prevent distortion. If the maximum audio source voltage is unknown, diodes may be used to clamp the input voltage, at the cost of distortion when the input signal level exceeds the required clamping voltage.

driving the output into clipping

The output of the TPA3001D1 may be driven into clipping to attain a higher output power than is possible with no distortion. Clipping is typically quantified by a THD measurement of 10%. The amount of additional power into the load may be calculated with equation 2.

$$P_{O(10\%\ THD)} = P_{O(1\%\ THD)} \times 1.25 \quad (2)$$

For example, consider an application in which the TPA3001D1 drives an 8-Ω speaker from an 18-V power supply. The maximum output power with no distortion (less than 1% THD) is 16 W, which corresponds to a maximum peak output voltage of 16 V. For the same output voltage level driven into clipping (10% THD), the output power is increased to 20 W.

output filter considerations

A ferrite bead filter (shown in Figure 34) should be used in order to pass FCC and/or CE radiated emissions specifications and if a frequency sensitive circuit operating higher than 1 MHz is nearby. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an additional LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires (greater than 11 inches) from the amplifier to the speaker, as shown in Figure 35 and Figure 36.

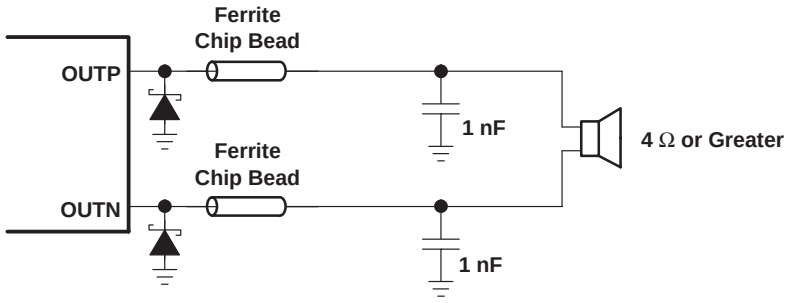


Figure 34. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

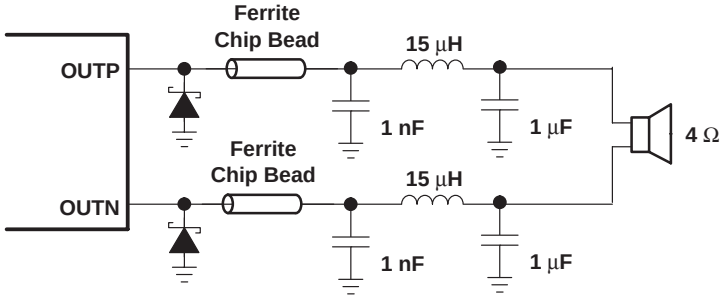


Figure 35. Typical LC Output Filter for 4-Ω Speaker, Cutoff Frequency of 41 kHz

APPLICATION INFORMATION

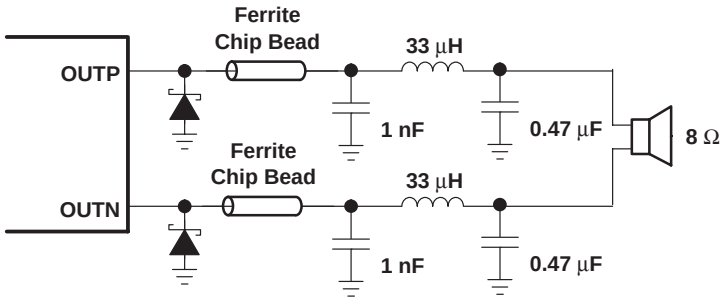


Figure 36. Typical LC Output Filter for 8-Ω Speaker, Cutoff Frequency of 41 kHz

short-circuit protection

The TPA3001D1 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive and enters into shutdown mode. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Two Schottky diodes are required to provide short-circuit protection. The diodes should be placed as close to the TPA3001D1 as possible, with the anodes connected to PGND and the cathodes connected to OUTP and OUTN as shown in the application circuit schematic. The diodes should have a forward voltage rating of 0.5V at a minimum of 1A output current and a DC blocking voltage rating of at least 30 V. The diodes must also be rated to operate at a junction temperature of 150°C.

If short-circuit protection is not required, the Schottky diodes may be omitted.

thermal protection

Thermal protection on the TPA3001D1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

APPLICATION INFORMATION

thermal considerations: output power and maximum ambient temperature

To calculate the maximum ambient temperature, the following equation may be used:

$$T_{Amax} = T_{Jmax} - \Theta_{JA} P_{Dissipated} \quad (3)$$

where: $T_{Jmax} = 150°C$

Θ_{JA} = 1 / derating factor = 1 / 0.03333 = 30°C/W

(The derating factor for the 24-pin PWP package is given in the dissipation rating table on page 3.)

To estimate the power dissipation, the following equation may be used:

$$P_{Dissipated} = P_{O(average)} \times ((1 / Efficiency) - 1) \quad (4)$$

Efficiency = ~85% for an 8-Ω load

= ~75% for a 4-Ω load

Example. What is the maximum ambient temperature for an application that requires the TPA3001D1 to drive 10 W into an 8-Ω speaker?

$P_{Dissipated}$ = 10 W x ((1 / 0.85) – 1) = 1.76 W

T_{Amax} = 150°C – (30°C/W x 1.76 W) = 97.2°C

This calculation shows that the TPA3001D1 can drive 10 W into an 8-Ω speaker up to the absolute maximum ambient temperature rating of 85°C, which must never be exceeded. Also, refer to Figures 2, 3, and 4 to determine the minimum load impedance for the desired output power.

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3001D1 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 23 kΩ, which is the absolute minimum input impedance of the TPA3001D1. At the lower gain settings, the input impedance could increase as high as 313 kΩ.

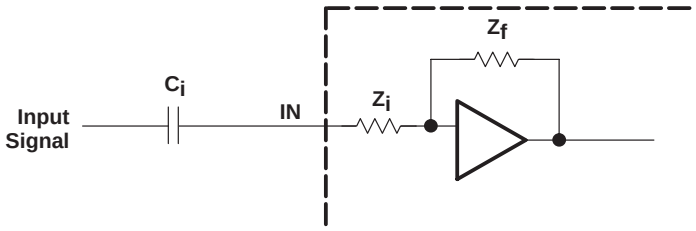
Table 1. Gain Settings

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	12	241
0	1	18	168
1	0	23.6	104
1	1	36	33

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the −3 dB or cutoff frequency also changes by over six times.



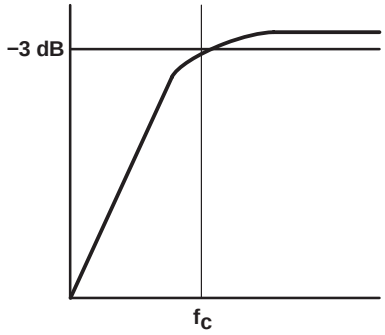
The −3-dB frequency can be calculated using equation 5. Use Table 1 for Z_i values.

$$f = \frac{1}{2\pi Z_i C_i} \tag{5}$$

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in equation 6.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{6}$$



The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 241 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 6 is reconfigured as equation 7.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{7}$$

In this example, C_i is 33 nF, so one would likely choose a value of 0.1 µF as this value is commonly used. If the gain is known and will be constant, use Z_i from Table 1 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling

The TPA3001D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

BSN and BSP capacitors

The full H-bridge output stage uses only NMOS transistors. It therefore requires bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-μF capacitor must be connected from OUTP to BSP, and one 0.22-μF capacitor must be connected from OUTN to BSN. (See Figure 30.)

BSN and BSP resistors

To limit the current when charging the bootstrap capacitors, a resistor with a value of approximately 50 Ω (+/−10% maximum) must be placed in series with each bootstrap capacitor. The current will be limited to less than 500 μA.

VCLAMP capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 1-μF capacitor must be connected from VCLAMP (pin 7) to ground and must be rated for at least 25 V. The voltage at VCLAMP (pin 7) varies with V_{CC} and may not be used for powering any other circuitry.

midrail bypass capacitor

The midrail bypass capacitor (C11 of Figure 30) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYPASS} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C11) values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD noise, and depop performance. The bypass capacitor **must** be a value greater than the input capacitors for optimum depop performance.

VREF decoupling capacitor

The VREF terminal (pin 23) is the output of an internally-generated 5-V supply, used for the oscillator and gain setting logic. It requires a 0.1-μF to 1-μF capacitor to ground to keep the regulator stable. The regulator may not be used to power any additional circuitry.

APPLICATION INFORMATION

differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3001D1 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3001D1 with a single-ended source, ac ground the INN input through a capacitor and apply the audio signal to the INP input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

switching frequency

The switching frequency is determined using the values of the components connected to R_{OSC} (pin 20) and C_{OSC} (pin 21) and may be calculated with the following equation:

$$f_s = \frac{6.6}{R_{OSC} C_{OSC}} \quad (8)$$

The frequency may be varied from 225 kHz to 275 kHz by adjusting the values chosen for R_{OSC} and C_{OSC}.

$\overline{\text{SHUTDOWN}}$ operation

The TPA3001D1 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)} = 1\ \mu A$. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable.

Ideally, the device should be held in shutdown when the system powers up and brought out of shutdown once any digital circuitry has settled. However, if $\overline{\text{SHUTDOWN}}$ is to be left unused, the terminal may be connected directly to V_{CC}.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

printed circuit board (PCB) layout

Because the TPA3001D1 is a class-D amplifier that switches at a high frequency, the layout of the printed circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

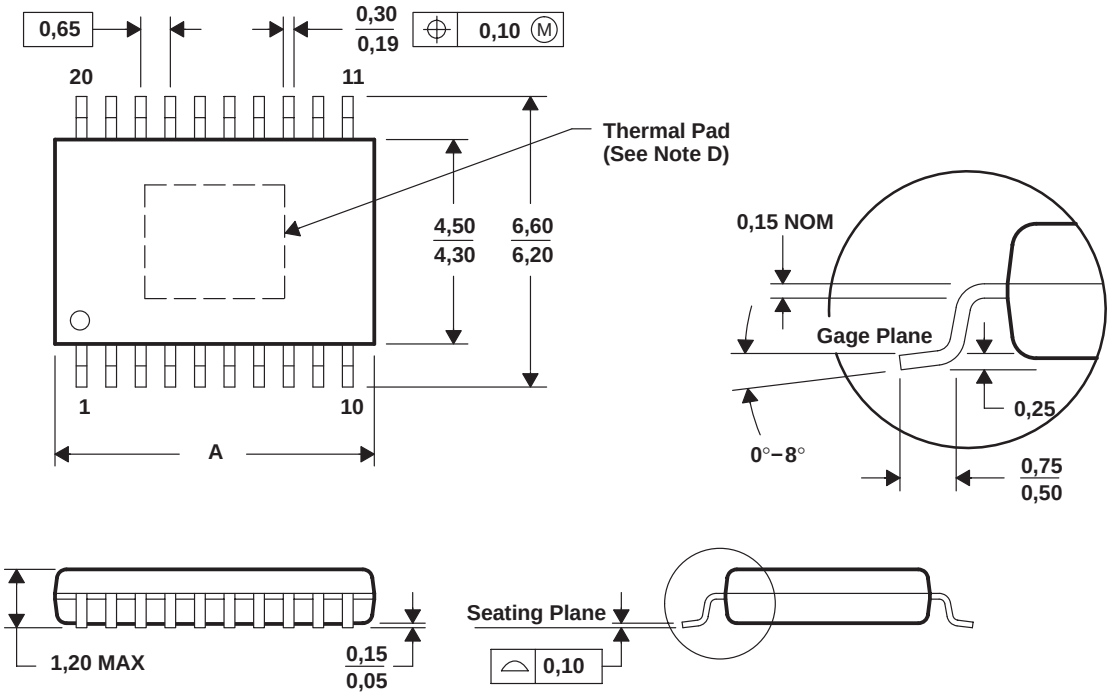
- Decoupling capacitors — As described on page 22, the high-frequency 0.1-uF decoupling capacitors should be placed as close to the PVCC (pin 9 and pin 16) and VCC (pin 24) terminals as possible. The BYPASS (pin 22) capacitor, VREF (pin 23) capacitor, and VCLAMP (pin 7) capacitor should also be placed as close to the device as possible. The large (10 uF or greater) bulk power supply decoupling capacitor should be placed near the TPA3001D1.
- Grounding — The VCC (pin 24) decoupling capacitor, VREF (pin 23) capacitor, BYPASS (pin 22) capacitor, COSC (pin 21) capacitor, and ROSC (pin 20) resistor should each be grounded to analog ground (AGND, pin 18 and pin 19). The PVCC (pin 9 and pin 16) decoupling capacitors should each be grounded to power ground (PGND, pin 12 and pin 13). Analog ground and power ground may be connected at the PowerPAD, which should be used as a central ground connection or star ground for the TPA3001D1.
- Output filter — The ferrite filter (Figure 34, page 18) should be placed as close to the output terminals (pins 10, 11, 14, and 15) as possible for the best EMI performance. The LC filter (Figure 35, page 18 and Figure 36, page 19) should be placed close to the ferrite filter. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- PowerPAD — The PowerPAD must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the PowerPAD thermal land should be 1.6 mm by 6.0 mm (63 mils by 236.2 mils). Two rows of solid vias (four vias per row, 0.3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. For additional information, please refer to the PowerPAD Thermally Enhanced Package application note, TI literature number SLMA002.

For an example layout, please refer to the TPA3001D1 Evaluation Module (TPA3001D1EVM) User Manual, TI literature number SLOU156. Both the EVM user manual and the PowerPAD application note are available on the TI web site at http://www.ti.com.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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