

# TPIC2810 8-BIT LED DRIVER WITH I<sup>2</sup>C INTERFACE

SLIS109A – DECEMBER 2001 – REVISED SEPTEMBER 2002

- Low  $r_{DS(on)}$  . . . 5  $\Omega$  Typical
- Eight Power DMOS Transistor Outputs of 100-mA Continuous Current
- 210-mA Current Limit Capability
- Drain Output ESD Protection . . . 3000 V
- Output Clamp Voltage . . . 40 V

## description

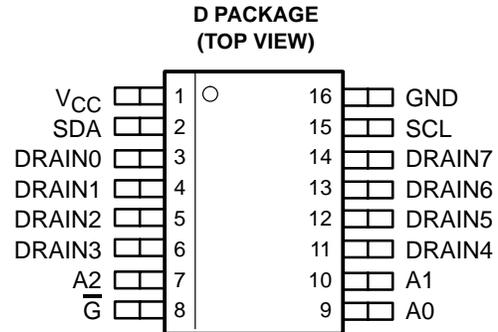
The TPIC2810 device is a monolithic, medium-voltage, low-current, 8-bit shift register design to drive low-side switched resistive loads such as LEDs. The device is not recommended for switching inductive loads.

This device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through the shift register via an I<sup>2</sup>C bus interface. Data is transferred into the data shift register only after the group ID and device address have been verified. The subaddress directs the I<sup>2</sup>C bus interface to read or write data to the device or transfer data to the output. When output enable ( $\overline{G}$ ) is held high, all drain outputs are off. When  $\overline{G}$  is held low, data from the output storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability.

The TPIC2810 device has an internal power-up clear to initialize all registers to an off state when power is applied to the device. It also has a thermal sensor to monitor the die temperature and shut the drain outputs off, if an over current condition occurs.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 100 mA continuous sink-current capability. Each output provides a 210-mA maximum current limit at  $T_C = 25^\circ\text{C}$ . The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 3000 V of ESD protection on output terminals and 2000 V of ESD protection on input terminals when tested using the human-body model.

The TPIC2810 device is characterized for operation over the operating case temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

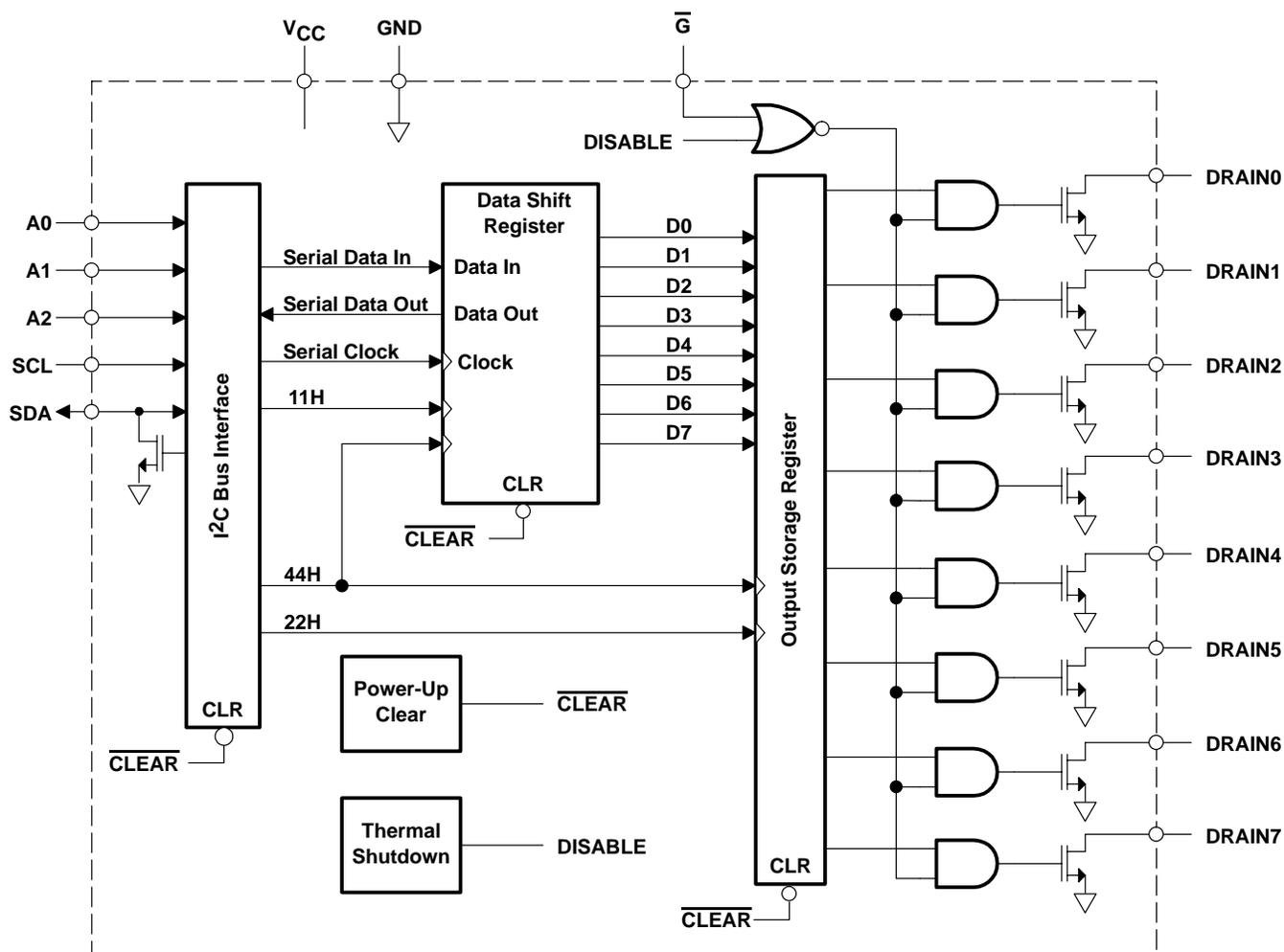
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## functional block diagram

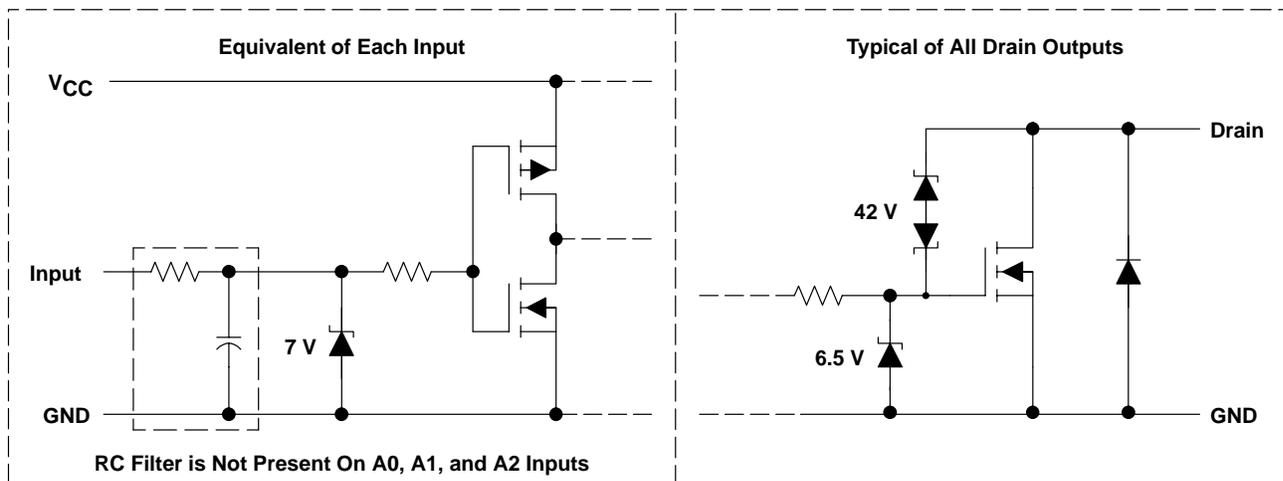


See the *TPIC2810 subaddress and I<sup>2</sup>C protocol definition* section of this data sheet for definition of the 11H, 22H, and 44H control signals.

### Terminal Functions

| TERMINAL NAME   | NO. | I/O | DESCRIPTION  |
|-----------------|-----|-----|--|
| A0              | 9   | I   | Address input 0  |
| A1              | 10  | I   | Address input 1  |
| A2              | 7   | I   | Address input 2  |
| DRAIN0          | 3   | O   | FET drain outputs. The DRAIN terminals are low-side switches for resistive loads.                |
| DRAIN1          | 4   |     |  |
| DRAIN2          | 5   |     |  |
| DRAIN3          | 6   |     |  |
| DRAIN4          | 11  |     |  |
| DRAIN5          | 12  |     |  |
| DRAIN6          | 13  |     |  |
| DRAIN7          | 14  |     |  |
| $\bar{G}$       | 8   | I   | Output enable. Active low input enables output FETs when low and disables output FETs when high. |
| GND             | 16  | O   | Ground   |
| SCL             | 15  | I   | Serial clock   |
| SDA             | 2   | I/O | Open drain, bidirectional serial data terminal   |
| V <sub>CC</sub> | 1   | I   | Supply voltage input   |

### schematic of inputs and outputs



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### absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

|  |                              |
|--|------------------------------|
| Logic supply voltage range, $V_{CC}$ (see Note 1)  | 7 V                          |
| Logic input voltage range, $V_I$   | -0.3 V to 7 V                |
| Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)  | 40 V                         |
| Continuous source-to-drain diode anode current   | 210 mA                       |
| Pulsed source-to-drain diode anode current (see Note 3)  | 420 mA                       |
| Pulsed drain current, each output, all outputs on, $I_D$ , $T_C = 25^\circ\text{C}$ (see Note 3) | 210 mA                       |
| Peak drain current, single output, $I_{DM}$ , $T_C = 25^\circ\text{C}$ (see Note 3)              | 210 mA                       |
| Continuous total dissipation   | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$  | -40°C to 150°C               |
| Operating case temperature range, $T_C$  | -40°C to 125°C               |
| Storage temperature range, $T_{stg}$   | -65°C to 150°C               |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
  2. Each power DMOS source is internally connected to GND.
  3. Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .

DISSIPATION RATING TABLE

| PACKAGE | $T_C = 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$<br>POWER RATING |
|---------|--|---|---|
| D       | 1087 mW                                  | 8.7 mW/°C   | 217 mW                                    |

### recommended operating conditions

|   | MIN          | MAX | UNIT |
|---|--------------|-----|------|
| Logic supply voltage, $V_{CC}$  | 3.0          | 5.5 | V    |
| High-level input voltage, $V_{IH}$  | 0.7 $V_{CC}$ |     | V    |
| Low-level input voltage, $V_{IL}$   | 0.3 $V_{CC}$ |     | V    |
| Pulse drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5 \text{ V}$ , all outputs on (see Notes 3 and 4 and Figure 8) | 210          |     | mA   |
| Operating case temperature, $T_C$   | -40          | 125 | °C   |

- NOTES:
3. Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .
  4. Technique must limit  $T_J - T_C$  to 10°C maximum.



# TPIC2810

## 8-BIT LED DRIVER WITH I<sup>2</sup>C INTERFACE

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### electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER            |   | TEST CONDITIONS  |  | MIN | TYP  | MAX  | UNIT             |
|----------------------|---|--|--|-----|------|------|------------------|
| $V_{CC}$             | Logic supply voltage                    |  |  | 3   |      | 5.5  | V                |
| $V_{(BR)DSX}$        | Drain-to-source breakdown voltage       | $I_D = 1\text{ mA}$  |  | 40  |      |      | V                |
| $V_{SD}$             | Source-to-drain diode forward voltage   | $I_F = 100\text{ mA}$  |  |     | 0.85 | 1.2  | V                |
| $V_{PUC}$            | Power-up clear voltage                  | $V_{CC}$ rising no load,   | See Note 5                               |     |      | 2.84 | V                |
| $I_{IH}$             | High-level input current                | $V_{CC} = 5.5\text{ V}$ ,  | $V_I = V_{CC}$                           |     |      | 1    | $\mu\text{A}$    |
| $I_{IL}$             | Low-level input current                 | $V_{CC} = 5.5\text{ V}$ ,  | $V_I = 0$                                |     |      | -1   | $\mu\text{A}$    |
| $V_{HYS}$            | Digital input hysteresis                |  |  |     | 1.1  |      | V                |
| $I_{CC}$             | Logic supply current                    | $V_{CC} = 5.5\text{ V}$  | All outputs off                          |     | 0.62 | 1    | mA               |
|                      |   |  | All outputs on                           |     | 0.7  | 1    |                  |
| $I_{CC}(\text{FRQ})$ | Logic supply current at frequency       | $f_{SCL} = 100\text{ kHz}$ ,<br>All outputs off,                               | $C_L = 30\text{ pF}$ ,<br>See Figure 3   |     | 0.74 | 1    | mA               |
| $I_{OL}$             | Low level output current; SDA           | $V_{OL} = 0.4\text{ V}$  |  |     | 13   |      | mA               |
| $I_L$                | Leakage current; SDA                    | $V_I = V_{CC}$   |  | -1  |      | 1    | $\mu\text{A}$    |
| $I_N$                | Nominal current                         | $V_{DS(\text{on})} = 0.5\text{ V}$ ,<br>$T_C = 85^\circ\text{C}$ ,             | $I_N = I_D$ ,<br>See Notes 4, 6, 7       |     | 75   |      | mA               |
| $I_{DSX}$            | Off-state drain current                 | $V_{DS} = 30\text{ V}$   | $V_{CC} = 5.5\text{ V}$                  |     | 0.3  | 0.6  | $\mu\text{A}$    |
|                      |   | $V_{DS} = 30\text{ V}$ , $T_C = 125^\circ\text{C}$                             |  |     | 0.3  | 0.6  |                  |
| $T_{TSD}$            | Thermal shutdown set points             |  |  | 160 |      |      | $^\circ\text{C}$ |
| $T_{HYS}$            | Thermal shutdown hysteresis             |  |  | 10  | 20   | 30   | $^\circ\text{C}$ |
| $r_{DS(\text{on})}$  | Static drain-source on-state resistance | $I_D = 100\text{ mA}$ , $V_{CC} = 3\text{ V}$                                  | See Notes 4 and 6<br>and Figures 4 and 5 |     | 8.0  | 10.8 | $\Omega$         |
|                      |   | $I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$                                |  |     | 5.1  | 6.9  |                  |
|                      |   | $I_D = 100\text{ mA}$ , $V_{CC} = 3.0\text{ V}$ ,<br>$T_C = 125^\circ\text{C}$ |  |     | 13.0 | 18.2 |                  |
|                      |   | $I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ ,<br>$T_C = 125^\circ\text{C}$ |  |     | 8.0  | 11.2 |                  |

- NOTES:
- Technique must limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum
  - The power-up clear resets the I<sup>2</sup>C interface and clears all outputs.
  - These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
  - Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage of 0.5 V at  $T_C = 85^\circ\text{C}$ .

# TPIC2810

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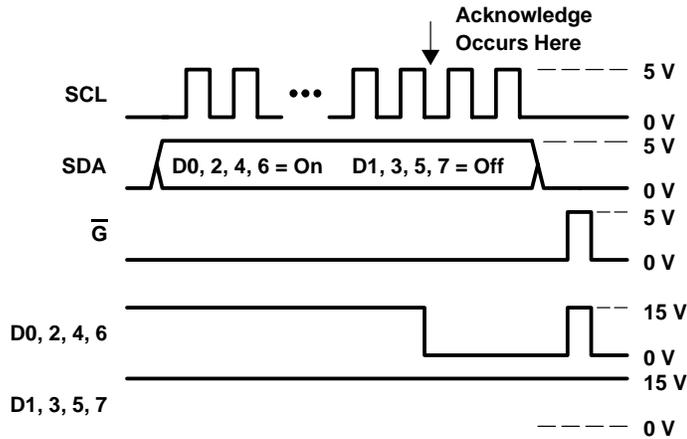
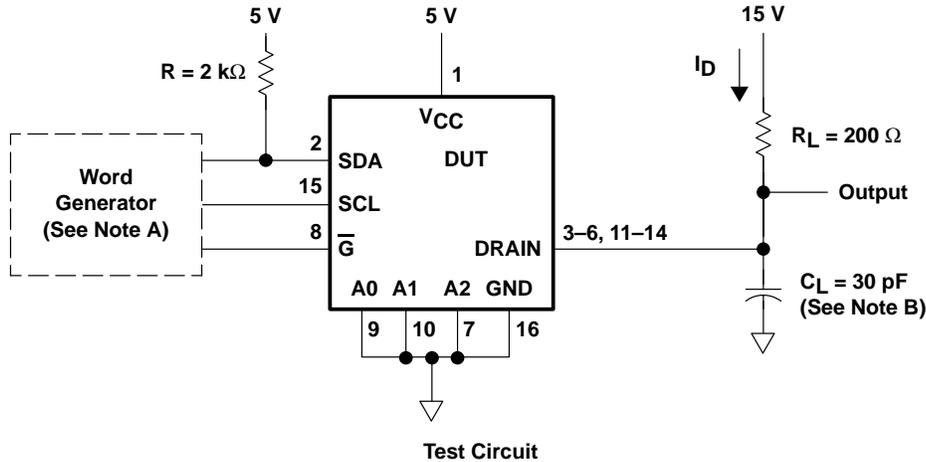
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$ ,  $C_L = 100\text{ pF}$  (unless otherwise noted)

| PARAMETER            |  | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT          |
|----------------------|--|---|-----|------|-----|---------------|
| $t_{PLH}$            | Propagation delay time, low-to-high-level output from $\overline{G}$ | $C_L = 30\text{ pF}$ ,<br>$I_D = 75\text{ mA}$ ,<br>See Figures 1, 2, and 6 |     | 1.15 |     | $\mu\text{s}$ |
| $t_{PHL}$            | Propagation delay time, high-to-low-level output from $\overline{G}$ |   |     | 0.64 |     |               |
| $t_r(\text{OUT})$    | Rise time, drain output  |   |     | 1.05 |     |               |
| $t_f(\text{OUT})$    | Fall time, drain output  |   |     | 0.89 |     | $\mu\text{s}$ |
| $f(\text{SCL})$      | Serial clock frequency   |   |     | 100  |     | $\text{kHz}$  |
|                      |  |   |     | 400  |     |               |
|                      |  |   |     |      | 2   |               |
| $t(\text{BUF})$      | Bus free time between stop and start condition                       | SCL = 100 kHz   | 4.7 |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 1.3 |      |     |               |
| $t(\text{SP})$       | Tolerable spike width on bus   |   |     | 50   |     | ns            |
| $t_{pd}(\text{ACK})$ | SCL low to data out valid (acknowledge)                              |   |     | 120  |     | ns            |
| $t_{LOW}$            | SCL low time   | SCL = 100 kHz   | 4.7 |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 1.3 |      |     |               |
|                      |  | SCL = 2 MHz   | 250 |      |     | ns            |
| $t_{HIGH}$           | SCL high time  | SCL = 100 kHz   | 4.0 |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 600 |      |     |               |
|                      |  | SCL = 2 MHz   | 200 |      |     | ns            |
| $t_{su}(\text{DAT})$ | SDA $\rightarrow$ SCL setup time                                     | SCL = 100 kHz   | 250 |      |     | ns            |
|                      |  | SCL = 400 kHz   | 100 |      |     |               |
|                      |  | SCL = 2 MHz   | 10  |      |     |               |
| $t_{su}(\text{STA})$ | Start condition setup time   | SCL = 100 kHz   | 4.7 |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 600 |      |     |               |
|                      |  | SCL = 2 MHz   | 300 |      |     | ns            |
| $t_{su}(\text{STO})$ | Stop condition setup time  | SCL = 100 kHz   | 4   |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 600 |      |     |               |
|                      |  | SCL = 2 MHz   | 140 |      |     | ns            |
| $t_h(\text{DAT})$    | SDA $\rightarrow$ SCL hold time                                      |   | 50  |      |     | ns            |
| $t_h(\text{STA})$    | Start condition hold time  | SCL = 100 kHz   | 4   |      |     | $\mu\text{s}$ |
|                      |  | SCL = 400 kHz   | 600 |      |     |               |
|                      |  | SCL = 2 MHz   | 160 |      |     | ns            |
| $t_r(\text{SCL})$    | Rise time of SCL signal  | SCL = 100 kHz   |     | 1000 |     | ns            |
|                      |  | SCL = 400 kHz   |     | 300  |     |               |
|                      |  | SCL = 2 MHz   |     | 70   |     |               |
| $t_f(\text{SCL})$    | Fall time of SCL signal  | SCL = 100 kHz   |     | 300  |     | ns            |
|                      |  | SCL = 400 kHz   |     | 300  |     |               |
|                      |  | SCL = 2 MHz   |     | 70   |     |               |
| $t_r(\text{SDA})$    | Rise time of SDA signal  | SCL = 100 kHz   |     | 1000 |     | ns            |
|                      |  | SCL = 400 kHz   |     | 300  |     |               |
|                      |  | SCL = 2 MHz   |     | 70   |     |               |
| $t_f(\text{SDA})$    | Fall time of SDA signal  | SCL = 100 kHz   |     | 300  |     | ns            |
|                      |  | SCL = 400 kHz   |     | 300  |     |               |
|                      |  | SCL = 2 MHz   |     | 140  |     |               |

thermal resistance

| PARAMETER   | TEST CONDITIONS                | MIN | MAX | UNIT |
|---|--------------------------------|-----|-----|------|
| R <sub>θJA</sub> Junction-to-ambient thermal resistance | All 8 outputs with equal power |     | 115 | °C/W |

PARAMETER MEASUREMENT INFORMATION



Voltage Waveforms

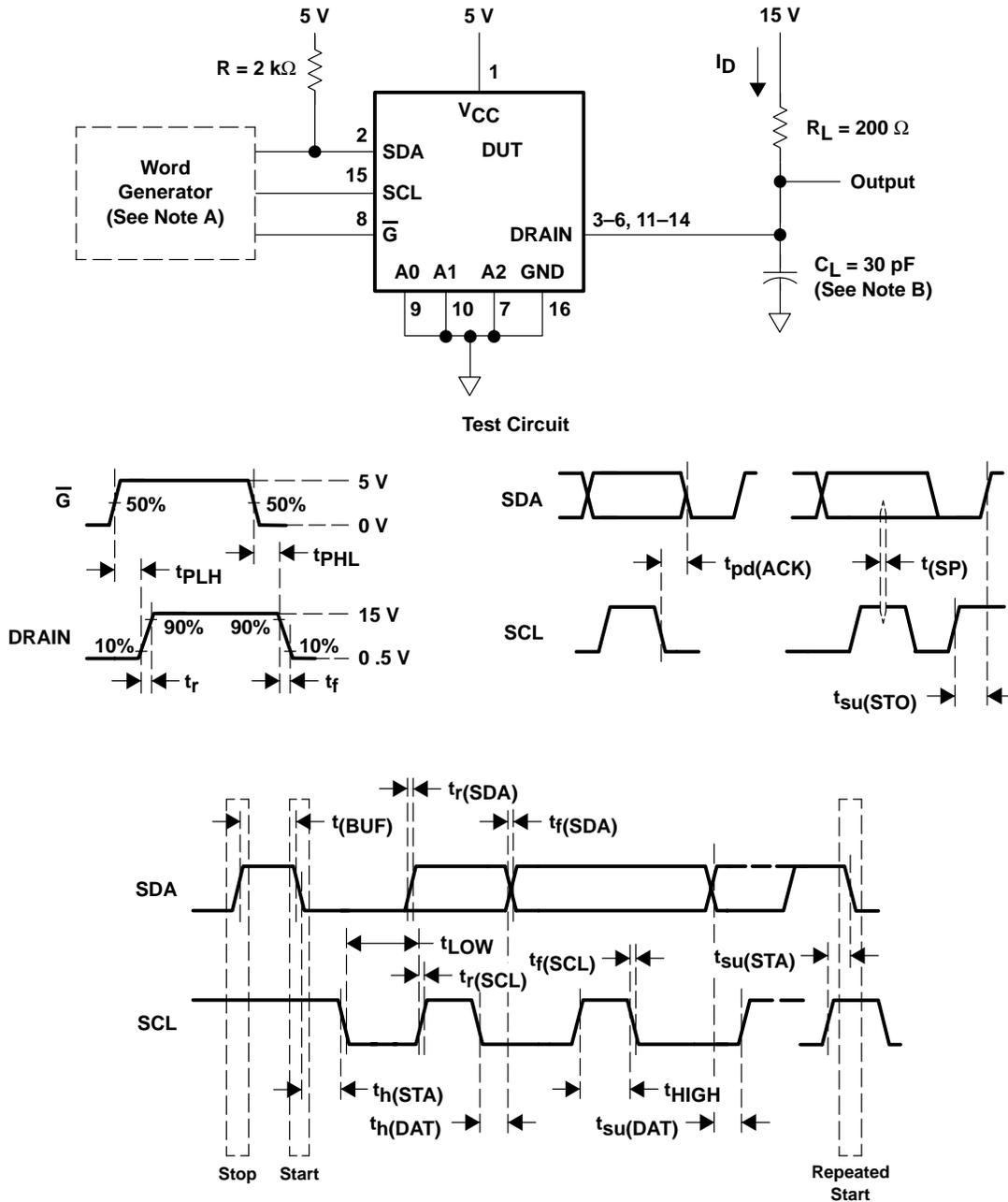
NOTES: A. The word generator has the following characteristics:  $t_r \leq 30$  ns,  $t_f \leq 30$  ns, pulsed repetition rate (PRR) = 400 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

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## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: t<sub>r</sub> ≤ 30 ns, t<sub>f</sub> ≤ 30 ns, pulsed repetition rate (PRR) = 400 kHz, Z<sub>O</sub> = 50 Ω.  
B. C<sub>L</sub> includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times and Voltage Waveforms

TYPICAL CHARACTERISTICS

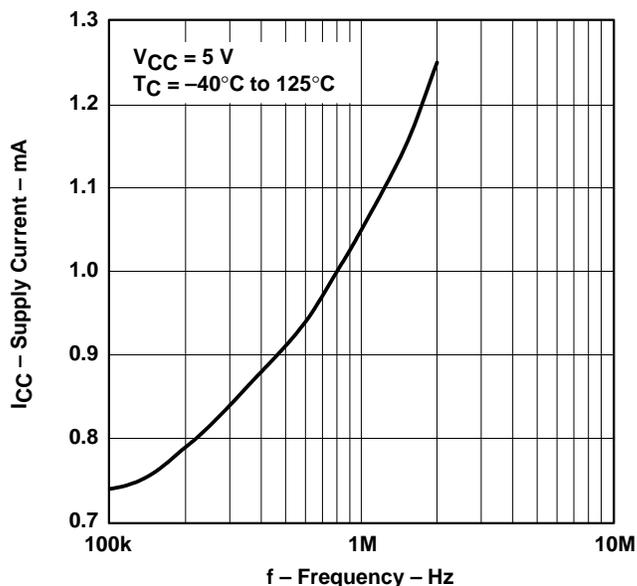


Figure 3. Supply Current vs Frequency

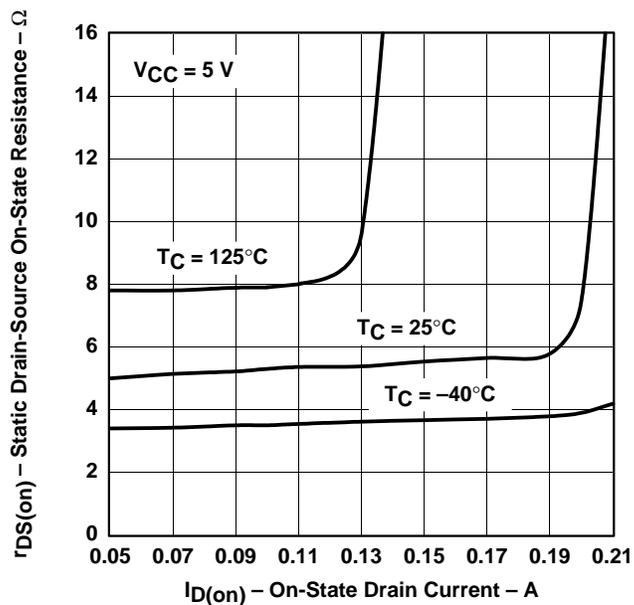


Figure 4. Static Drain-Source On-State Resistance vs On-State Drain Current

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## TYPICAL CHARACTERISTICS

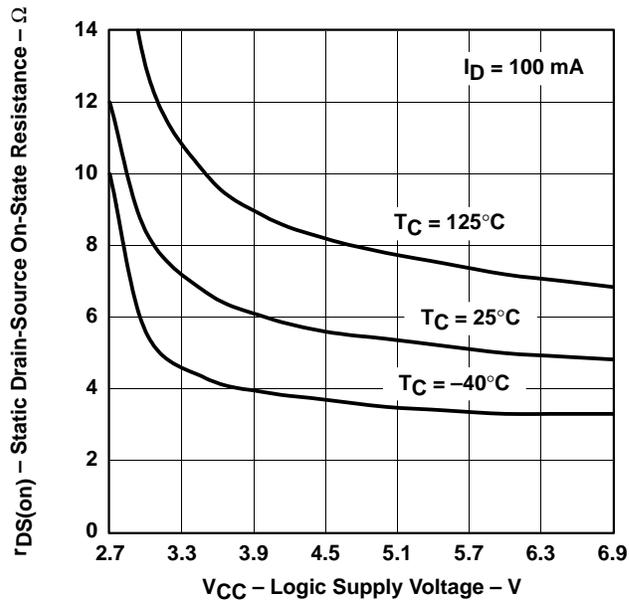


Figure 5. Static Drain-Source On-State Resistance vs Logic Supply Voltage

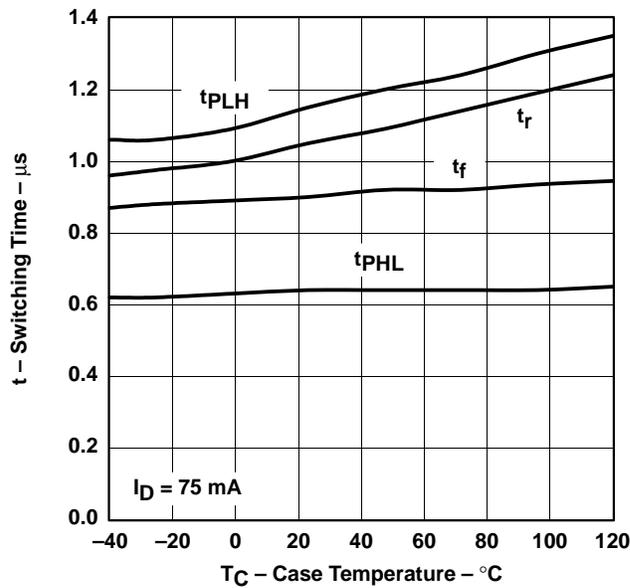


Figure 6. Switching Time vs Case Temperature

TYPICAL CHARACTERISTICS

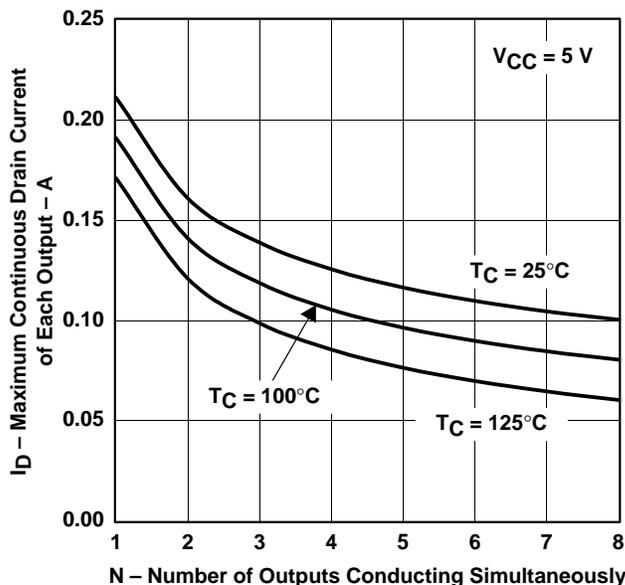


Figure 7. Maximum Continuous Drain Current Of Each Output vs Number Of Outputs Conducting Simultaneously

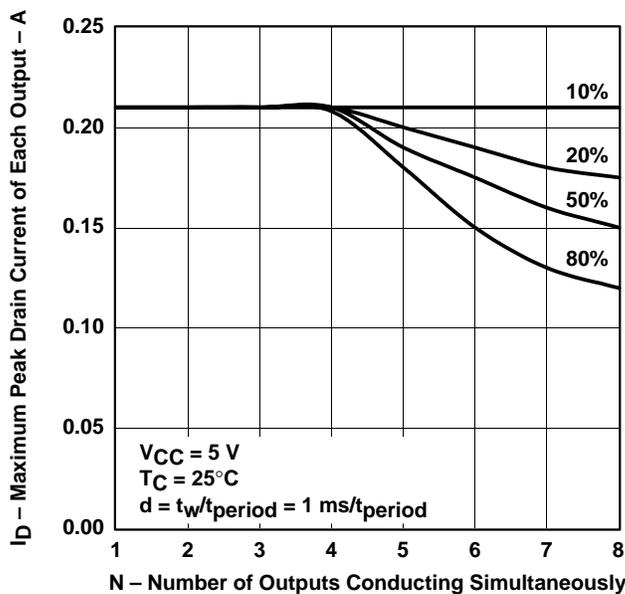


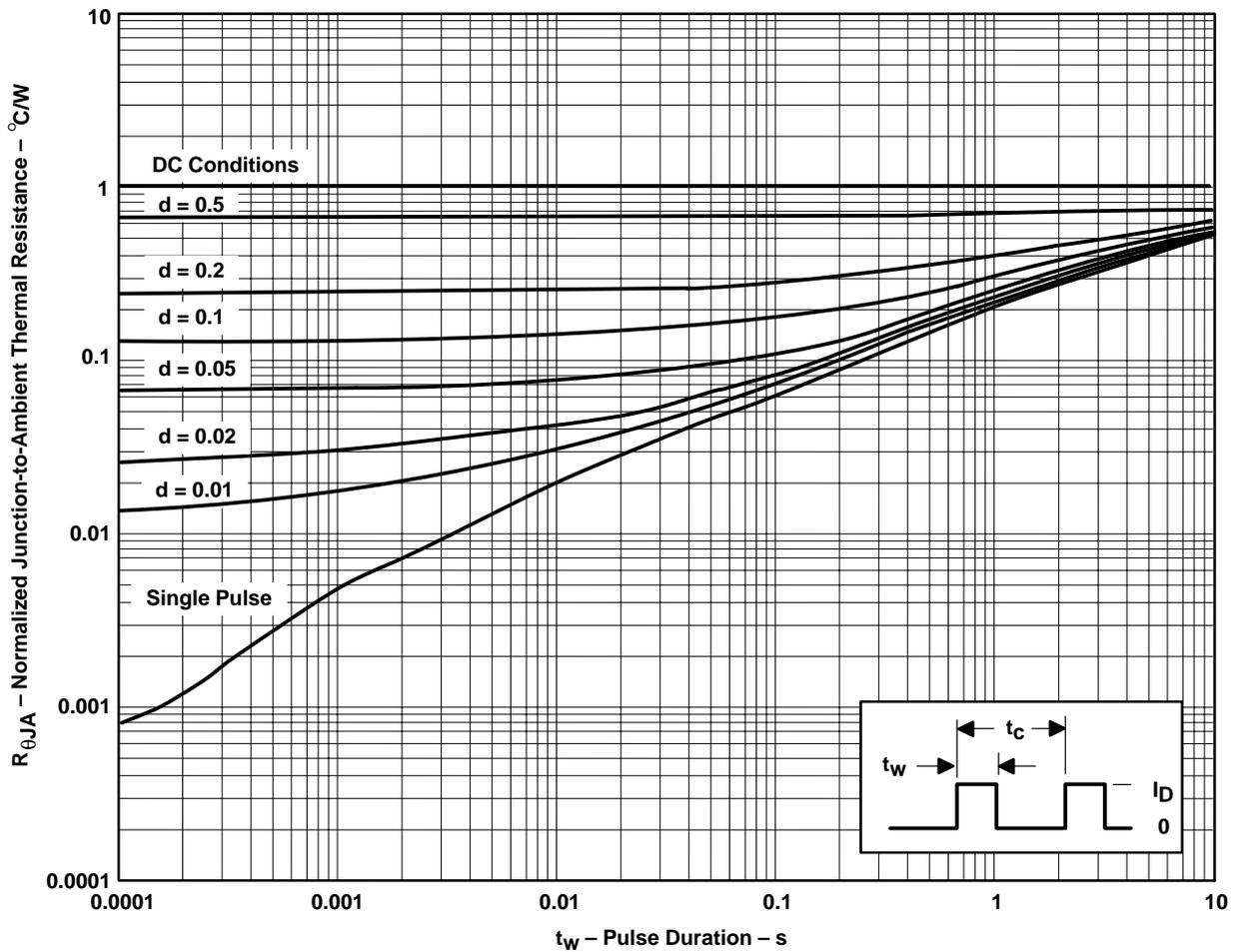
Figure 8. Maximum Peak Drain Current Of Each Output vs Number Of Outputs Conducting Simultaneously

# TPIC2810 8-BIT LED DRIVER WITH I<sup>2</sup>C INTERFACE

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## THERMAL INFORMATION

### D PACKAGE†



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

**Figure 9. Normalized Junction-to-Ambient Thermal Resistance vs Pulse Duration**

## PRINCIPLES OF OPERATION

### TPIC2810 subaddress and I<sup>2</sup>C protocol definition

#### subaddress definition:

##### Summary:

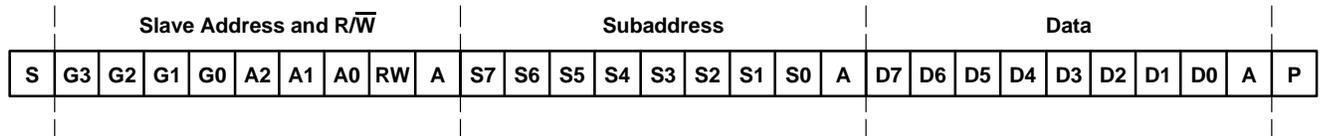
| HEX Value | R/ $\bar{W}$ Bit | Function   |
|-----------|------------------|--|
| 11H       | 1                | Read data from the input register  |
| 11H       | 0                | Write data to the data shift register, do not transfer to output register  |
| 22H       | 0                | Command to transfer data from the data shift register to the output storage register   |
| 44H       | 0                | Write data to the data shift register and transfer it to the output storage register immediately (extra load 22H command not needed) |
| Other     | x                | No action on undefined subaddresses  |

All other undefined subaddress values are not acknowledged.

#### register definition:

- The data shift register receives serial data from the I<sup>2</sup>C interface.
- The data shift register receives data from the input interface and holds it until it is transferred to the output storage register.
- The output storage register controls whether the FET is on or off.

### TPIC2810 I<sup>2</sup>C input interface protocol definition



|                   |  |
|-------------------|--|
| <b>S</b>          | <b>Start Condition</b>                                       |
| <b>G</b>          | <b>Group ID: Defined as 1100</b>                             |
| <b>A(0:2)</b>     | <b>Device Address Selectable Via Input Terminals</b>         |
| <b>RW</b>         | <b>Read/Write Select Bit</b>                                 |
| <b>A</b>          | <b>Acknowledge</b>   |
| <b>Subaddress</b> | <b>Defined Per Subaddress Table</b>                          |
| <b>Data</b>       | <b>Data to Be Loaded Into the Shift and Output Registers</b> |
| <b>P</b>          | <b>Stop Condition</b>  |

# TPIC2810

## 8-BIT LED DRIVER WITH I<sup>2</sup>C INTERFACE

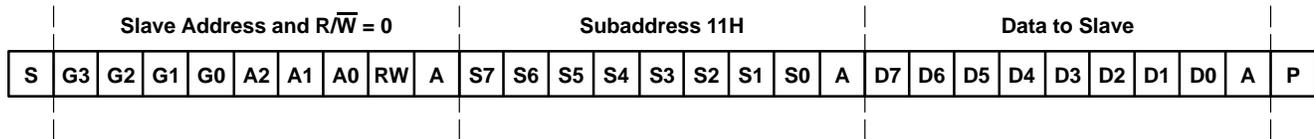
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### PRINCIPLES OF OPERATION

#### Case 1: Read/Write serial data, but do not load output register

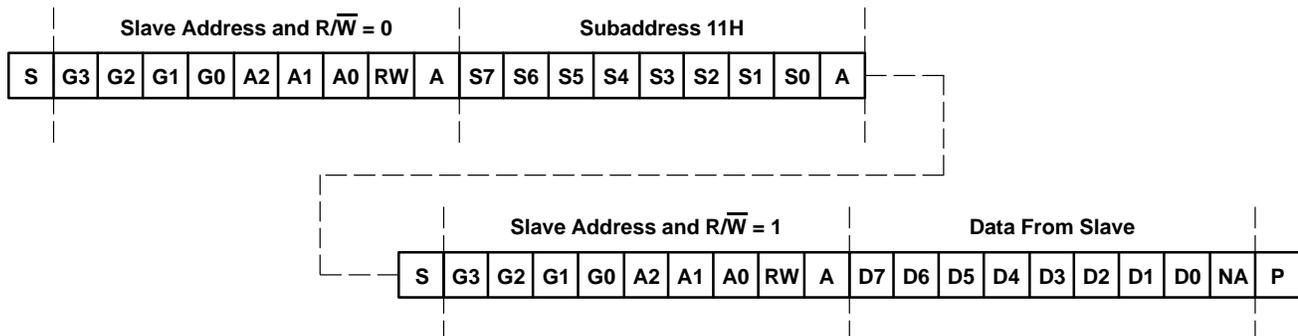
This case loads the data shift register with data via the I<sup>2</sup>C interface. Data is not transferred to the output storage register.

#### write operation:



- G[3:0]: Fixed at 1100
- A[2:0]: Selectable Via Input Terminals
- RW: 0 = Write Shift Register
- Subaddress: 11H (0001 0001)
- Data: Output Data to the TPIC2810 Device
- Acknowledge: Occurs After Valid Address Byte, After the Subaddress Byte, and After the Data Byte

#### read operation:



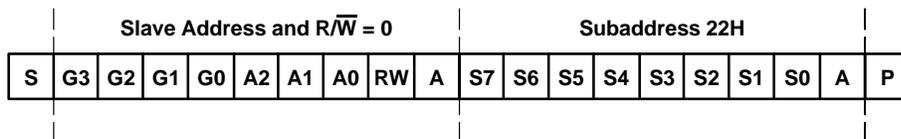
- G[3:0]: Fixed at 1100
- A[2:0]: Selectable Via Input Terminals
- RW: 1 = Read Shift Register (Note the Slave Address RW Bit = 0)
- Subaddress: 11H (0001 0001)
- Data: Input Data From the TPIC2810 Device
- Acknowledge: Occurs After Valid Address Byte and After the Subaddress Byte



## PRINCIPLES OF OPERATION

### Case 2: Transfer serial data to output storage register

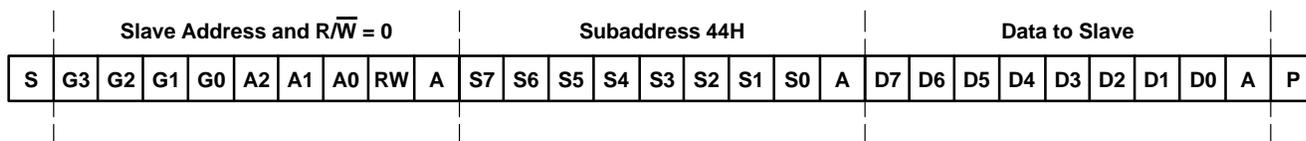
This case transfers data from the data shift register to the output storage register. The transfer must occur during the subaddress acknowledge bit and the data byte is ignored.



**G[3:0]:** Fixed at 1100  
**A[2:0]:** Selectable Via Input Terminals  
**RW:** 0 = Write Shift Register  
**Subaddress:** 22H (0010 0010)  
**Data:** Output Data to the TPIC2810 Device  
**Acknowledge:** Occurs After Valid Address Byte and After the Subaddress Byte

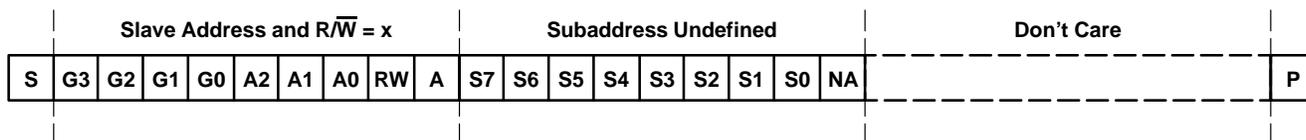
### Case 3: Read serial data and load output storage register

This case loads the data shift register with data via the I<sup>2</sup>C interface and transfers the data to output storage register, if  $R/\overline{W} = 0$ . The transfer occurs during the acknowledge bit following the data byte. Data byte and transfer to the output register is ignored if  $R/\overline{W} = 1$ .



**G[3:0]:** Fixed at 1100  
**A[2:0]:** Selectable Via Input Terminals  
**RW:** 0 = Write Shift Register  
**Subaddress:** 44H (0100 0100)  
**Data:** Output Data to the TPIC2810 Device  
**Acknowledge:** Occurs After Valid Address Byte, After the Subaddress Byte and After the Data Byte

### Case 4: Undefined subaddress values



**G[3:0]:** Fixed at 1100  
**A[2:0]:** Selectable Via Input Terminals  
**RW:** Don't Care  
**Subaddress:** All Bit Combinations Except 11H, 22H, and 44H  
**Data:** Don't Care; Data Is Ignored  
**Acknowledge:** Occurs After Valid Address Byte, But Is Not Issued After an Undefined Subaddress Byte or After the Data Byte Following an Undefined Subaddress Byte

# TPIC2810

## 8-BIT LED DRIVER WITH I<sup>2</sup>C INTERFACE

SLIS109A – DECEMBER 2001 – REVISED SEPTEMBER 2002

### PRINCIPLES OF OPERATION

#### I<sup>2</sup>C bus operation

The I<sup>2</sup>C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data signal is bidirectional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data signal to provide the high level portion of the data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 10. Both the SCL and SDA signals must remain in a logic high state when the controller is not communicating with the slave devices. A start condition is recognized by the slave devices when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the TPIC2810 device receives serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device issues an acknowledge pulse and prepares the receive subaddress data. The group ID for the TPIC2810 device is hard coded to be 1100. The slave address bits are set to correspond to the A(0:2) inputs for the device. Up to eight TPIC2810 devices can be placed on the bus. Subaddress data is decoded and responded to as per the *TPIC2810 subaddress and I<sup>2</sup>C protocol definition* section of this data sheet. Data transmission is complete by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low-to-high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal.

An acknowledge is issued by the TPIC2810 device after the reception of valid address, subaddress and data words as per the *TPIC2810B subaddress and I<sup>2</sup>C protocol definition* section of this document. Reference Figure 10. The device acknowledges each byte of data that it receives from the controller.

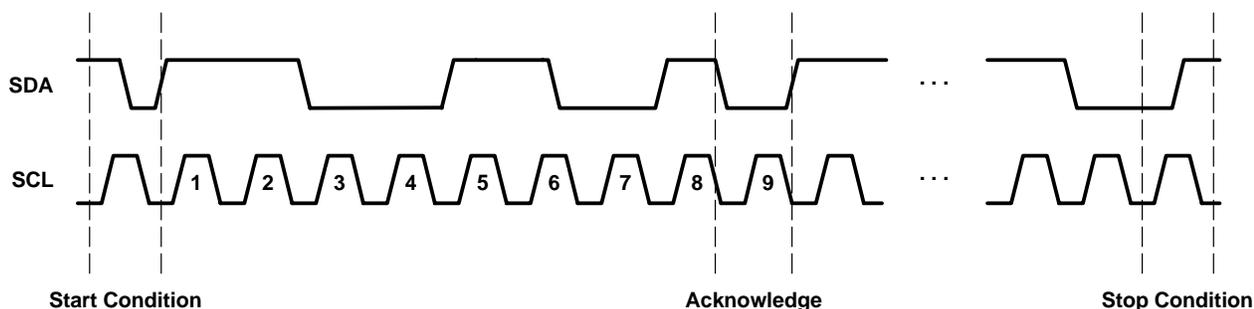


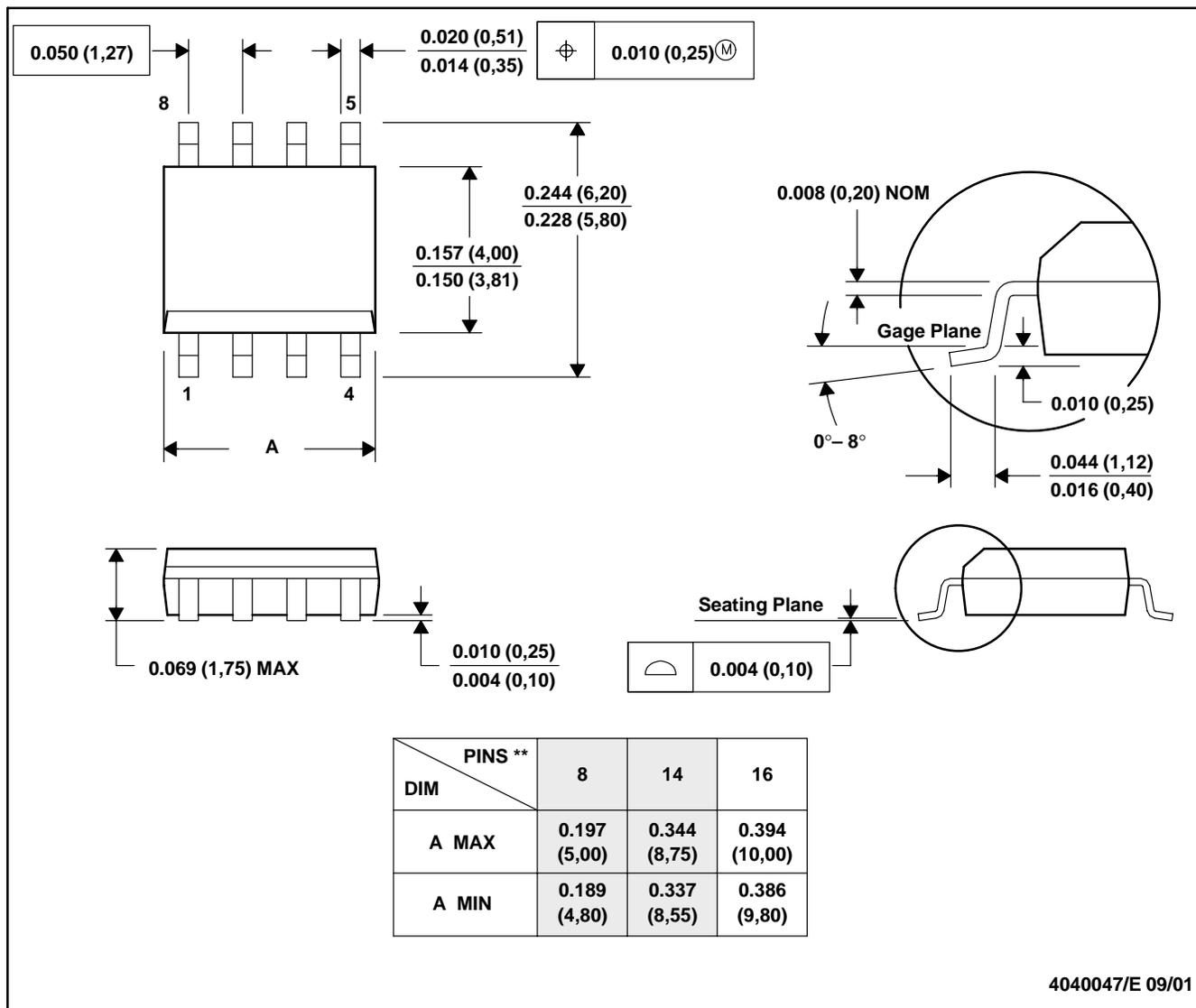
Figure 10. Start/Stop/Acknowledge Protocol

MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPIC2810D        | ACTIVE                | SOIC         | D               | 16   | 40          | TBD                     | CU NIPDAU        | Level-1-220C-UNLIM           |
| TPIC2810DG4      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPIC2810DR       | ACTIVE                | SOIC         | D               | 16   | 2500        | TBD                     | CU NIPDAU        | Level-1-220C-UNLIM           |
| TPIC2810DRG4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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