TS482

100mW STEREO HEADPHONE AMPLIFIER

- Operating from **Vcc=2V to 5.5V**
- 100mW into 16Ω at 5V
- 38mW into 16Ω at 3.3V
- 11.5mW into 16Ω at 2V
- Switch ON/OFF click reduction circuitry
- High Power Supply Rejection Ratio: 85dB at 5V
- High Signal-to-Noise ratio: 110dB(A) at 5V
- High Crosstalk immunity: 100dB (F=1kHz)
- Rail to Rail input and output
- Unity-Gain Stable
- Available in **SO8, MiniSO8 & DFN8**

DESCRIPTION

The TS482 is a dual audio power amplifier able to drive a 16 or 32Ω stereo headset down to low voltages.

It's delivering up to 100mW per channel (into 16Ω loads) of continuous average power with 0.1% THD+N from a 5V power supply.

The unity gain stable TS482 can be configured by external gain-setting resistors.

APPLICATIONS

- Stereo Headphone Amplifier
- Optical Storage
- Computer Motherboard
- PDA, organizers & Notebook computers
- High end TV, Set Top Box, DVD Players
- Sound Cards

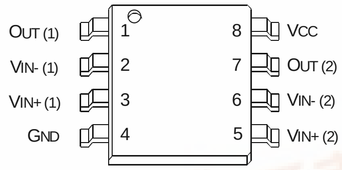
ORDER CODE

Part Number	Temperature Range	Package			Marking
		D	S	Q	
TS482ID/DT	-40, +85°C	•			482I
TS482IST			•		
TS482IQT				•	

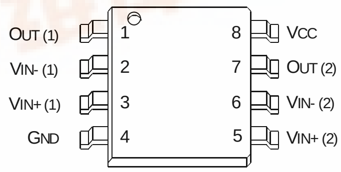
MiniSO & DFN only available in Tape & Reel with T suffix,
SO is available in Tube (D) and in Tape & Reel (DT))

PIN CONNECTIONS (top view)

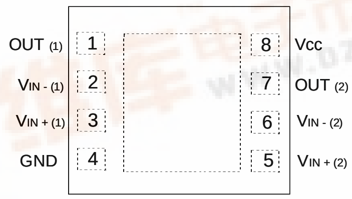
TS482ID, TS482IDT - SO8



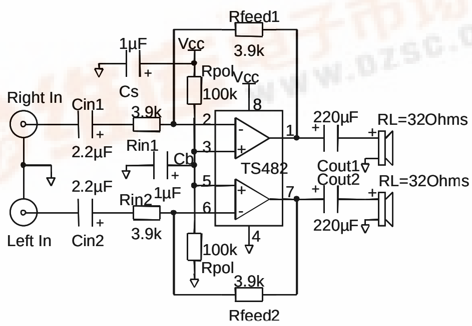
TS482IST - MiniSO8



TS482IQT - DFN8



TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage	-0.3 to V_{CC} +0.3	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8	 175 215 70	°C/W
Pd	Power Dissipation [2] SO8 MiniSO8 DFN8	 0.71 0.58 1.79	W
ESD	Human Body Model (pin to pin)	2	kV
ESD	Machine Model - 220pF - 240pF (pin to pin)	200	V
Latch-up	Latch-up Immunity (All pins)	200	mA
	Lead Temperature (soldering, 10sec)	250	°C
	Output Short-Circuit Duration	see note [3]	

1. All voltages values are measured with respect to the ground pin.
2. Pd has been calculated with Tamb = 25°C, Tjunction = 150°C.
3. Attention must be paid to continuous power dissipation. Exposure of the IC to a short circuit on one or two amplifiers simultaneously can cause excessive heating and the destruction of the device.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
R_L	Load Resistor	>= 16	Ω
C_L	Load Capacitor R_L = 16 to 100Ω R_L > 100Ω	 400 100	pF
V_{ICM}	Common Mode Input Voltage Range	G_{ND} to V_{CC}	V
R_{THJA}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8[1]	 150 190 41	°C/W

1. When mounted on a 4-layer PCB.

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin (fc = 1 / (2 x Pi x Rin x Cin))
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass capacitor which provides half supply filtering
Cout	Output coupling capacitor which blocks the DC voltage at the load input terminal This capacitor also forms a high pass filter with RL (fc = 1 / (2 x Pi x RL x Cout))
Rpol	These 2 resistors form a voltage divider which provide a DC biasing voltage (Vcc/2) for the 2 amplifiers.
Av	Closed loop gain = -Rfeed / Rin

ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$	 60 95	65 67.5 100 107		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) [1)] $R_L = 32\Omega$, P_{out} = 60mW, 20Hz ≤ F ≤ 20kHz $R_L = 16\Omega$, P_{out} = 90mW, 20Hz ≤ F ≤ 20kHz		0.03 0.03		%
PSRR	Power Supply Rejection Ratio (A_V=1), inputs floating F = 100Hz, Vripple = 100mVpp		85		dB
I_O	Max Output Current THD +N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$	106	120		mA
V_O	Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$	 4.45 4.2	0.4 4.6 0.55 4.4	0.48 0.65	V
SNR	Signal-to-Noise Ratio (Filter Type A, A_V=-1) ($R_L = 32\Omega$, THD +N < 0.2%, 20Hz ≤ F ≤ 20kHz)	95	110		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz		100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.35	2.2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.45	0.7		V/µs

1. Fig. 68 to 79 show dispersion of these parameters.

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) [2)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.3	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	 23 36	27 28 38 42		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) [1)] R_L = 32Ω, P_{out} = 16mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 35mW, 20Hz ≤ F ≤ 20kHz		0.03 0.03		%
PSRR	Power Supply Rejection Ratio (A_V=1), inputs floating F = 100Hz, Vripple = 100mVpp		80		dB
I_O	Max Output Current THD +N < 1%, R_L = 16Ω connected between out and $V_{CC}/2$	64	75		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	 2.85 2.68	0.3 3 0.45 2.85	0.38 0.52 	V
SNR	Signal-to-Noise Ratio (Filter Type A, A_V=-1) (R_L = 32Ω, THD +N < 0.2%, 20Hz ≤ F ≤ 20kHz)	92	107		dB
Crosstalk	Channel Separation, R_L = 32Ω F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω F = 1kHz F = 20Hz to 20kHz		 100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwith Product (R_L = 32Ω)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)	0.45	0.7		V/μs

1. Fig. 68 to 79 show dispersion of these parameters.

2. All electrical values are guaranteed with correlation measurements at 2V and 5V

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2.5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) [2)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.1	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$	 12.5 17.5	 13.5 14.5 20.5 22		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) [1)] $R_L = 32\Omega$, P_{out} = 10mW, 20Hz ≤ F ≤ 20kHz $R_L = 16\Omega$, P_{out} = 16mW, 20Hz ≤ F ≤ 20kHz		 0.03 0.03		%
PSRR	Power Supply Rejection Ratio (A_V=1), inputs floating F = 100Hz, Vripple = 100mVpp		75		dB
I_O	Max Output Current THD +N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$	45	56		mA
V_O	Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$	 2.14 1.97	 0.25 2.25 0.35 2.15	 0.325 0.45 	V
SNR	Signal-to-Noise Ratio (Filter Type A, A_V=-1) ($R_L = 32\Omega$, THD +N < 0.2%, 20Hz ≤ F ≤ 20kHz)	89	102		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz		 100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.45	0.7		V/µs

1. Fig. 68 to 79 show dispersion of these parameters.

2. All electrical values are guaranteed with correlation measurements at 2V and 5V

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω	 7 9.5	 8 9 11.5 13		mW
THD + N	Total Harmonic Distortion + Noise (A_V=-1) [1] R_L = 32Ω, P_{out} = 6.5mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 8mW, 20Hz ≤ F ≤ 20kHz		 0.02 0.025		%
PSRR	Power Supply Rejection Ratio (A_V=1), inputs floating F = 100Hz, Vripple = 100mVpp		75		dB
I_O	Max Output Current THD +N < 1%, R_L = 16Ω connected between out and $V_{CC}/2$	33	41.5		mA
V_O	Output Swing V_{OL} : R_L = 32Ω V_{OH} : R_L = 32Ω V_{OL} : R_L = 16Ω V_{OH} : R_L = 16Ω	 1.67 1.53	 0.24 1.73 0.33 1.63	 0.295 0.41 	V
SNR	Signal-to-Noise Ratio (Filter Type A, A_V=-1) (R_L = 32Ω, THD +N < 0.2%, 20Hz ≤ F ≤ 20kHz)	88	101		dB
Crosstalk	Channel Separation, R_L = 32Ω F = 1kHz F = 20Hz to 20kHz Channel Separation, R_L = 16Ω F = 1kHz F = 20Hz to 20kHz		 100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwith Product (R_L = 32Ω)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting (R_L = 16Ω)	0.42	0.65		V/µs

1. Fig. 68 to 79 show dispersion of these parameters.

Index of Graphs

Fig. 1 : Open Loop Gain and Phase vs Frequency

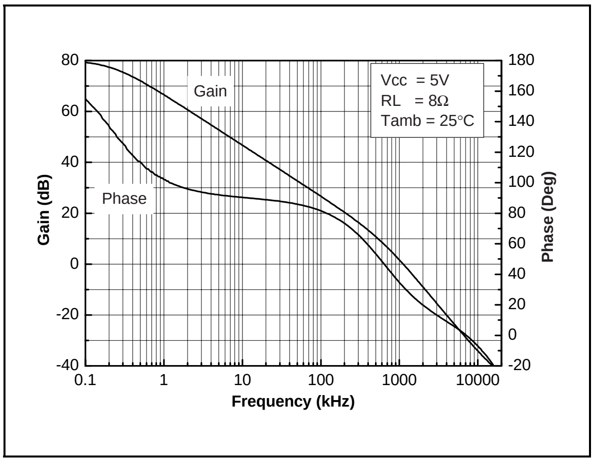


Fig. 2 : Open Loop Gain and Phase vs Frequency

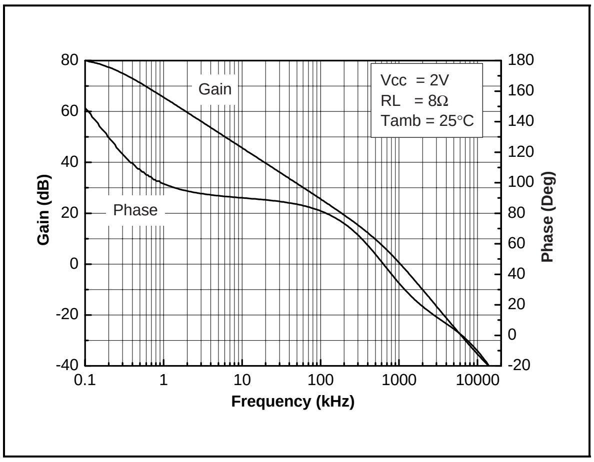


Fig. 3 : Open Loop Gain and Phase vs Frequency

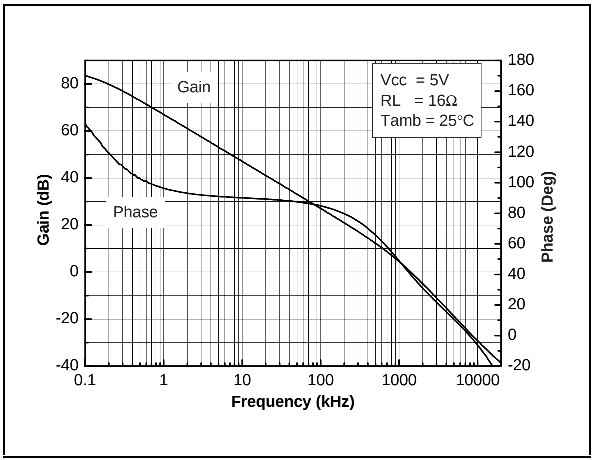


Fig. 4 : Open Loop Gain and Phase vs Frequency

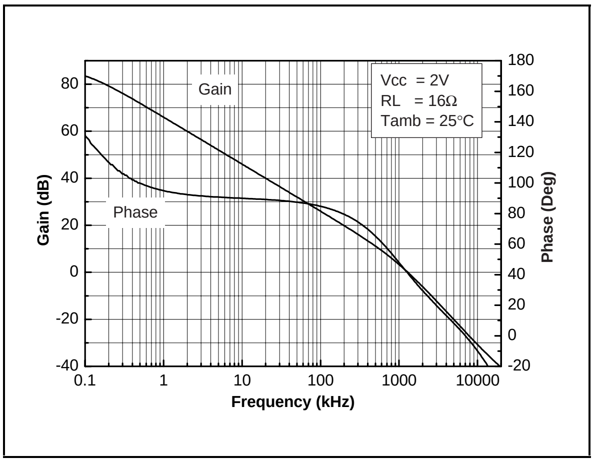


Fig. 5 : Open Loop Gain and Phase vs Frequency

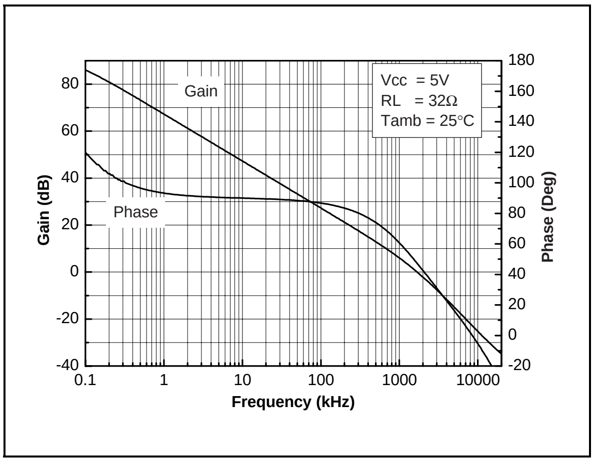


Fig. 6 : Open Loop Gain and Phase vs Frequency

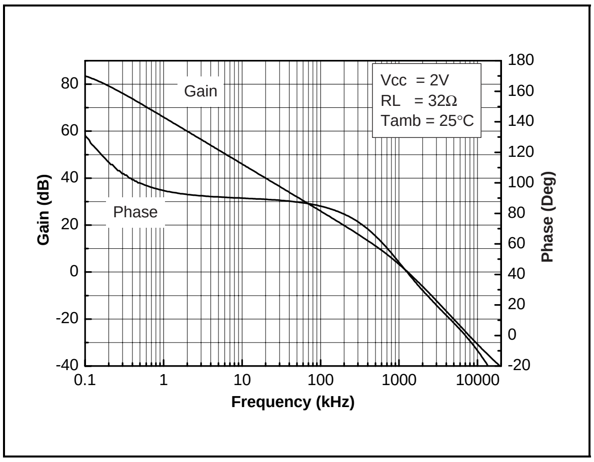


Fig. 7 : Open Loop Gain and Phase vs Frequency

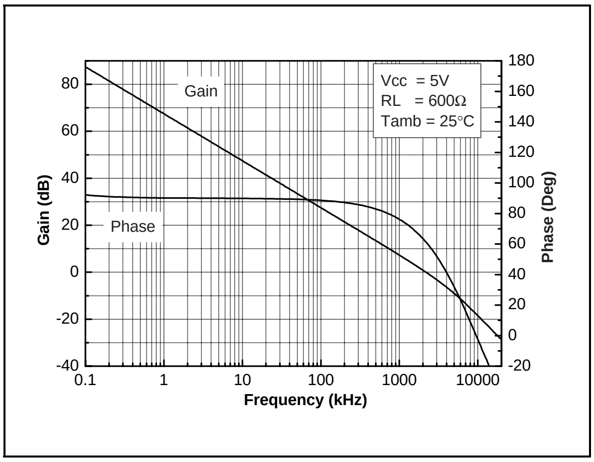


Fig. 8 : Open Loop Gain and Phase vs Frequency

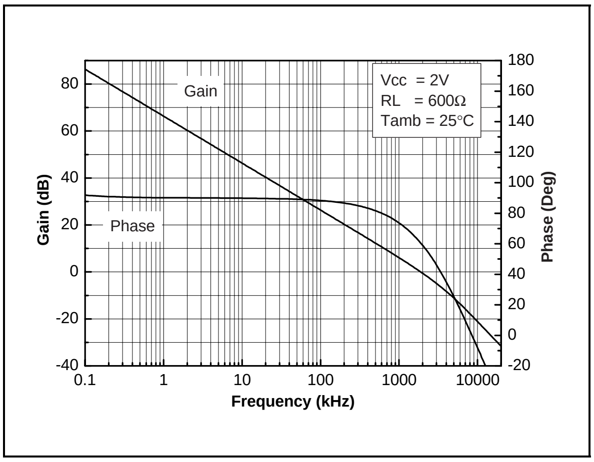


Fig. 9 : Open Loop Gain and Phase vs Frequency

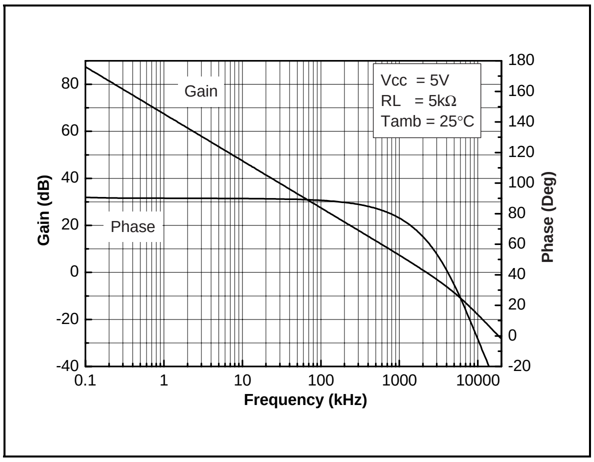


Fig. 10 : Open Loop Gain and Phase vs Frequency

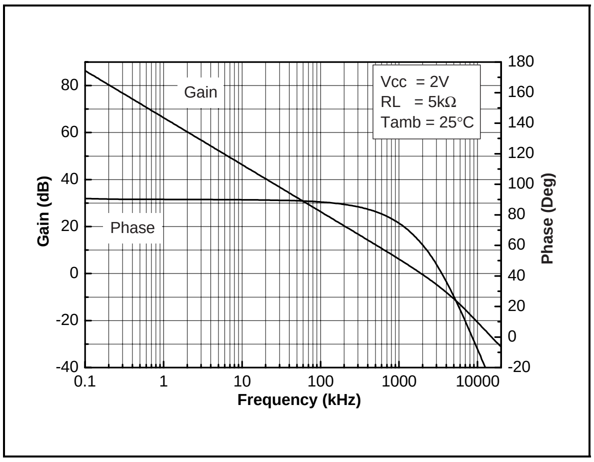


Fig. 11 : Phase Margin vs Power Supply Voltage

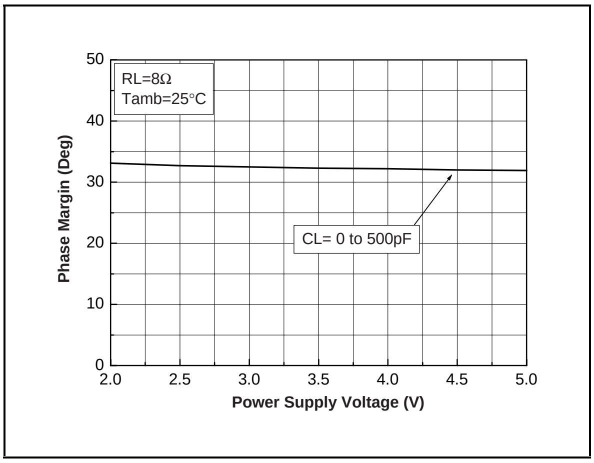


Fig. 12 : Gain Margin vs Power Supply Voltage

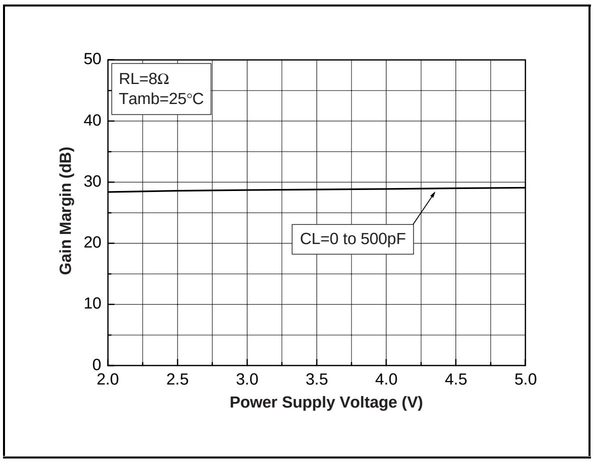


Fig. 13 : Phase Margin vs Power Supply Voltage

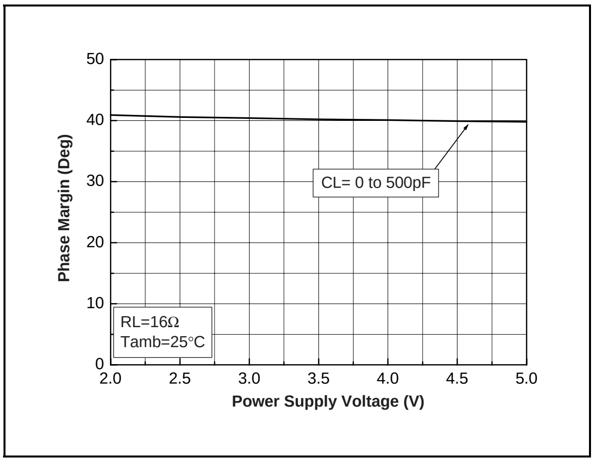


Fig. 14 : Gain Margin vs Power Supply Voltage

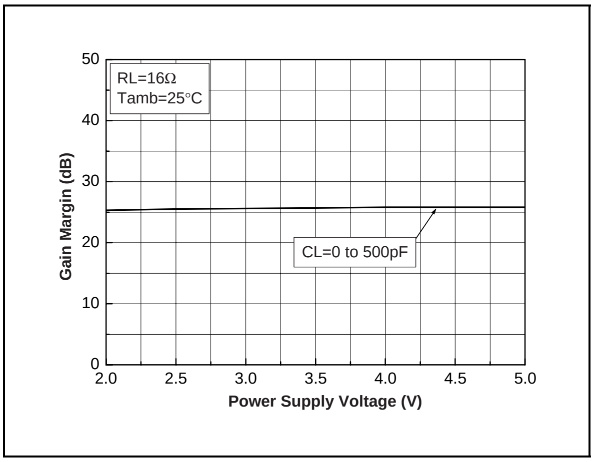


Fig. 15 : Phase Margin vs Power Supply Voltage

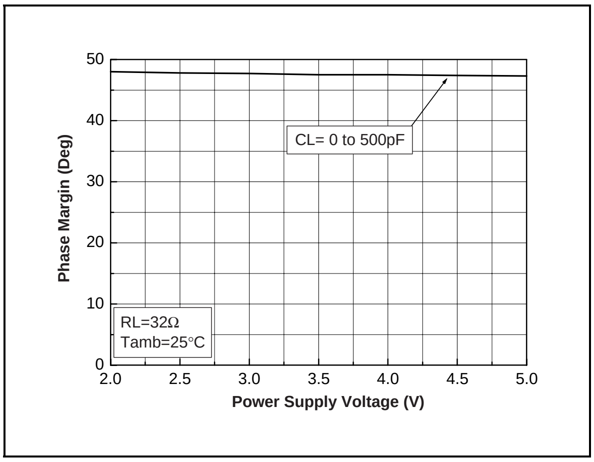


Fig. 16 : Gain Margin vs Power Supply Voltage

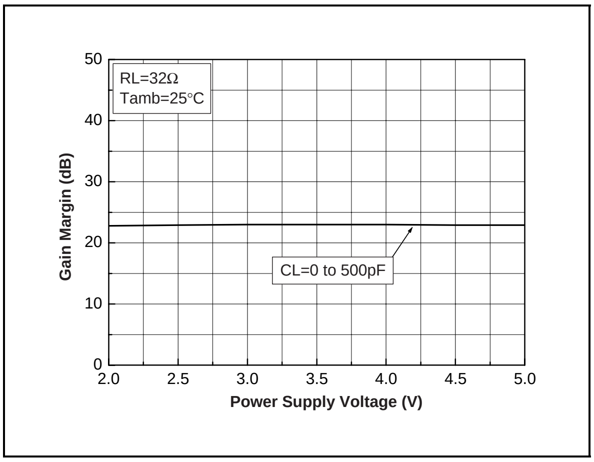


Fig. 17 : Phase Margin vs Power Supply Voltage

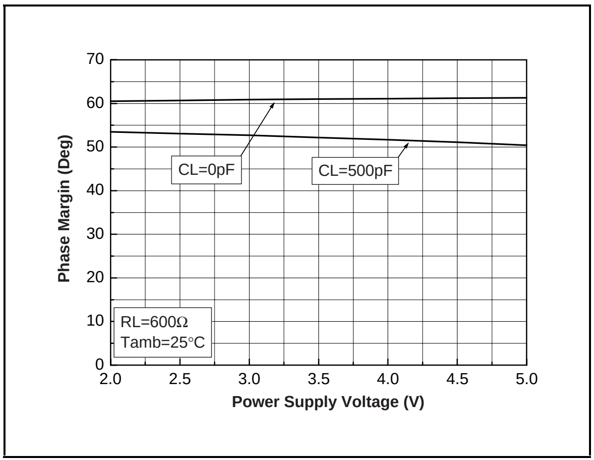


Fig. 18 : Gain Margin vs Power Supply Voltage

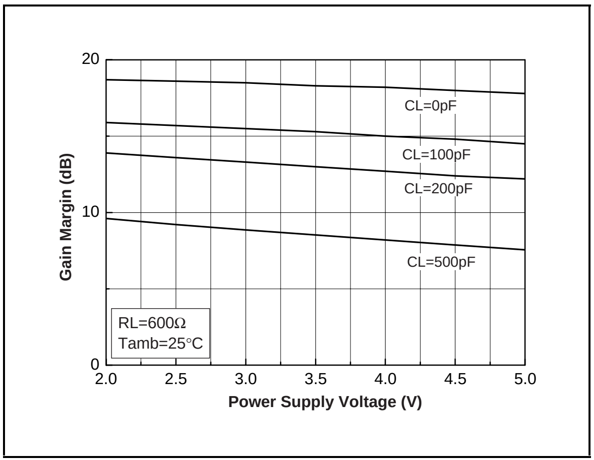


Fig. 19 : Phase Margin vs Power Supply Voltage

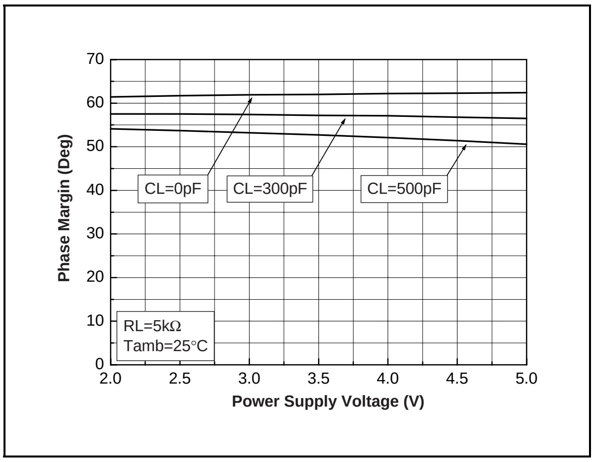


Fig. 20 : Gain Margin vs Power Supply Voltage

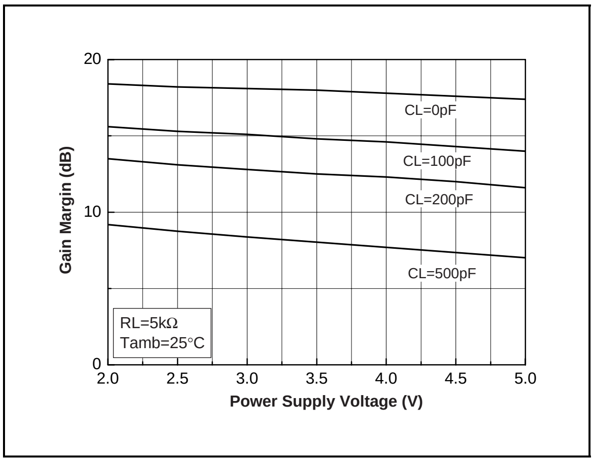


Fig. 21 : Output Power vs Power Supply Voltage

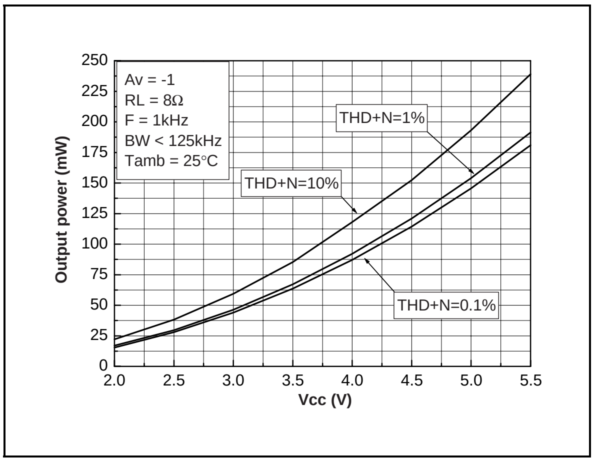


Fig. 22 : Output Power vs Power Supply Voltage

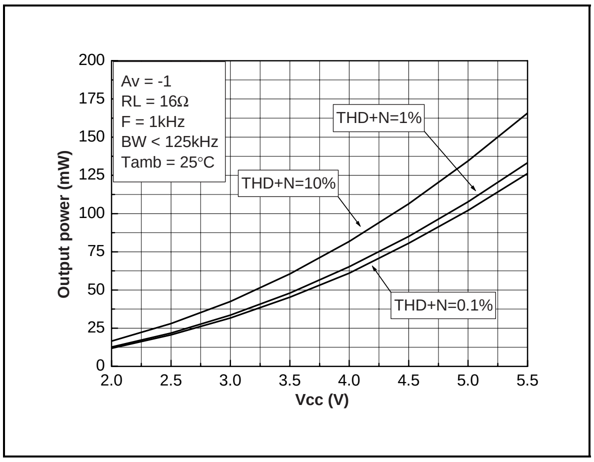


Fig. 23 :Output Power vs Power Supply Voltage

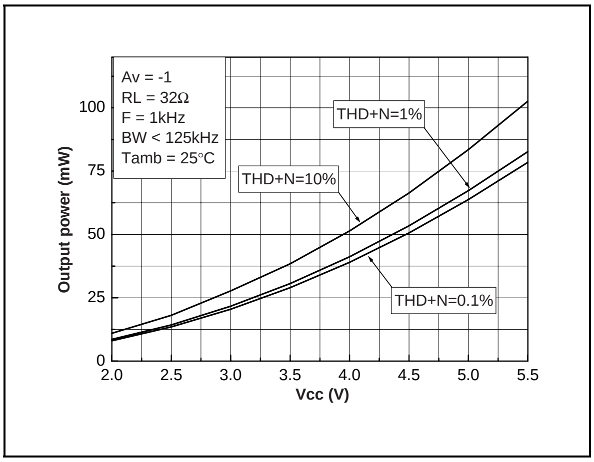


Fig. 24 : Output Power vs Load Resistance

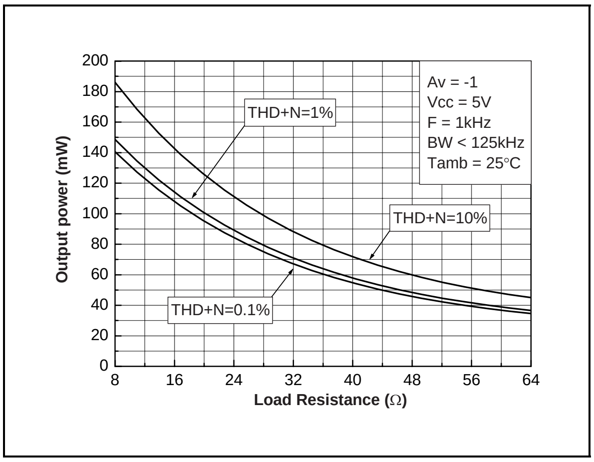


Fig. 25 : Output Power vs Load Resistance

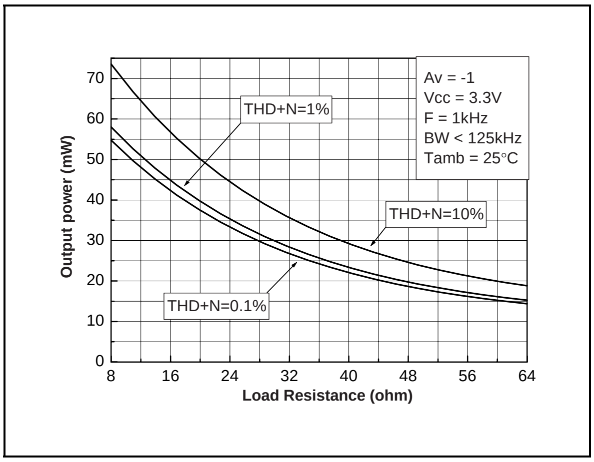


Fig. 26 : Output Power vs Load Resistance

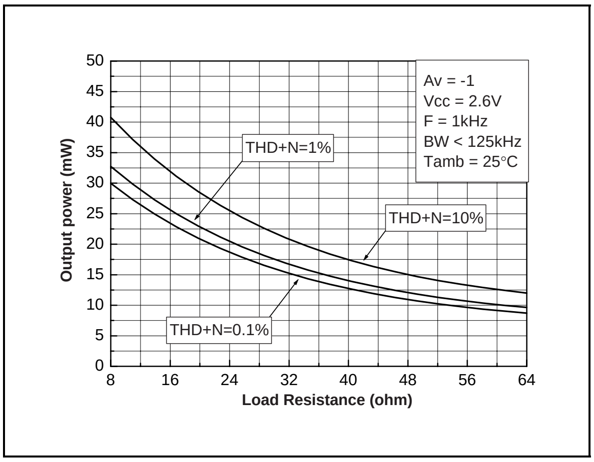


Fig. 27 : Output Power vs Load Resistance

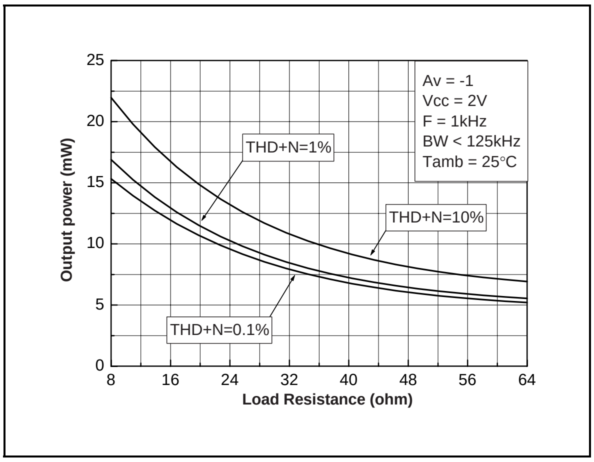


Fig. 28 : Power Dissipation vs Output Power

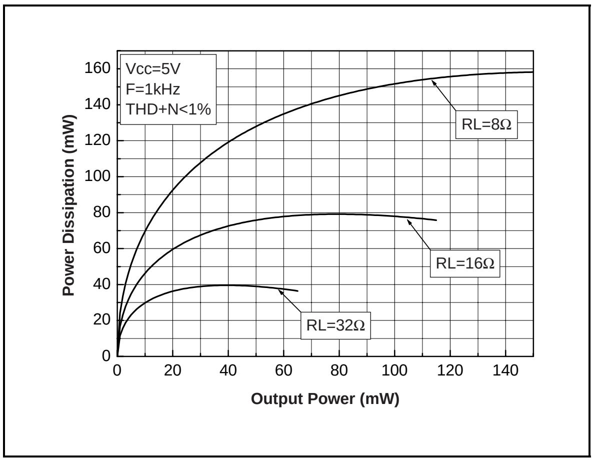


Fig. 29 : Power Dissipation vs Output Power

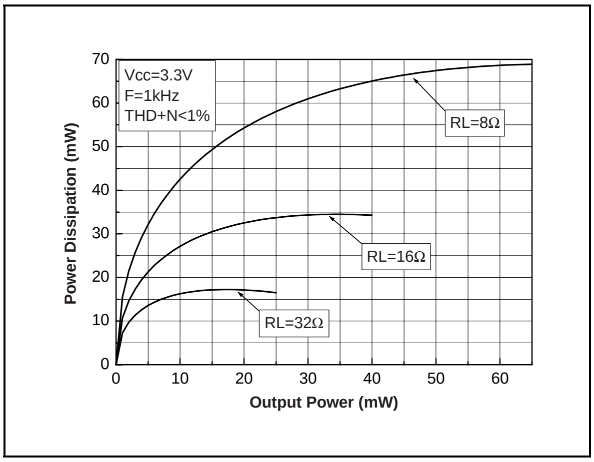


Fig. 30 : Power Dissipation vs Output Power

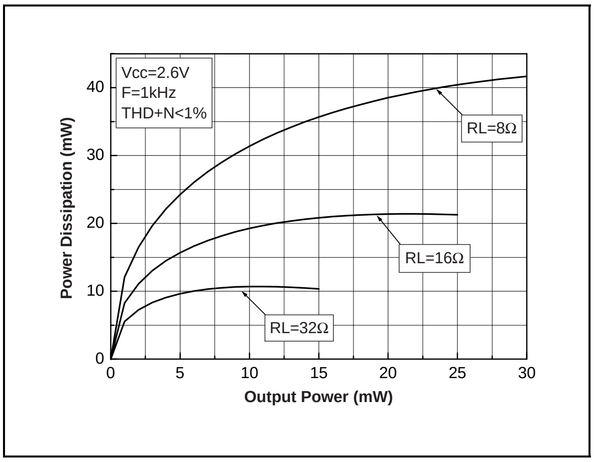


Fig. 31 : Power Dissipation vs Output Power

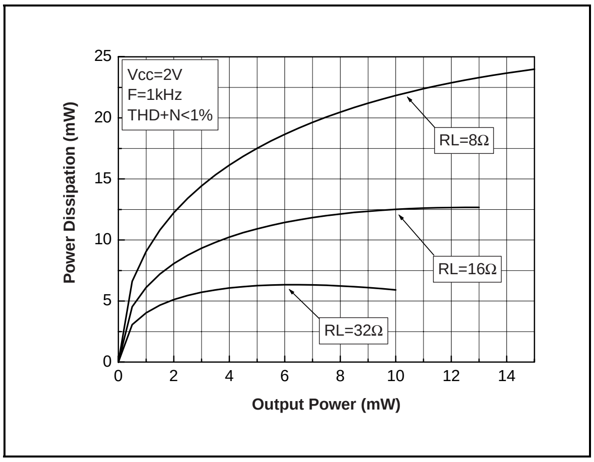


Fig. 32 : Power Derating vs Ambiant Temperature

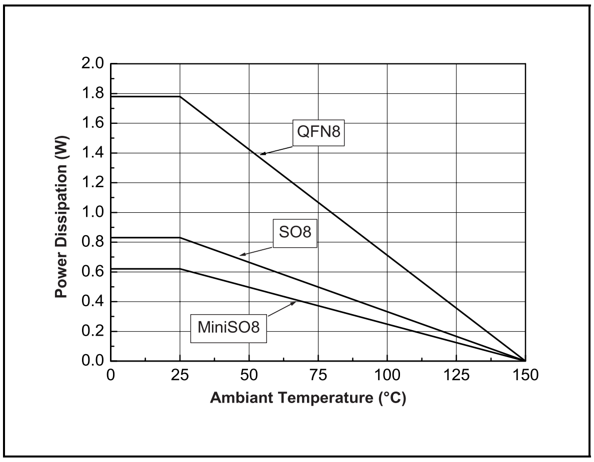


Fig. 33 : Current Consumption vs Power Supply Voltage

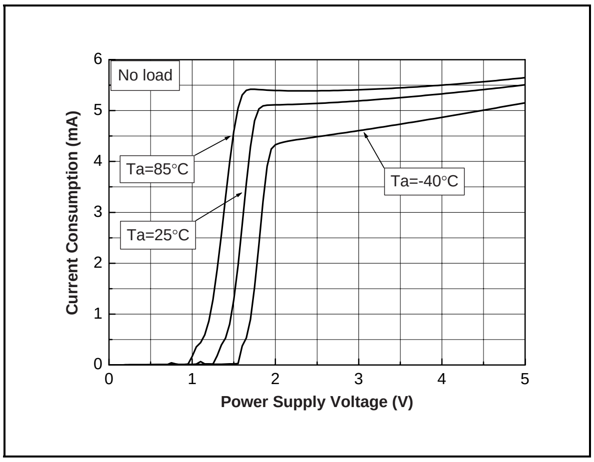


Fig. 34 : Power Supply Rejection Ration vs Frequency

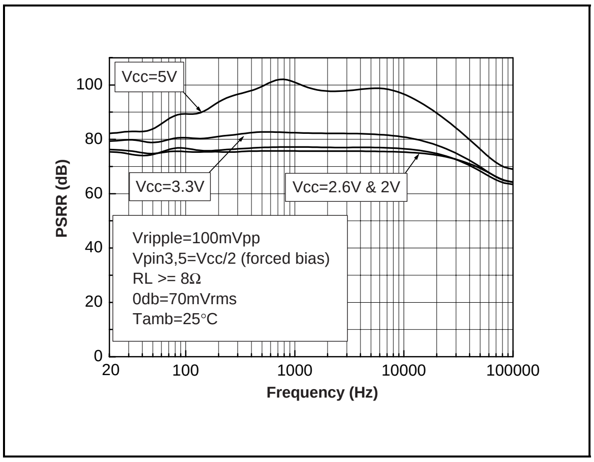


Fig. 35 : THD + N vs Output Power

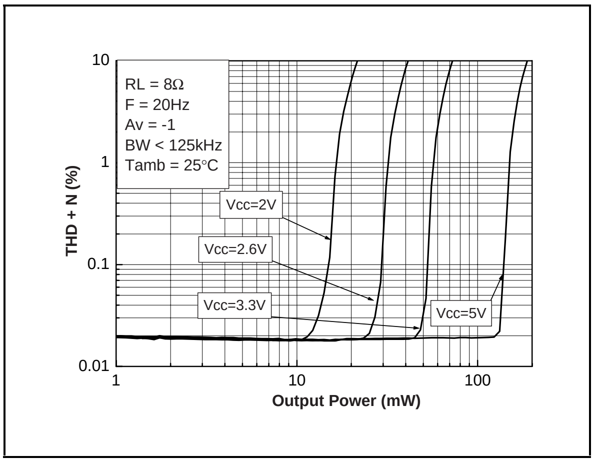


Fig. 36 : THD + N vs Output Power

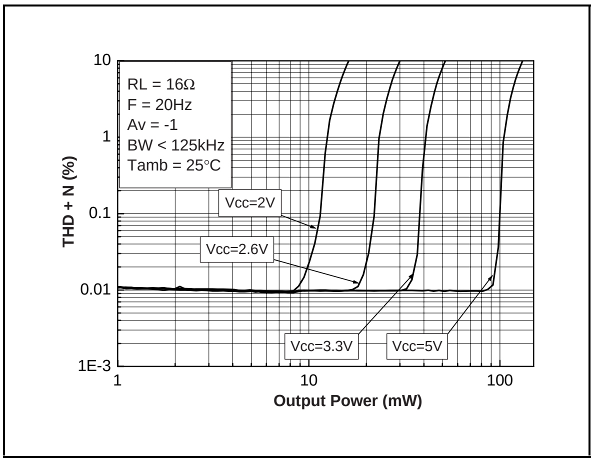


Fig. 37 : THD + N vs Output Power

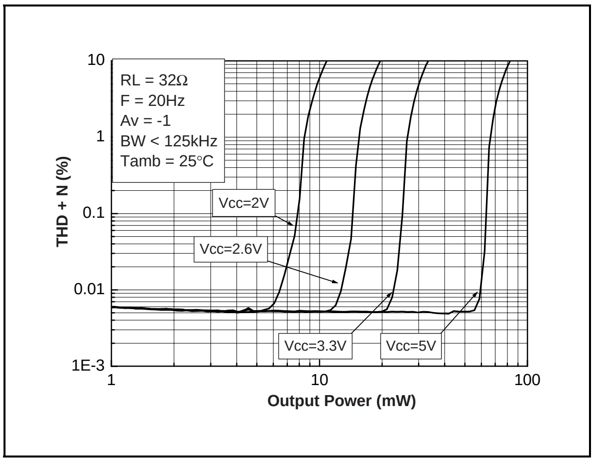


Fig. 38 : THD + N vs Output Power

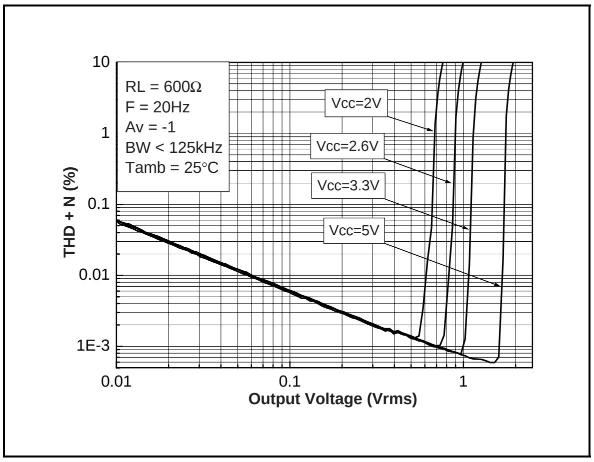


Fig. 39 : THD + N vs Output Power

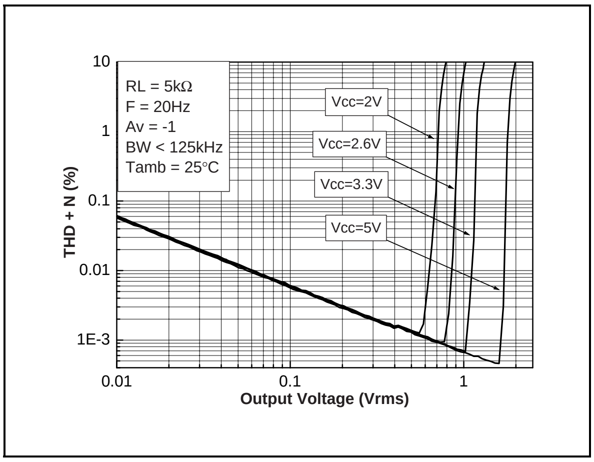


Fig. 40 : THD + N vs Output Power

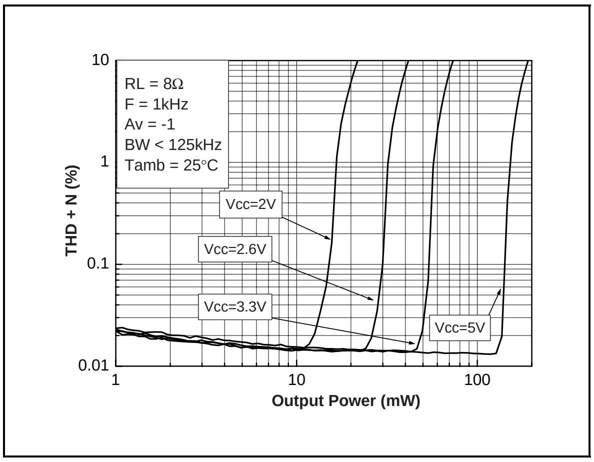


Fig. 41 : THD + N vs Output Power

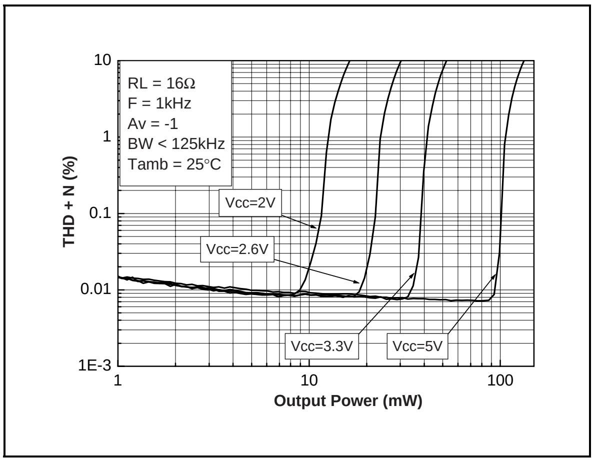


Fig. 42 : THD + N vs Output Power

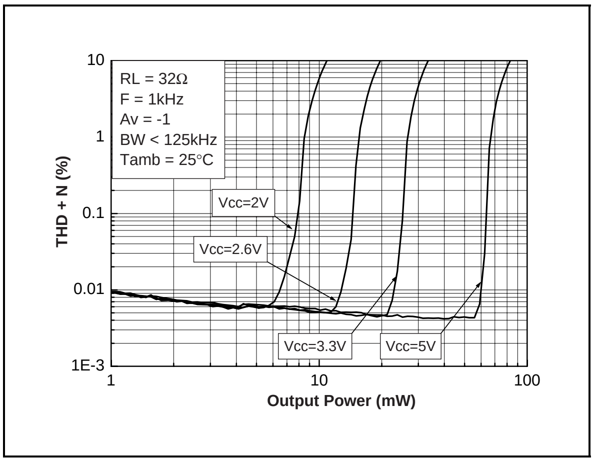


Fig. 43 : THD + N vs Output Power

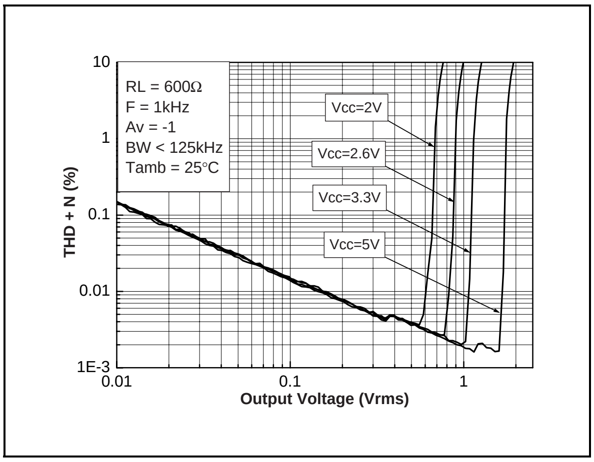


Fig. 44 : THD + N vs Output Power

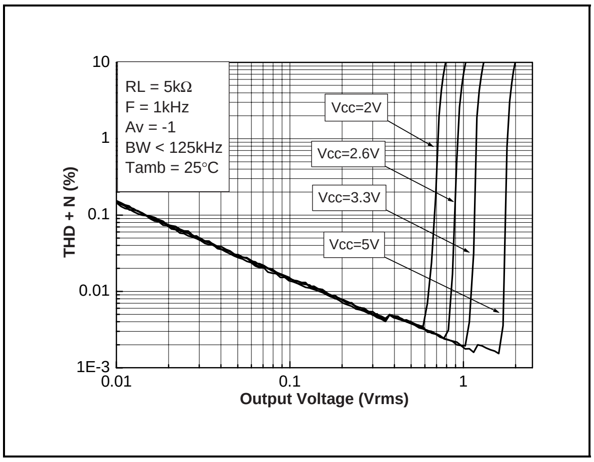


Fig. 45 : THD + N vs Output Power

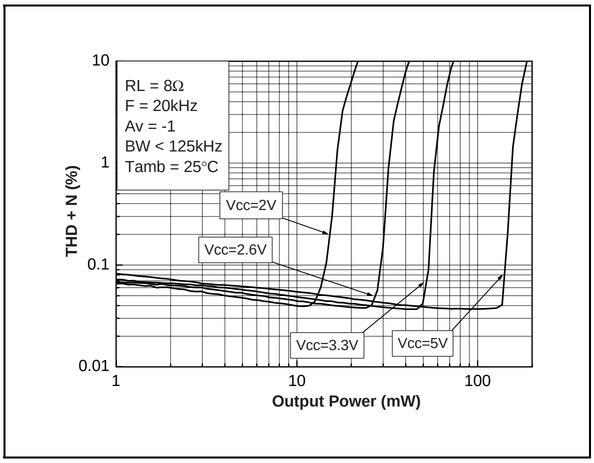


Fig. 46 : THD + N vs Output Power

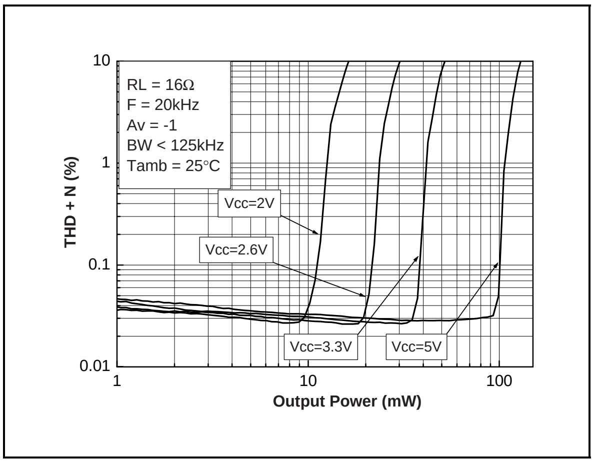


Fig. 47 : THD + N vs Output Power

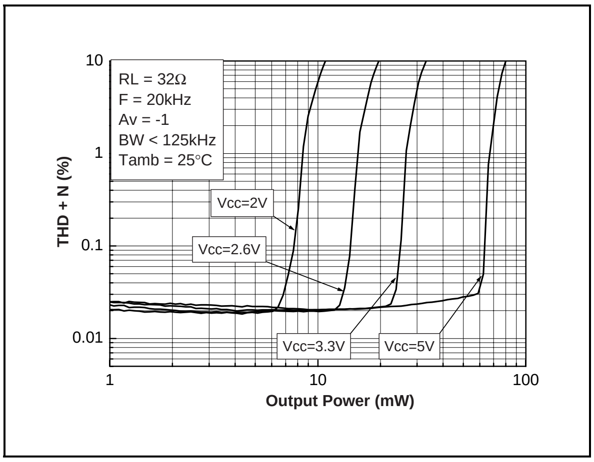


Fig. 48 : THD + N vs Output Power

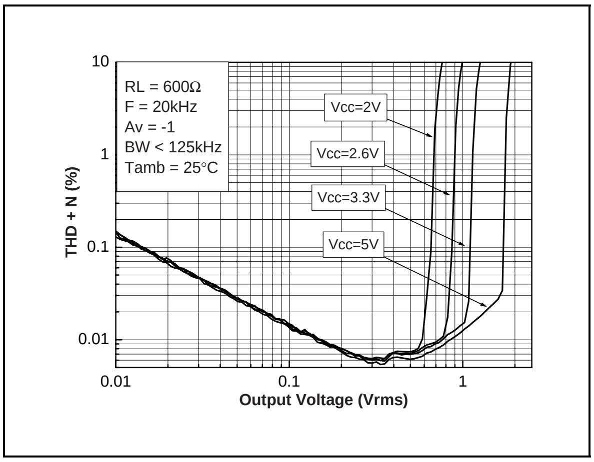


Fig. 49 : THD + N vs Output Power

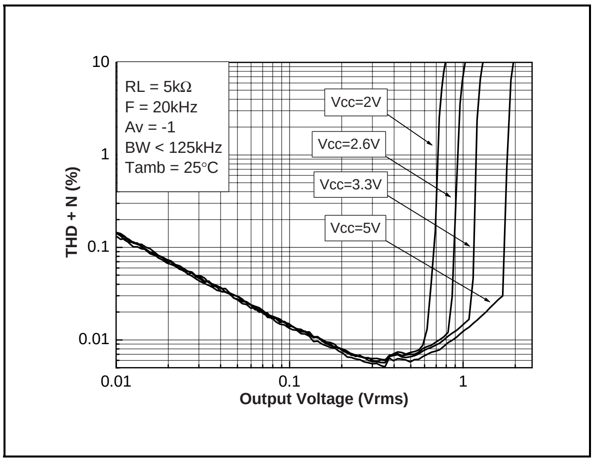


Fig. 50 : THD + N vs Frequency

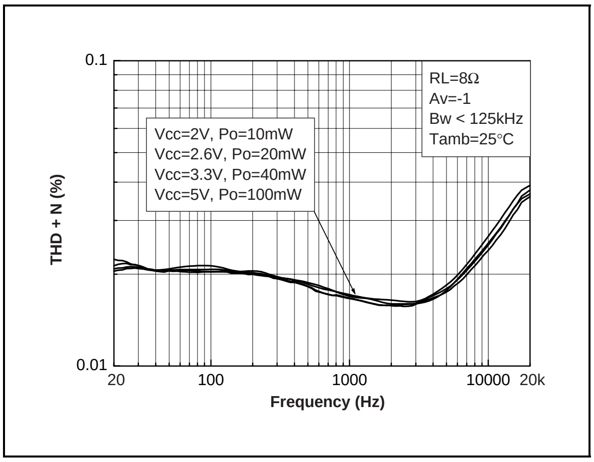


Fig. 51 : THD + N vs Frequency

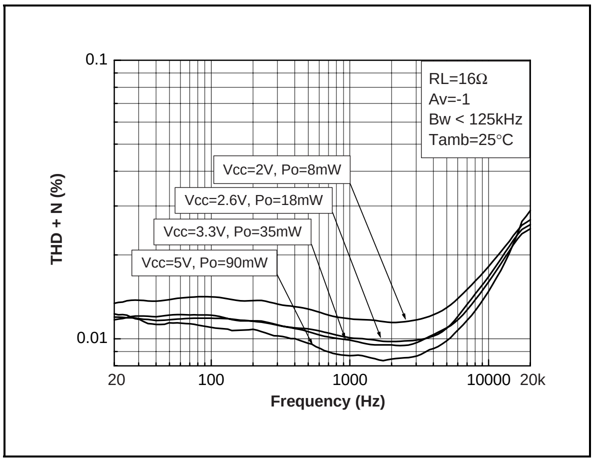


Fig. 52 : THD + N vs Frequency

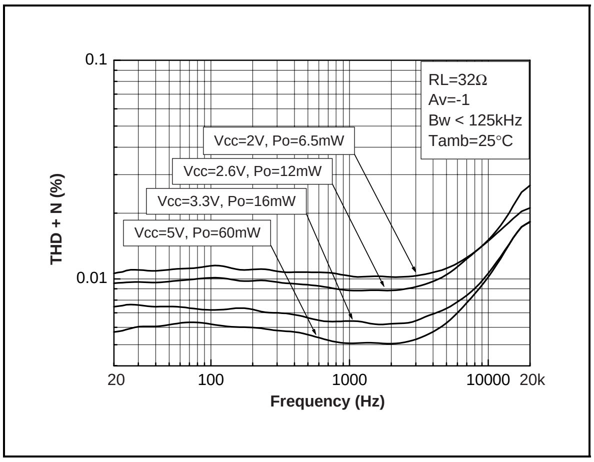


Fig. 53 : THD + N vs Frequency

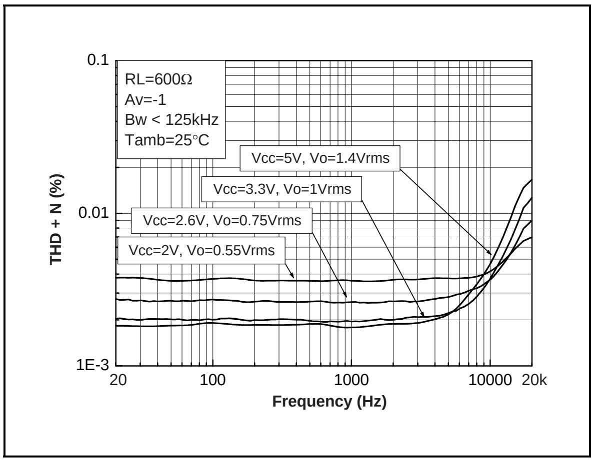


Fig. 54 : THD + N vs Frequency

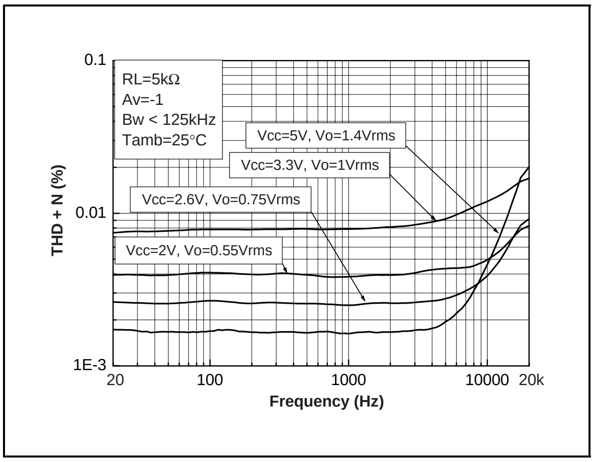


Fig. 55 : Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

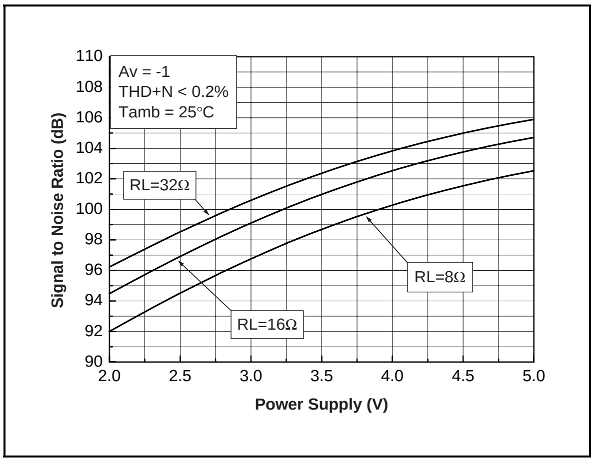


Fig. 56 : Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

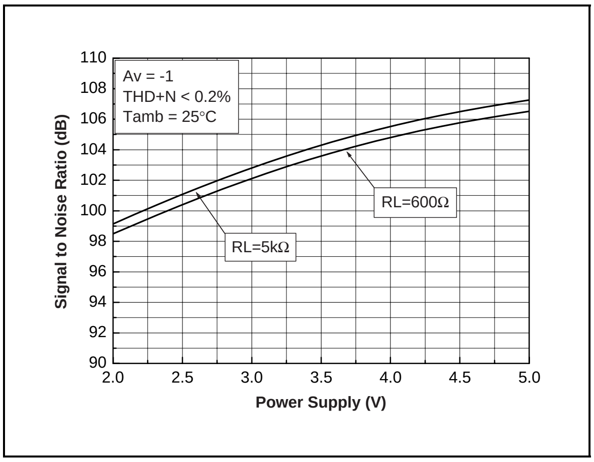


Fig. 57 : Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

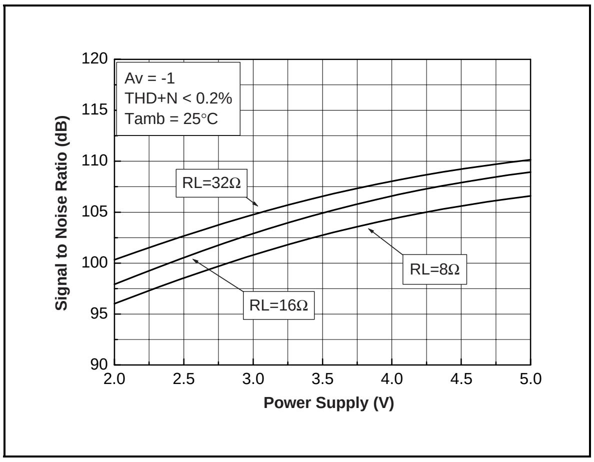


Fig. 58 : Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

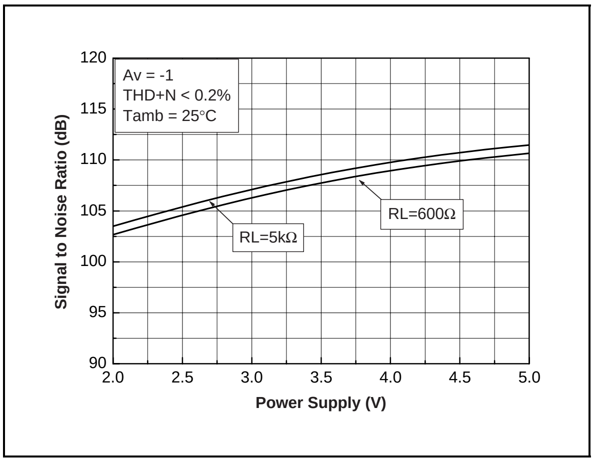


Fig. 59 : Equivalent Input Noise Voltage vs Frequency

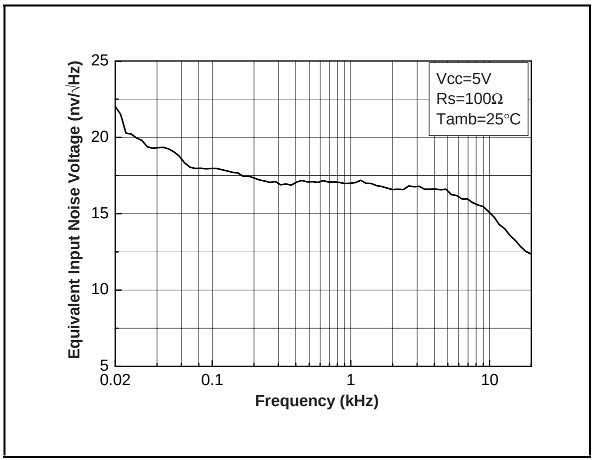


Fig. 60 : Output Voltage Swing vs Power Supply Voltage

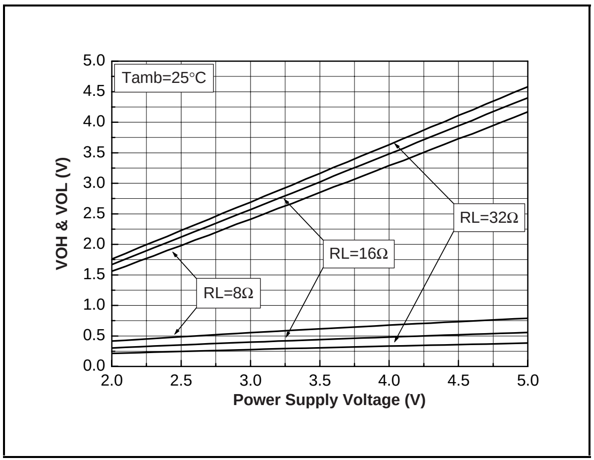


Fig. 61 : Crosstalk vs Frequency

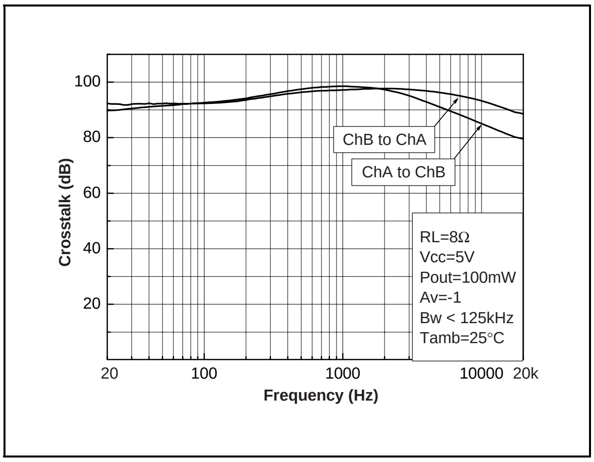


Fig. 62 : Crosstalk vs Frequency

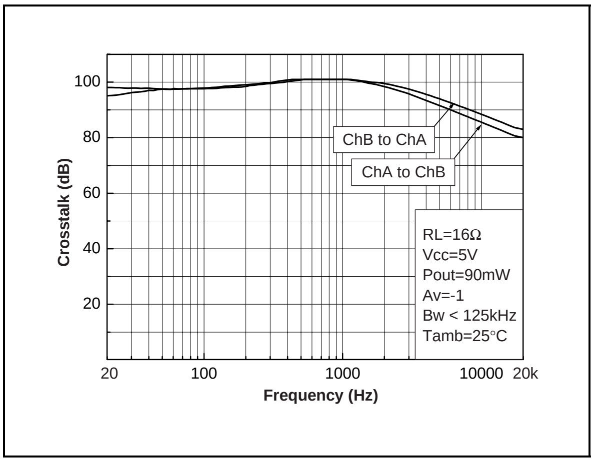


Fig. 63 : Crosstalk vs Frequency

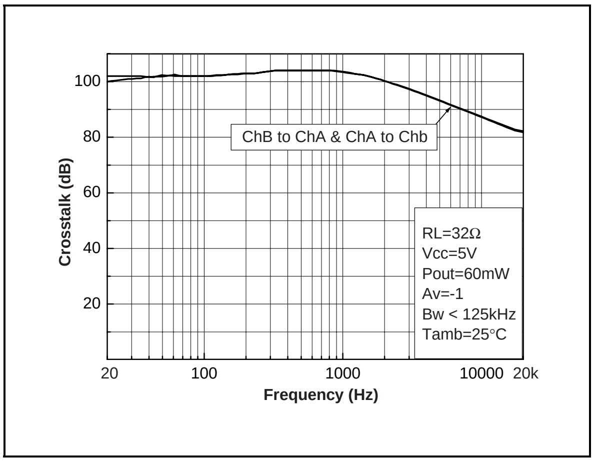


Fig. 64 : Crosstalk vs Frequency

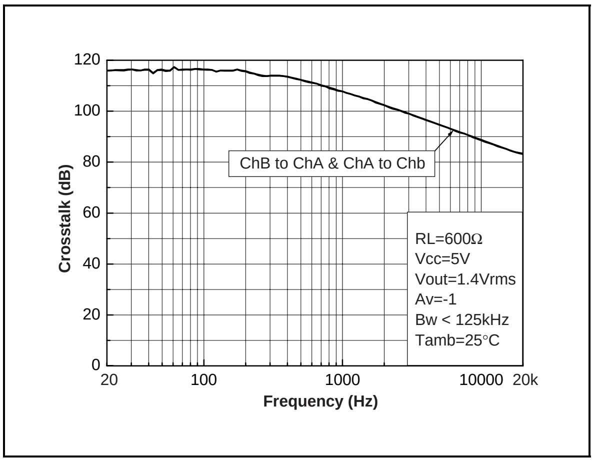


Fig. 65 : Crosstalk vs Frequency

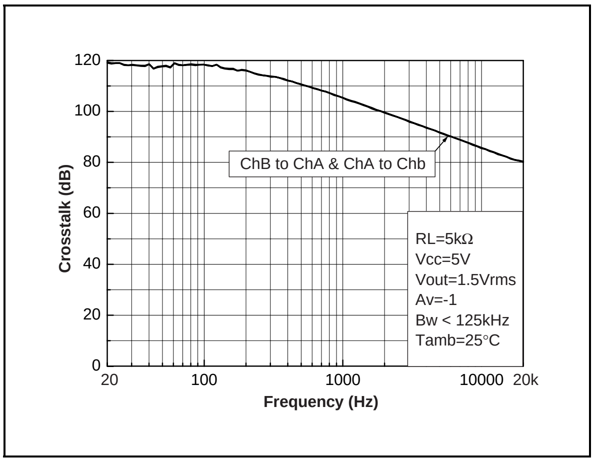


Fig. 66 : Lower Cut Off Frequency vs Output Capacitor

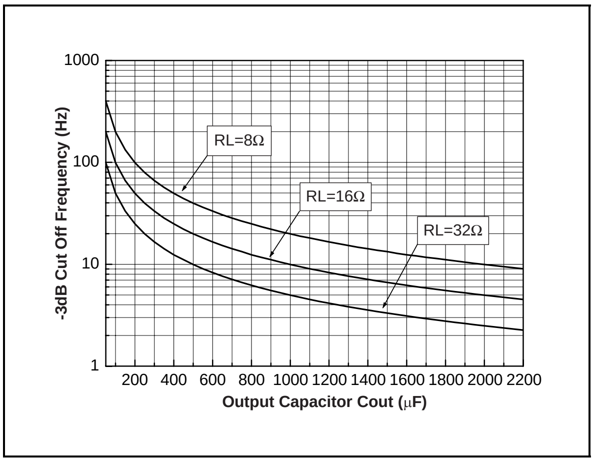


Fig. 67 : Lower Cut Off Frequency vs Input Capacitor

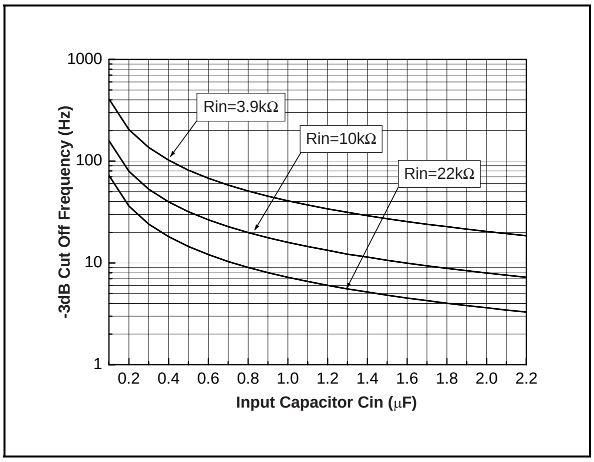


Fig. 68 : Typical Distribution of THD+N

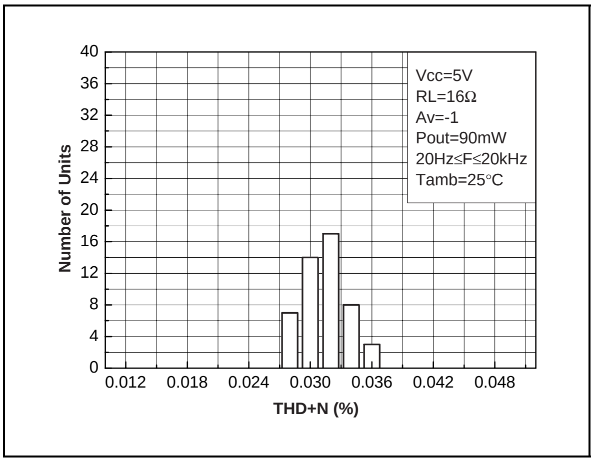


Fig. 69 : Best Case Distribution of THD+N

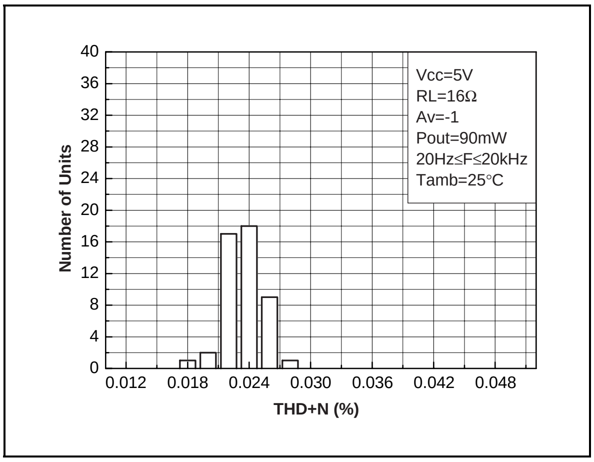


Fig. 70 : Worst Case Distribution of THD+N

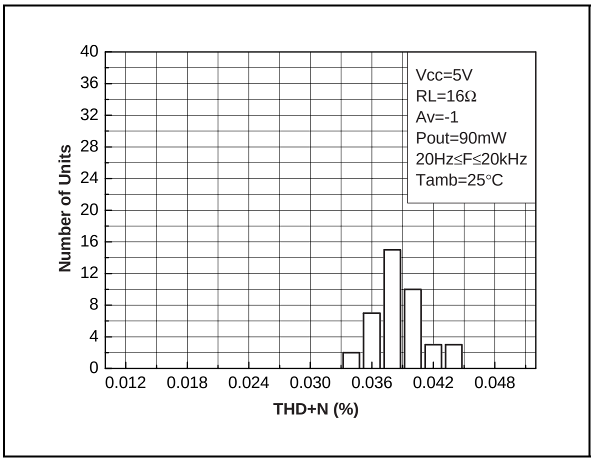


Fig. 71 : Typical Distribution of THD+N

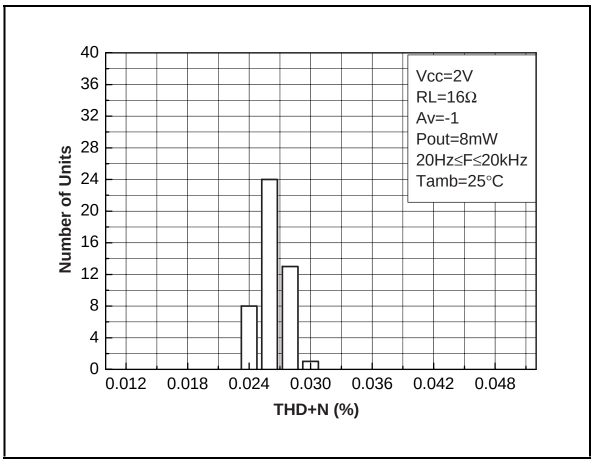


Fig. 72 : Best Case Distribution of THD+N

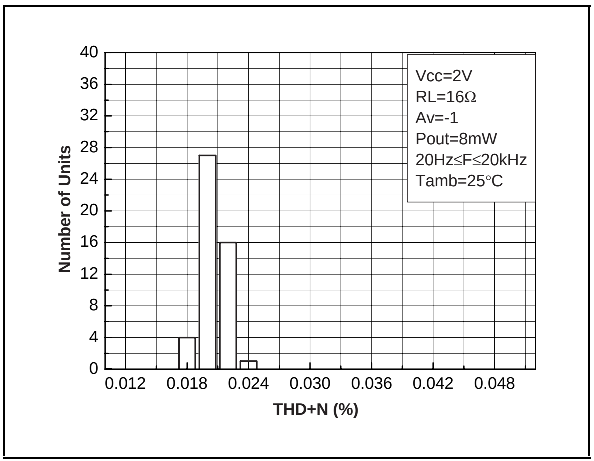


Fig. 73 : Worst Case Distribution of THD+N

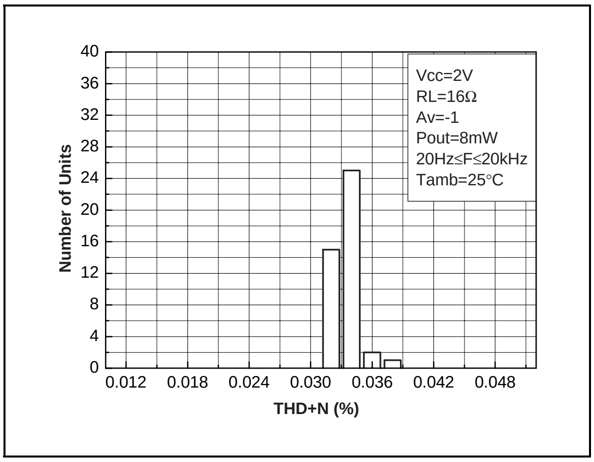


Fig. 74 : Typical Distribution of THD+N

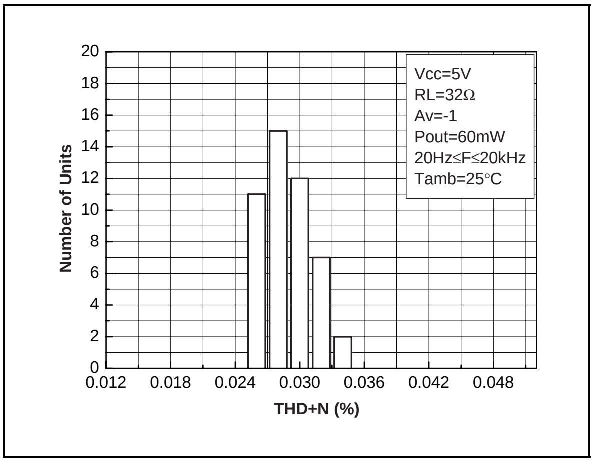


Fig. 75 : Best Case Distribution of THD+N

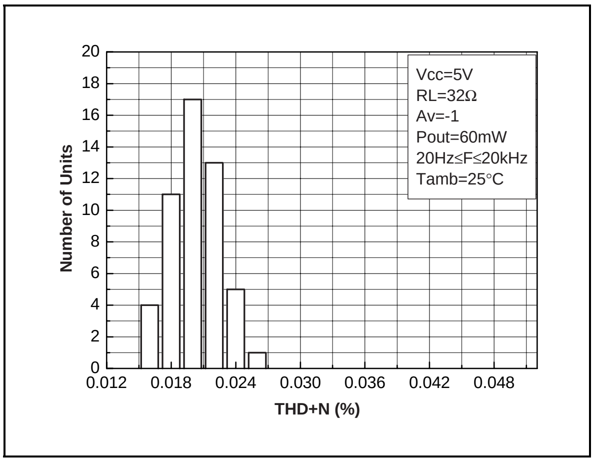


Fig. 76 : Worst Case Distribution of THD+N

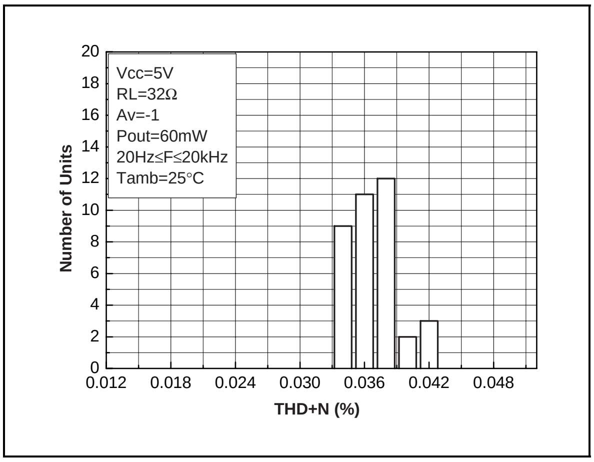


Fig. 77 : Typical Distribution of THD+N

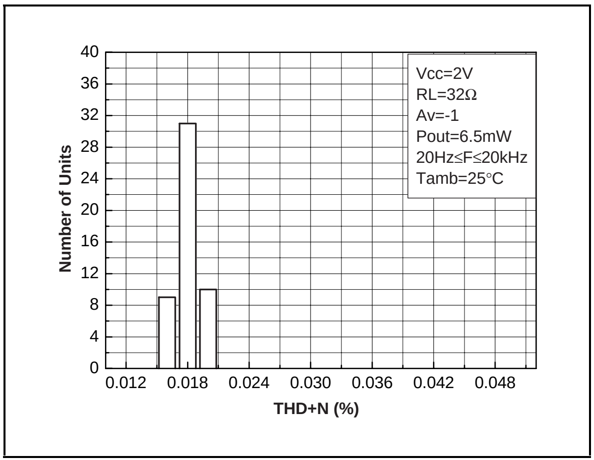


Fig. 78 : Best Case Distribution of THD+N

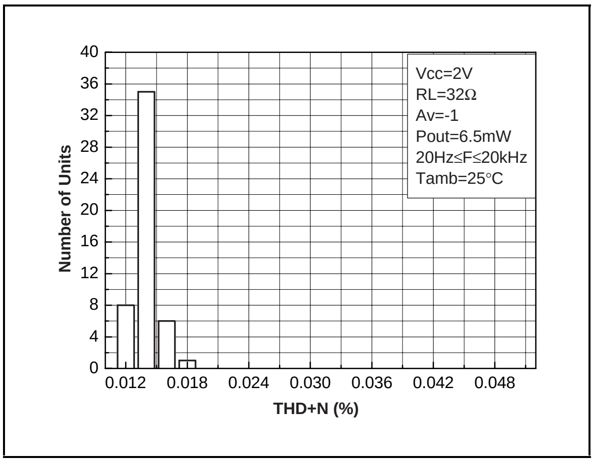
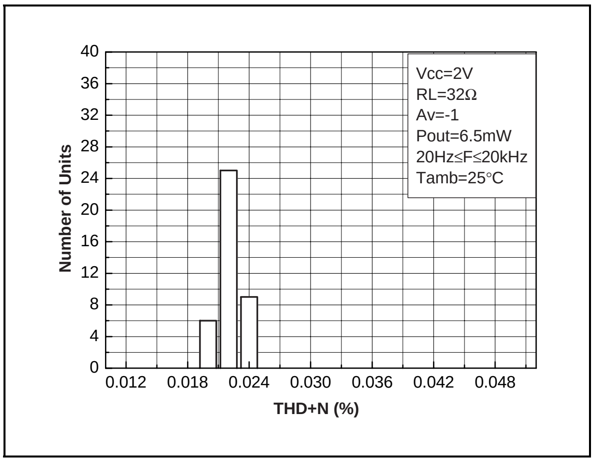


Fig. 79 : Worst Case Distribution of THD+N



PACKAGE MECHANICAL DATA

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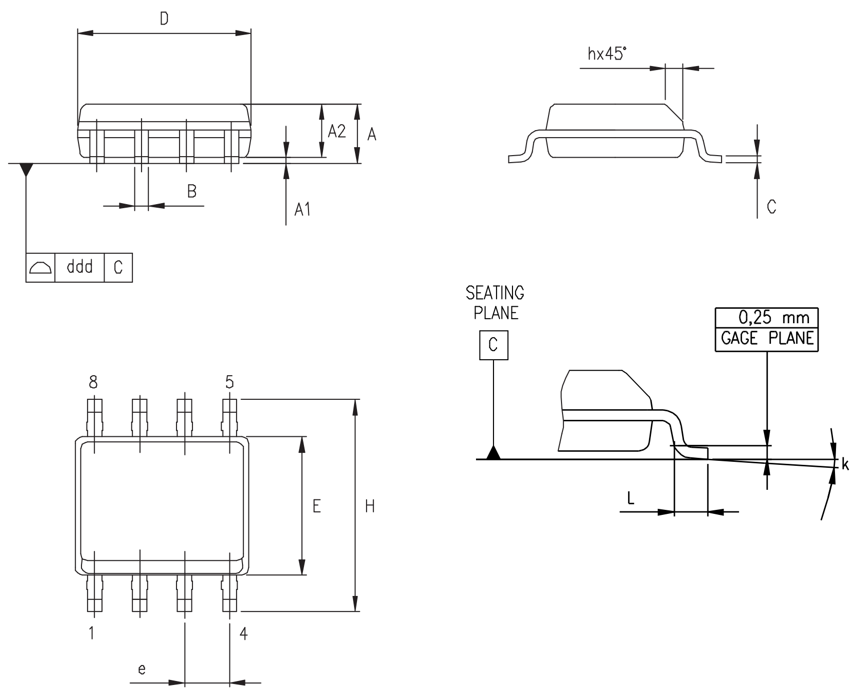
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

PACKAGE MECHANICAL DATA

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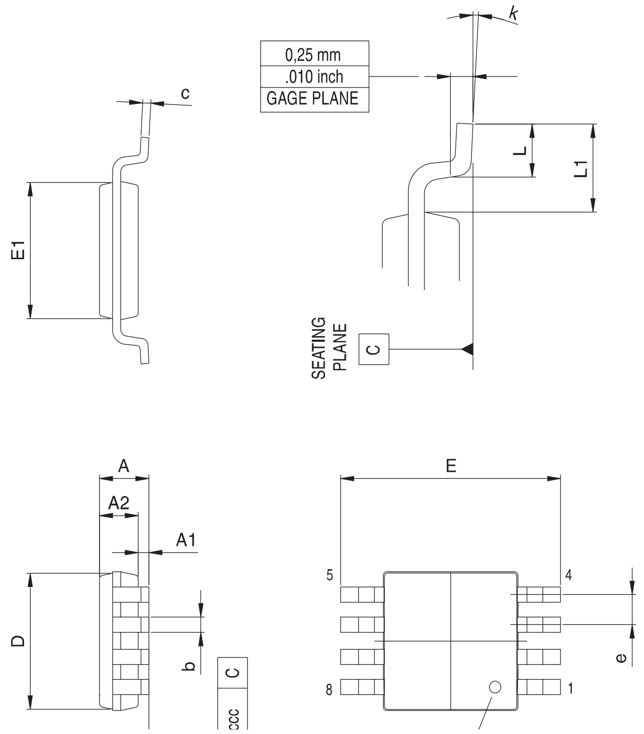
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



PACKAGE MECHANICAL DATA

DFN8 (3x3) MECHANICAL DATA

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A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7