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TS4851

MONO 1 W SPEAKER AND STEREO 160 mW HEADSET BTL DRIVERS WITH DIGITAL VOLUME CONTROL

- **Operating from V_{CC} = 3 V to 5.5 V**
- **Rail to rail input/output**
- **Speaker driver with 1 W output @ Vcc = 5 V, THD+N = 1%, F = 1 kHz, 8 Ω load**
- **Headset drivers with 160 mW output @ Vcc = 5 V, THD+N = 1%, F = 1 kHz, 32 Ω load**
- **Headset output is 30 mW in stereo @ Vcc = 3 V**
- **THD+N < 0.5% Max @ 20 mW into 32 Ω BTL, 50 Hz < Frequency < 20 kHz**
- **32-step digital volume control from -34.5 dB to +12 dB**
- **+6 dB power up volume and full standby**
- **8 different output modes**
- **Pop & click reduction circuitry**
- **Low shutdown current (< 100 nA)**
- **Thermal shutdown protection**
- **Flip-chip package 18 x 300 µm bumps**

DESCRIPTION

The TS4851 is a low power audio amplifier that can drive either both a mono speaker or a stereo headset. To the speaker, it can deliver 400 mW (typ.) of continuous RMS output power into an 8 Ω load with a 1% THD+N value. To the headset driver, the amplifier can deliver 30 mW (typ.) per channel of continuous average power into a stereo 32 Ω bridged-tied load with 0.5% THD+N @ 3.3 V.

This device features a 32-step digital volume control and 8 different output selections. The digital volume and output modes are controlled through a three-digit SPI interface bus.

APPLICATIONS

- Mobile Phones

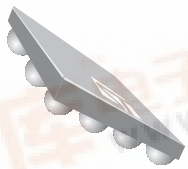
ORDER CODE

Part Number	Temperature Range	Package	
		J	
TS4851IJT	-40, +85°C	•	

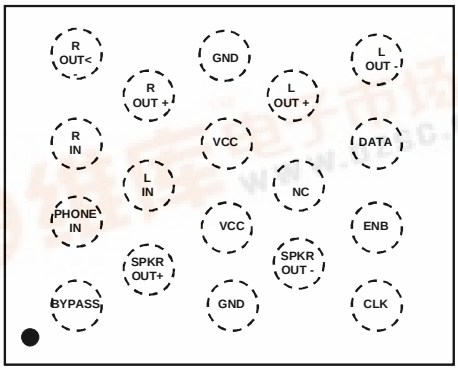
J = Flip Chip Package - only available in Tape & Reel (JT))

PIN CONNECTIONS (top view)

TS485IJT - Flip Chip



Pin Out (top view)



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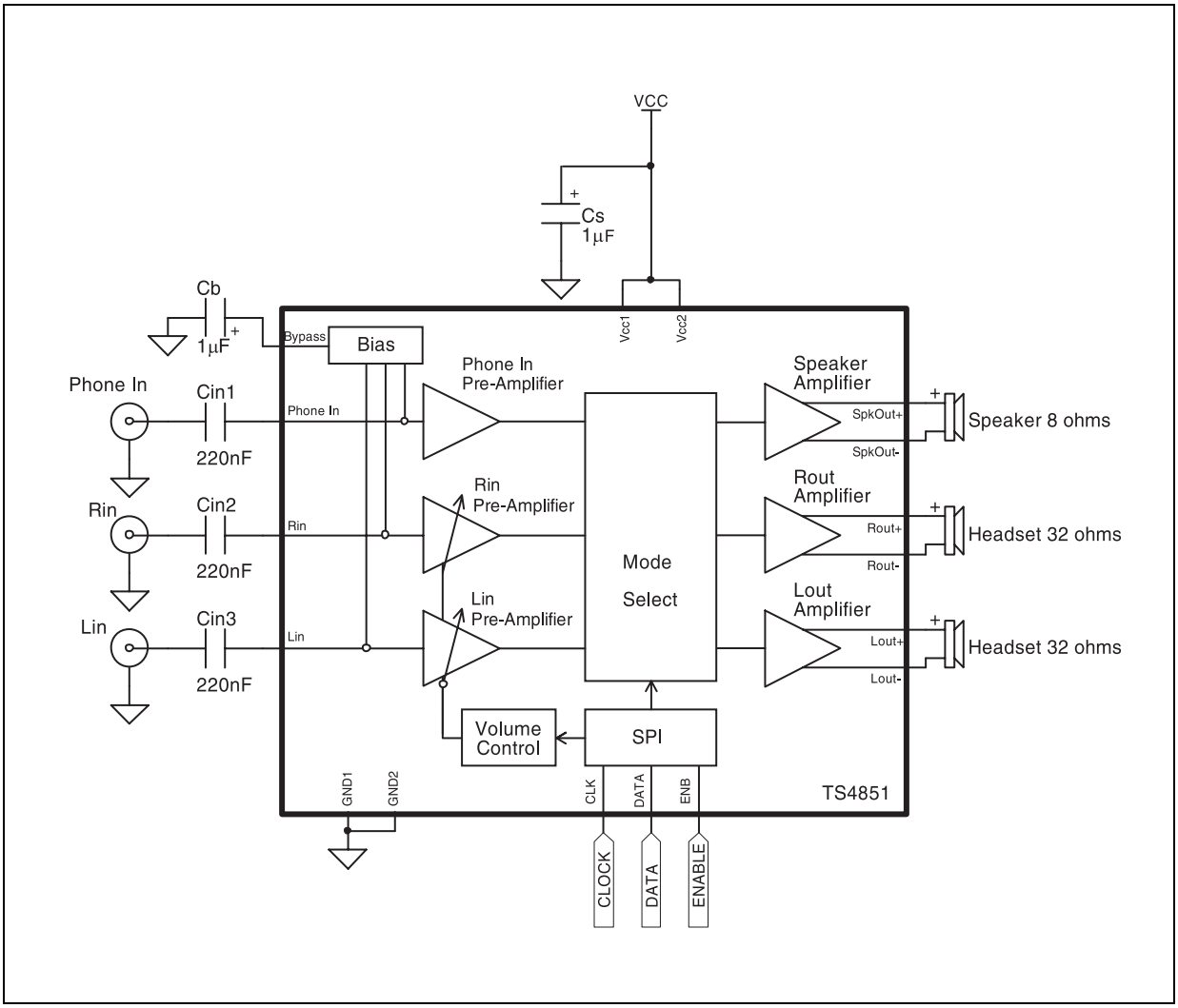
1 APPLICATION INFORMATION FOR A TYPICAL APPLICATION



External component descriptions

Component	Functional Description
C_{in}	This is the input coupling capacitor. It blocks the DC voltage at, and couples the input signal to the amplifier's input terminals. Cin also creates a highpass filter with the internal input impedance Zin at Fc =1/ (2πi x Zin x Cin).
C_S	This is the Supply Bypass capacitor. It provides power supply filtering.
C_B	This is the Bypass pin capacitor. It provides half-supply filtering.

2 SPI BUS INTERFACE

2.1 Pin descriptions

Pin	Functional Description
DATA	This is the serial data input pin.
CLK	This is the clock input pin.
ENB	This is the SPI enable pin active at high level.

2.2 Description of SPI operation

The serial data bits are organized into a field containing 8 bits of data as shown in *Table 1*. The DATA 0 to DATA 2 bits determine the output mode of the TS4851 as shown in *Table 2*. The DATA 3 to DATA 7 bits determine the gain level setting as illustrated by *Table 3*. For each SPI transfer, the data bits are written to the DATA pin with the least significant bit (LSB) first. All serial data are sampled at the rising edge of the CLK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic low to complete the SPI sequence. All 8 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the height rising clock edge has occurred. For any data sequence longer than 8 bits, only the first 8 bits will get loaded into the shift register and the rest of the bits will be disregarded.

Table 1: Bit Allocation

	DATA	MODES
LSB	DATA 0	Mode 1
	DATA 1	Mode 2
	DATA 2	Mode 3
	DATA 3	gain 1
	DATA 4	gain 2
	DATA 5	gain 3
	DATA 6	gain 4
MSB	DATA 7	gain 5

Table 2: Output mode selection: G from -34.5 dB to +12 dB (by steps of 1.5 dB)

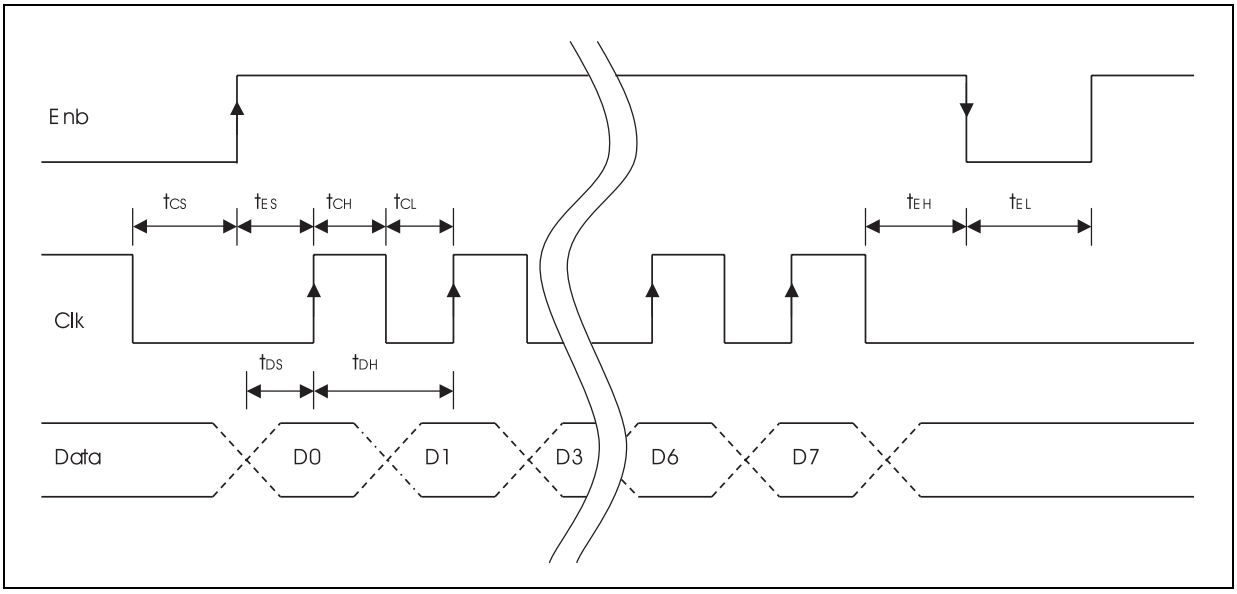
Output Mode #	DATA 2	DATA 1	DATA 0	SPKERout[1]	Rout	Lout
0	0	0	0	SD	SD	SD
1	0	0	1	6dBxP	SD	SD
2	0	1	0	SD	0dBxP	0dBxP
3	0	1	1	Gx(R+L)	SD	SD
4	1	0	0	SD	GxR	GxL
5	1	0	1	Gx(R+L) +6dBxP	SD	SD
6	1	1	0	SD	GxR+0dBxP	GxL+0dBxP
7	1	1	1	6dBxP	GxR+0dBxP	GxL+0dBxP

1) SD = Shutdown Mode, P = Phone in Input, R = Rin input and L = Lin input

Table 3: Volume Control Settings

K : Gain (dB)	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3
-34.5	0	0	0	0	0
-33.0	0	0	0	0	1
-31.5	0	0	0	1	0
-30.0	0	0	0	1	1
-28.5	0	0	1	0	0
-27.0	0	0	1	0	1
-25.5	0	0	1	1	0
-24.0	0	0	1	1	1
-22.5	0	1	0	0	0
-21.0	0	1	0	0	1
-19.5	0	1	0	1	0
-18.0	0	1	0	1	1
-16.5	0	1	1	0	0
-15.0	0	1	1	0	1
-13.5	0	1	1	1	0
-12.0	0	1	1	1	1
-10.5	1	0	0	0	0
-9.0	1	0	0	0	1
-7.5	1	0	0	1	0
-6.0	1	0	0	1	1
-4.5	1	0	1	0	0
-3.0	1	0	1	0	1
-1.5	1	0	1	1	0
0.0	1	0	1	1	1
1.5	1	1	0	0	0
3.0	1	1	0	0	1
4.5	1	1	0	1	0
6	1	1	0	1	1
7.5	1	1	1	0	0
9	1	1	1	0	1
10.5	1	1	1	1	0
12	1	1	1	1	1

2.3 SPI Timing Diagram



3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VCC	Supply voltage[1]	6	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient[2]	200	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model	2	kV
ESD	Machine Model	100	V
	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C

1) All voltages values are measured with respect to the ground pin.

2) Device is protected in case of over temperature by a thermal shutdown active @ 150°C

4 OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	3 to 5.5	V
V_{phin}	Maximum Phone In Input Voltage	G_{ND} to V_{CC}	V
VRin/VLin	Maximum Rin & Lin Input Voltage	G_{ND} to V_{CC}	V
TSD	Thermal Shut Down Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient[1]	90	°C/W

1) Device is protected in case of over temperature by a thermal shutdown active @ 150°C

5 ELECTRICAL CHARACTERISTICS

Table 4: Electrical characteristics at VCC = +5 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current Output Mode 7, Vin = 0 V, no load All other output modes, Vin = 0 V, no load		 8 4.5	 11 6.5	mA
$I_{STANDBY}$	Standby Current Output Mode 0		 0.1	 2	µA
Voo	Output Offset Voltage (differential) Vin = 0 V		 5	 50	mV
Vil	“Logic low” input Voltage	0		0.4	V
Vih	“Logic high” input Voltage	1.4		5	V
Po	Output Power SPKERout, RL = 8 Ω, THD = 1%, F = 1 kHz Rout & Lout, RL = 32 Ω, THD = 0.5%, F = 1 kHz	 800 80	 1000 120		mW
THD + N	Total Harmonic Distortion + Noise Rout & Lout, Po = 80 mW, F = 1 kHz, RL = 32 Ω SPKERout, Po = 800 mW, F = 1 kHz, RL = 8 Ω Rout & Lout, Po = 50 mW, 20 Hz < F < 20 kHz, RL = 32 Ω SPKERout, Po = 40 mW, 20 Hz < F < 20 kHz, RL = 8 Ω		 0.5 1	 0.5 1	%
SNR	Signal To Noise Ratio (A-Weighted)		90		dB
PSRR[1]	Power Supply Rejection Ratio (Output Mode = 2)[2] Vripple = 200 mV Vpp, F = 217 Hz, Input Floating Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 10 Ω		 61 62		dB
G	Digital Gain Range - Rin & Lin no load	 -34.5		 +12	dB
	Digital gain stepsize		1.5		dB
	Stepsize G ≥ -22.5 dB G < -22.5 dB	 -0.5 -1		 +0.5 +1	dB
	Phone In Gain, no load BTL gain from Phone In to SPKERout BTL gain from Phone In to Rout & Lout		 6 0		dB
Zin	Phone In Input Impedance	15	20	25	kΩ
Zin	Rin & Lin Input Impedance (all gain setting)	37.5	50	62.5	kΩ
tes	Enable Stepup Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

1) All PSRR data limits are guaranted by evaluation desgin test.

2) Dynamic measurements [20 x log(rms(Vout)/rms(Vripple)]. Vripple is the superimposed sinus signal to Vcc @ F = 217 Hz

Table 5: Electrical characteristics at VCC = +3.0V, GND = 0V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current Output Mode 7, Vin = 0 V,no load All other output modes, Vin = 0 V,no load		 7.5 4.5	 10 6.5	mA
$I_{STANDBY}$	Standby Current Output Mode 0		 0.1	 2	µA
Voo	Output Offset Voltage (differential) Vin = 0 V		 5	 50	mV
Vil	“Logic low” input Voltage	0		0.4	V
Vih	“Logic high” input Voltage	1.4		5	V
Po	Output Power SPKERout, RL = 8 Ω, THD = 1%, F = 1 kHz Rout & Lout, RL = 32 Ω, THD = 0.5%, F = 1 kHz	 300 20	 340 30		mW
THD + N	Total Harmonic Distortion + Noise Rout & Lout, Po = 20 mW, F = 1 kHz, RL = 32 Ω SPKERout, Po = 300 mW, F = 1 kHz, RL = 8 Ω Rout & Lout, Po = 15 mW, 20 Hz < F < 20 kHz, RL = 32 Ω SPKERout, Po = 250 mW, 20 Hz < F < 20 kHz, RL = 8 Ω		 0.5 1	 0.5 1	%
SNR	Signal To Noise Ratio (A-Weighted)		86		dB
PSRR[1]	Power Supply Rejection Ratio (Output Mode = 2)[2] Vripple = 200 mV Vpp, F = 217 Hz, Input Floating Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 10 Ω		 61 62		dB
G	Digital Gain Range - Rin & Lin no load	 -34.5	 -	 +12	dB
	Digital gain stepsize		1.5		dB
	Stepsize error G ≥ -22.5 dB G < -22.5 dB	 -0.5 -1		 +0.5 +1	dB
	Phone In Gain, no load BTL gain from Phone In to SPKERout BTL gain from Phone In to Rout & Lout		 6 0		dB
Zin	Phone In Input Impedance [1]	15	20	25	kΩ
Zin	Rin & Lin Input Impedance (All Gain Setting) [1]	37.5	50	62.5	kΩ
tes	Enable Stepup Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

1) All PSRR data limits are guaranted by evaluation desgin test.

2) Dynamic measurements [20 x log(rms(Vout)/rms(Vripple)]. Vripple is the superimposed sinus signal to Vcc @ F = 217 Hz.

Index of Graphics

Note: In the graphs that follow, the abbreviations Spkout = Speaker Output, and HDout = Headphone Output are used.
All measurements made with Cin = 220 nF, Cb = Cs = 1 µF except in PSRR condition where Cs = 0.

Figure 1: Spkout THD+N vs. output power (output modes 1, 7)

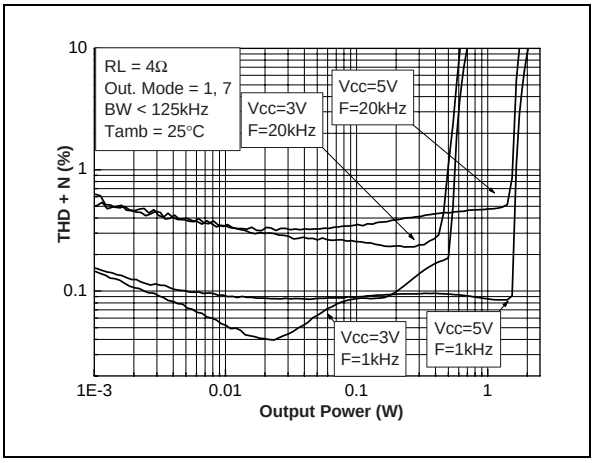


Figure 2: Spkout THD+N vs. output power (output modes 1, 7)

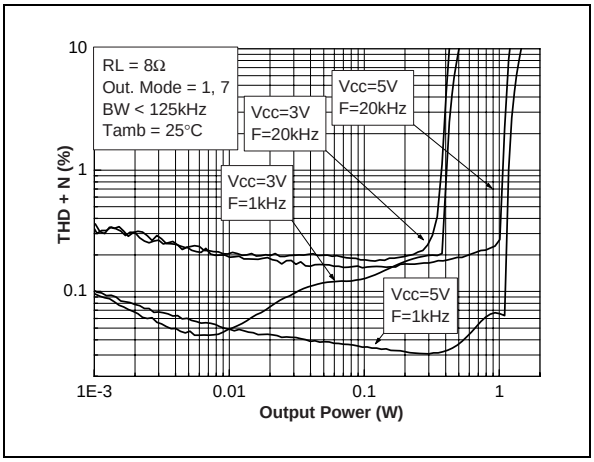


Figure 3: Spkout THD+N vs. output power (output modes 1, 7)

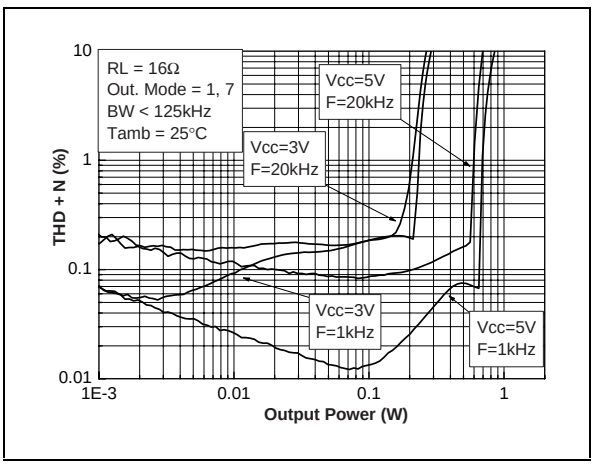


Figure 4: HDout THD+N vs. output power (output mode 2)

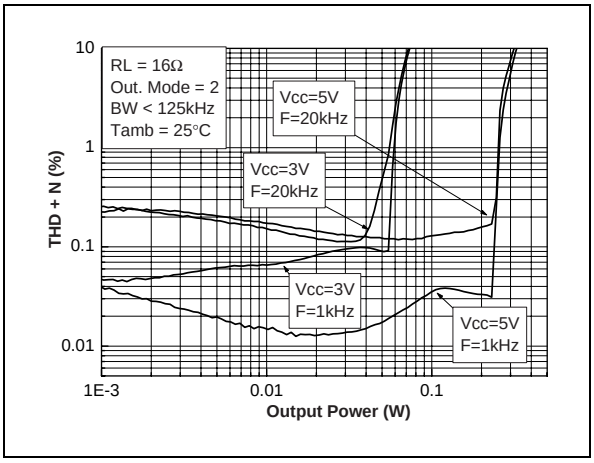


Figure 5: HDout THD+N vs. output power (output mode 2)

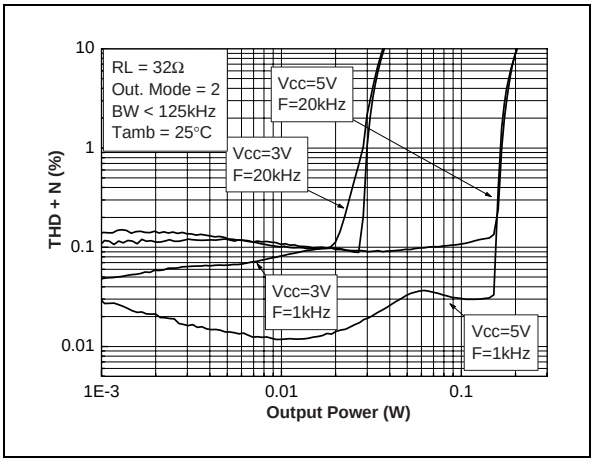


Figure 6: Spkout THD+N vs. output power (output mode 3, G=+12dB)

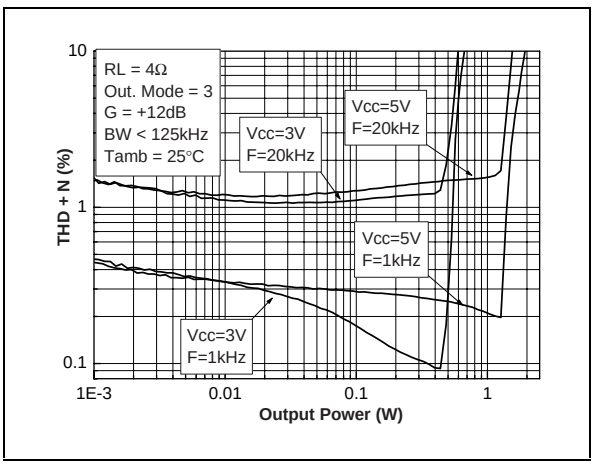


Figure 7: Spkout THD+N vs. output power (output mode 3, G=+12dB)

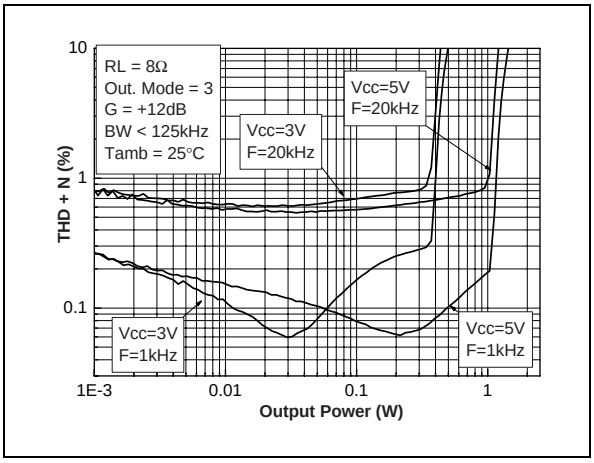


Figure 8: Spkout THD+N vs. output power (output mode 3, G=+12dB)

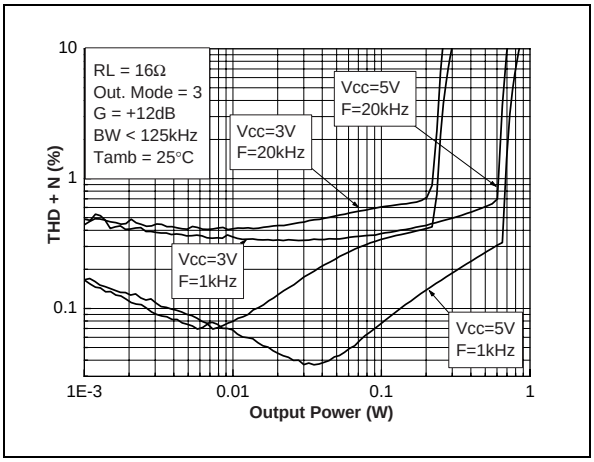


Figure 9: HDout THD+N vs. output power (output mode 4, G=+12dB)

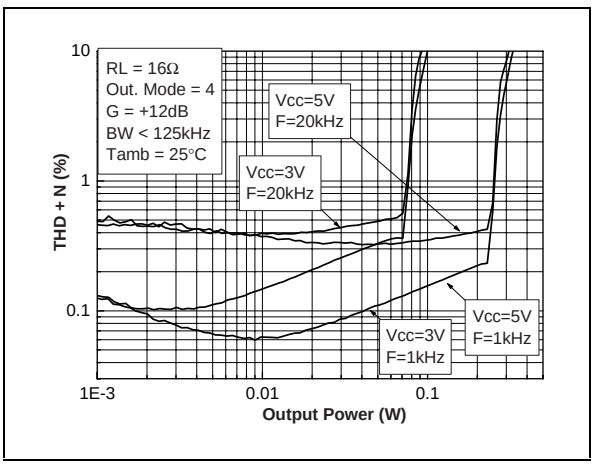


Figure 10: HDout THD+N vs. output power (output mode 4, G=+12dB)

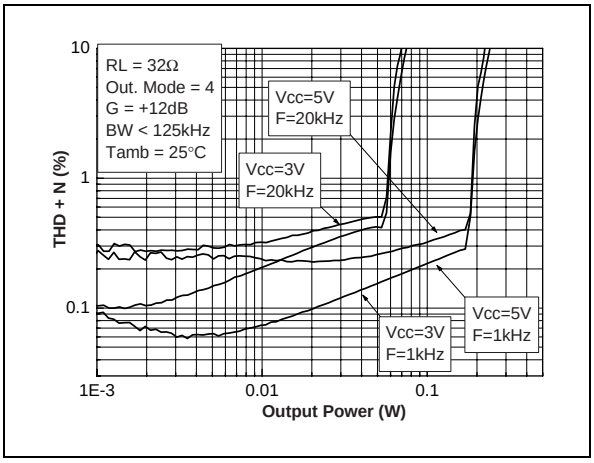


Figure 11: Spkout THD+N vs. frequency (output modes 1, 7)

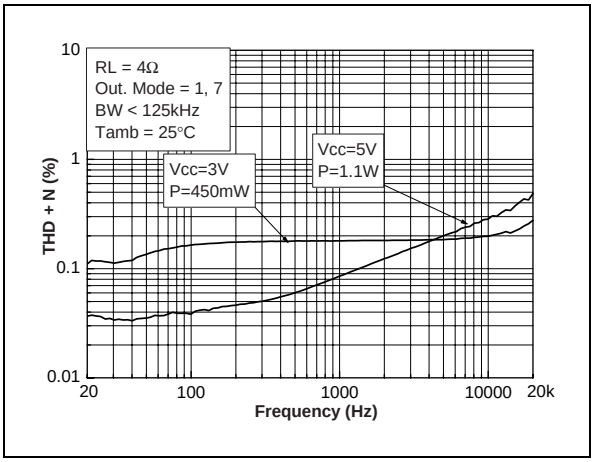


Figure 12: Spkout THD+N vs. frequency (output modes 1, 7)

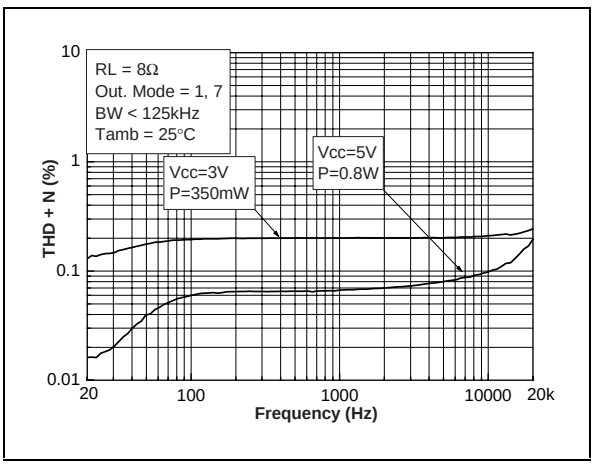


Figure 13: Spkout THD+N vs. frequency (output modes 1, 7)

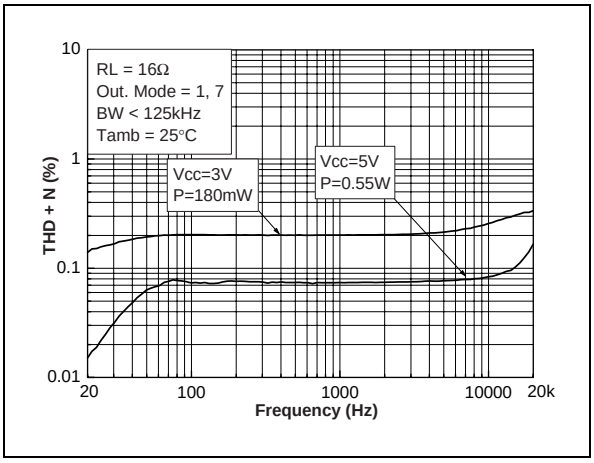


Figure 14: HDout THD+N vs. frequency (output mode 2)

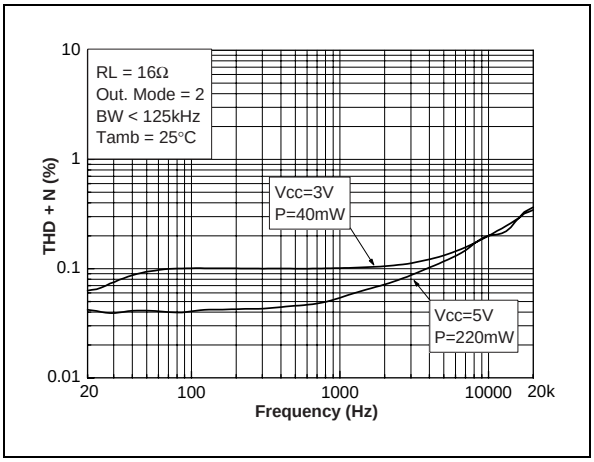


Figure 15: HDout THD+N vs. frequency (output mode 2)

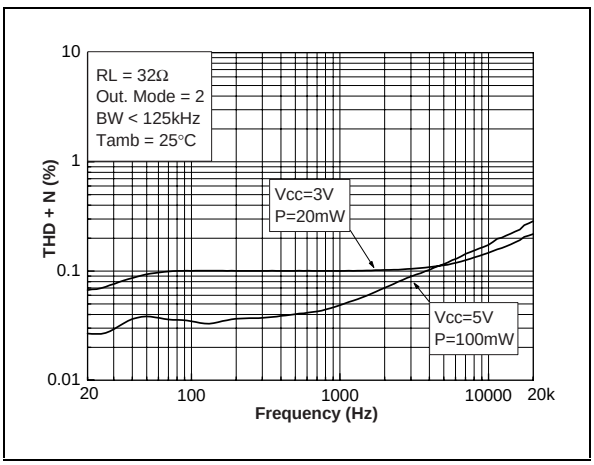


Figure 16: Spkout THD+N vs.frequency (output mode 3, G = +12 dB)

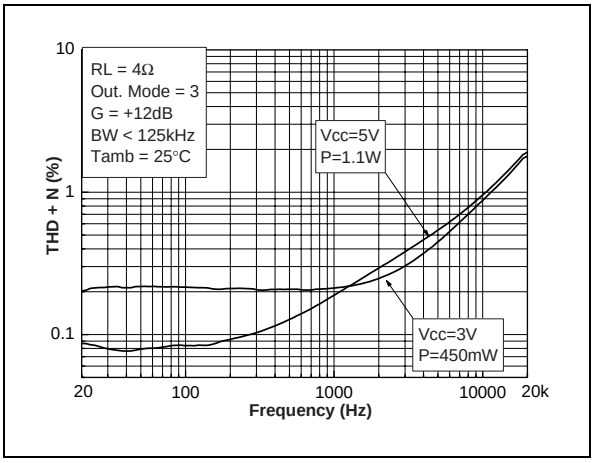


Figure 17: Spkout THD+N vs. frequency (output mode 3, G = +12 dB)

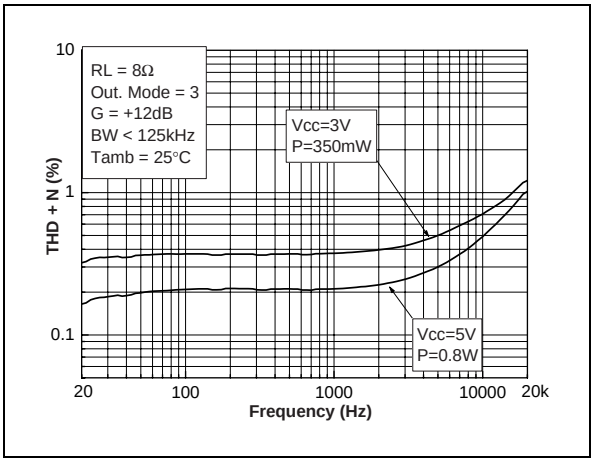


Figure 18: Spkout THD+N vs. frequency (output mode 3, G = +12 dB)

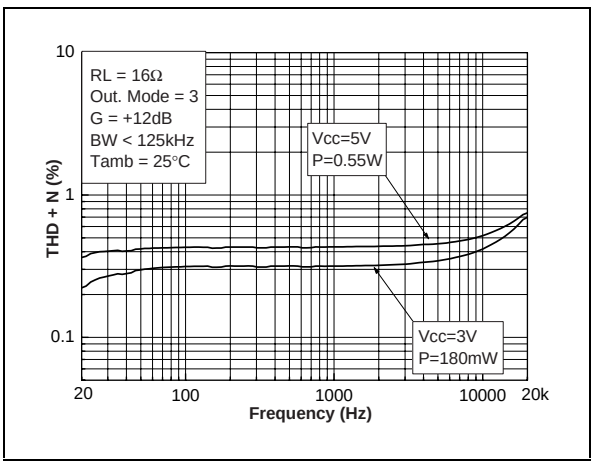


Figure 19: HDout THD+N vs. frequency (output mode 4, G = +12 dB)

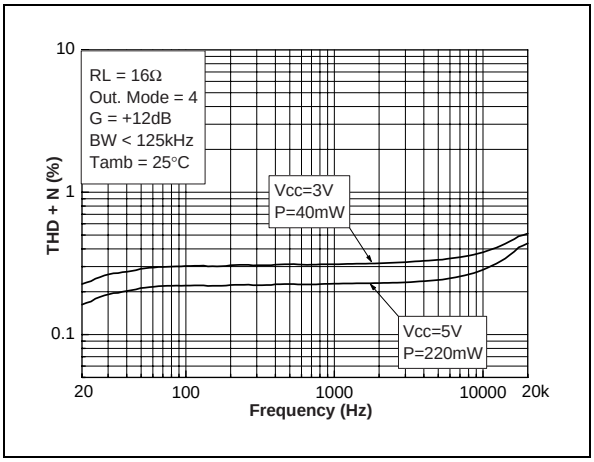


Figure 20: HDout THD+N vs. frequency (output mode 4, G = +12 dB)

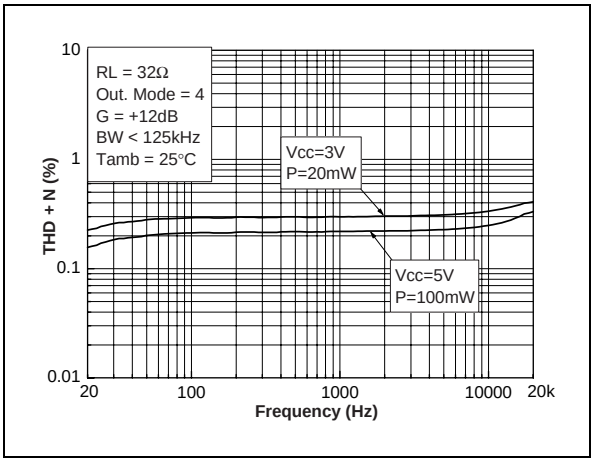


Figure 21: Speaker output power vs. power supply voltage (output mode 1, 7)

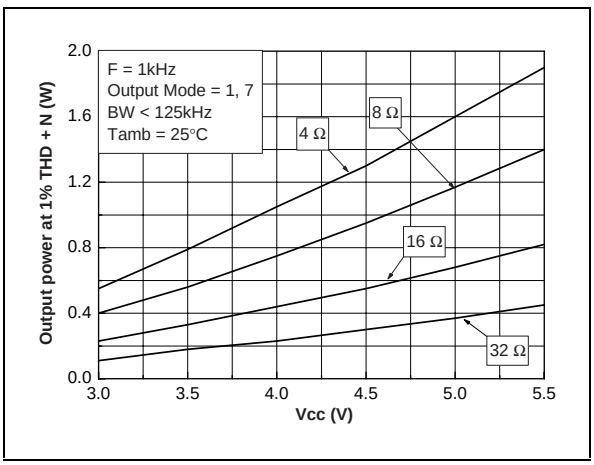


Figure 22: Speaker output power vs. power supply voltage (output mode 1, 7)

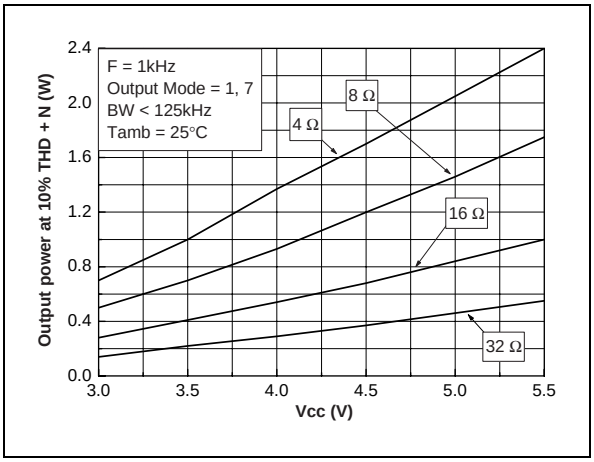


Figure 23: Headphone output power vs. load resistor (output mode 2)

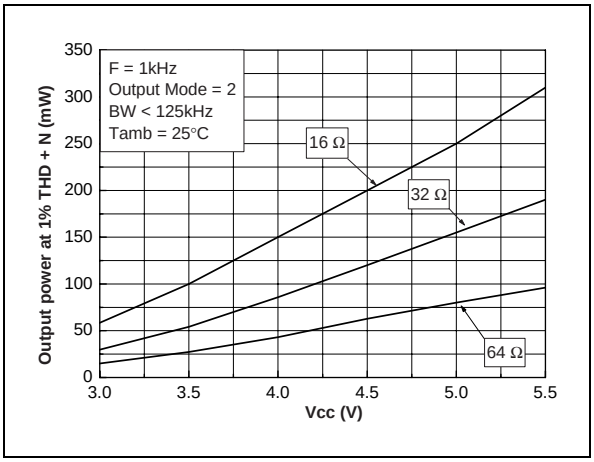


Figure 24: Headphone output power vs. load resistor (output mode 2)

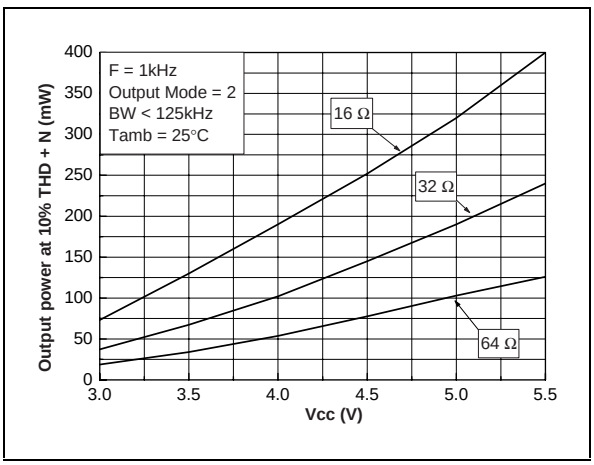


Figure 25: Speaker output power vs. power supply voltage (output mode 3)

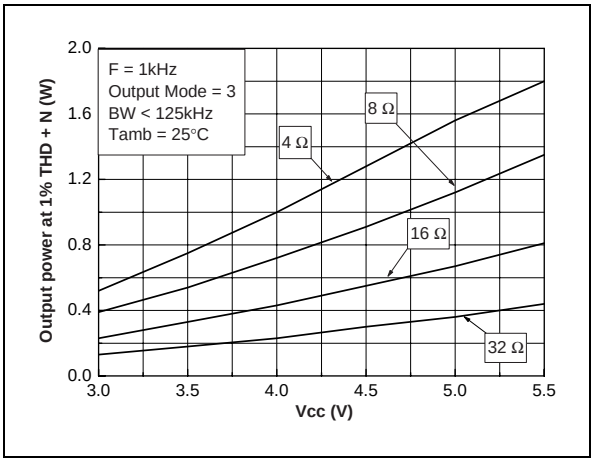


Figure 26: Speaker output power vs. power supply voltage (output mode 3)

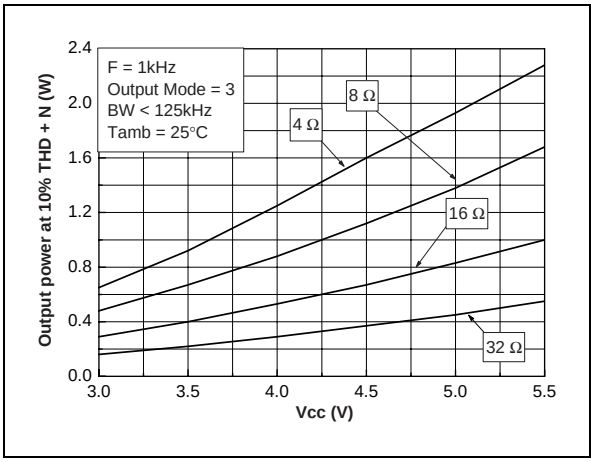


Figure 27: Headphone output power vs. load resistor (output mode 4)

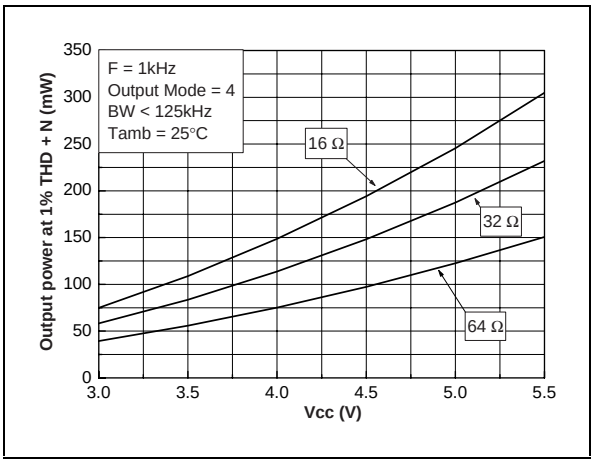


Figure 28: Headphone output power vs. load resistance (output mode 2)

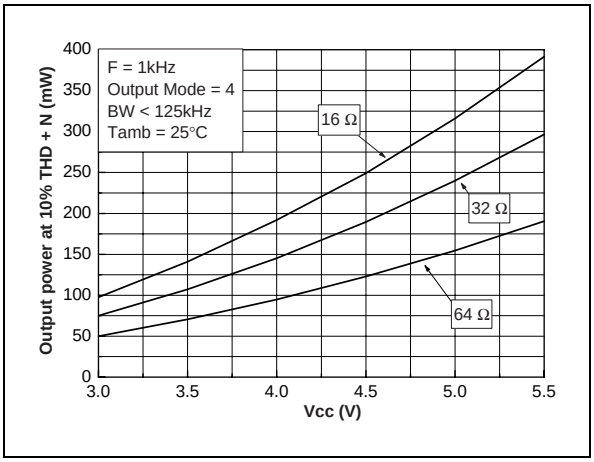


Figure 29: Spkout PSRR vs. frequency (output modes 1, 7, input grounded)

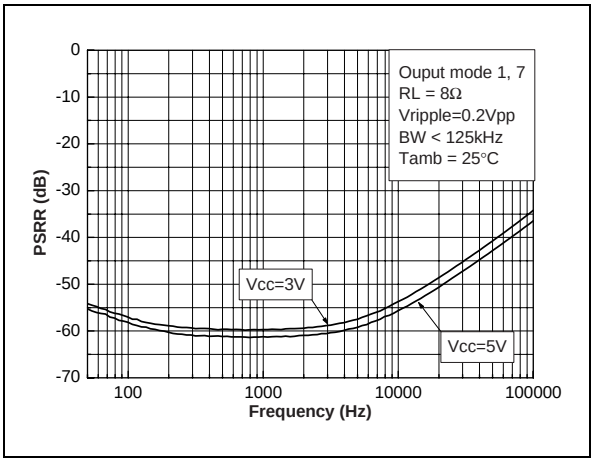


Figure 30: HDout PSRR vs. frequency (output mode 2, input grounded)

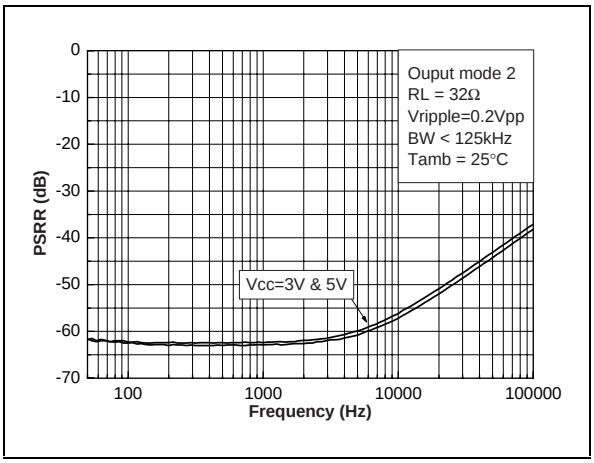


Figure 31: Spkout PSRR vs. frequency (output mode 3, inputs grounded)

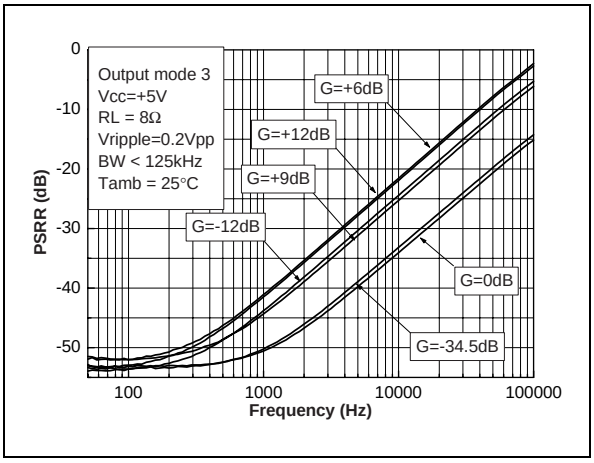


Figure 32: Spkout PSRR vs. frequency (output mode 3, inputs grounded)

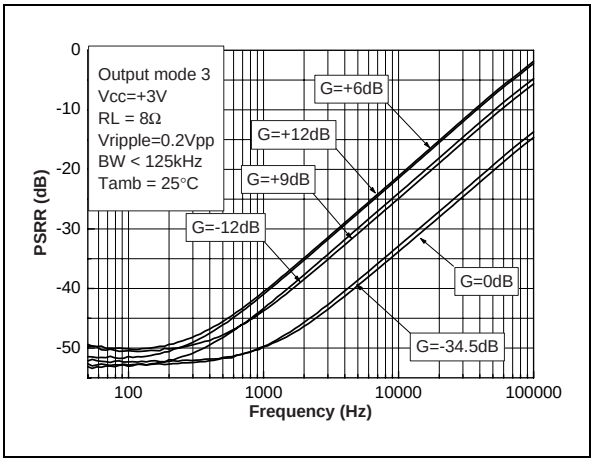


Figure 33: HDout PSRR vs. frequency (output mode 4, inputs grounded)

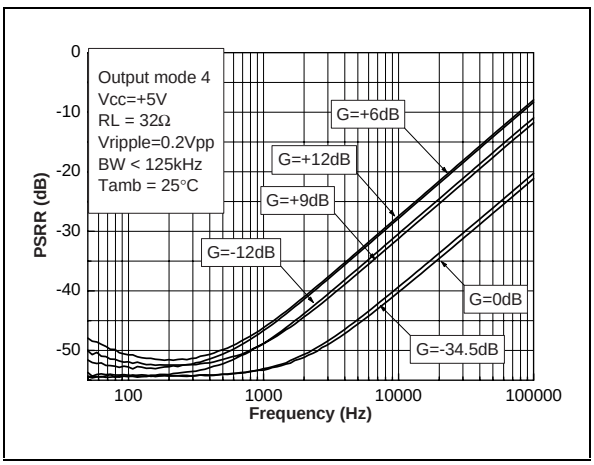


Figure 34: HDout PSRR vs. frequency (output mode 4, inputs grounded)

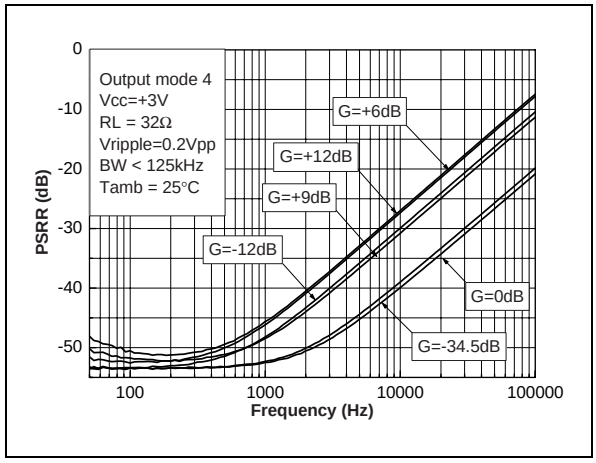


Figure 35: Spkout PSRR vs. frequency (output mode 5, inputs grounded)

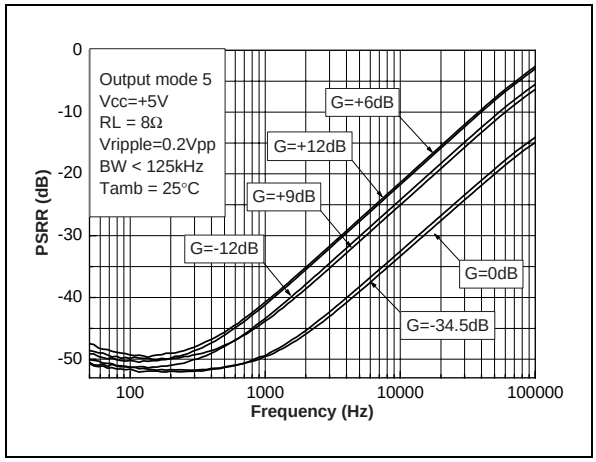


Figure 36: Spkout PSRR vs. frequency (output mode 5, inputs grounded)

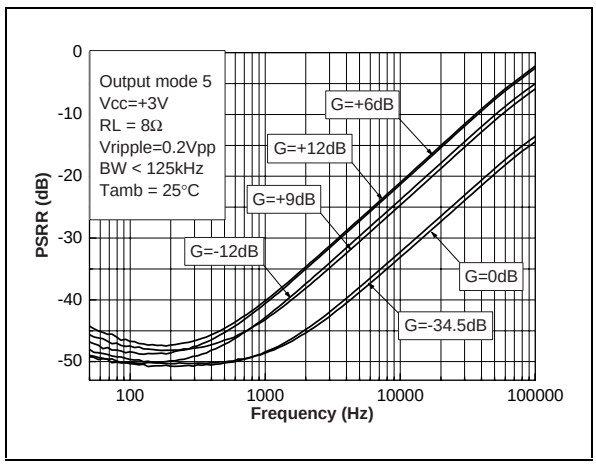


Figure 37: HDout PSRR vs. frequency (output modes 6, 7, inputs grounded)

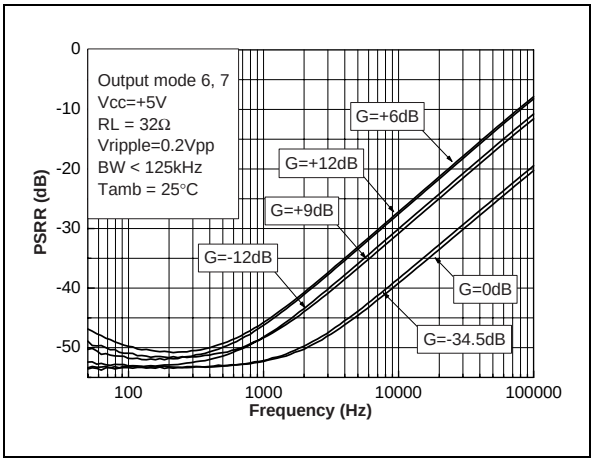


Figure 38: HDout PSRR vs. freq., (output modes 6, 7, inputs grounded)

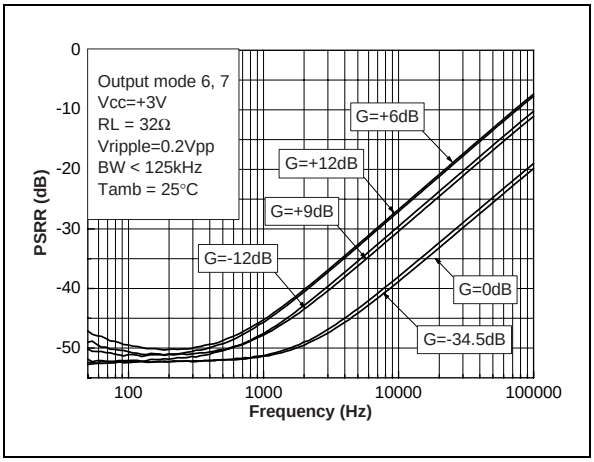


Figure 39: Spkout frequency response (output mode 1, 7)

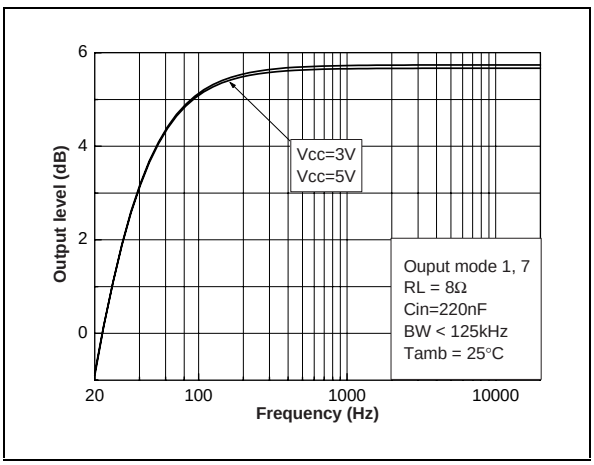


Figure 40: HDout frequency response (output mode 2)

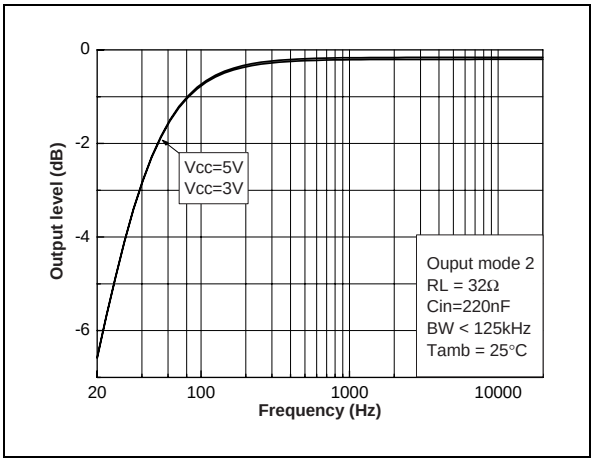


Figure 41: Spkout frequency response (output mode 3)

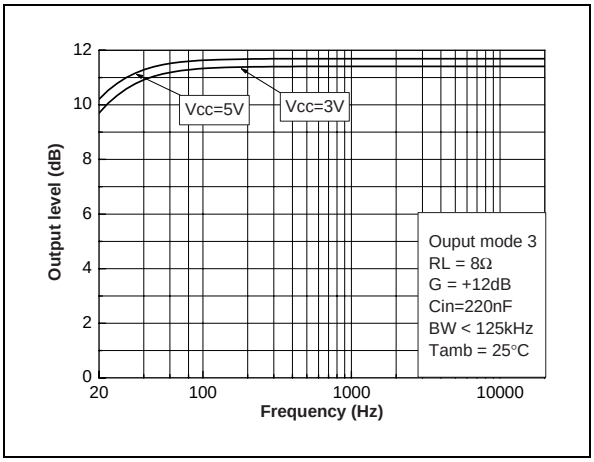


Figure 42: HDout frequency response (output mode 4)

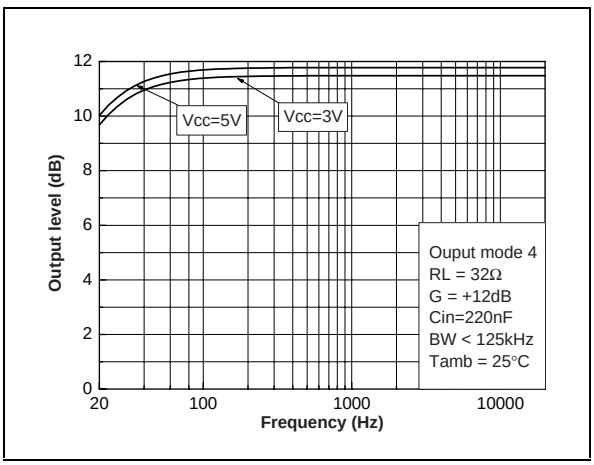


Figure 43: Spkout SNR vs. power supply voltage, unweighted filter, BW = 20 Hz to 20 kHz

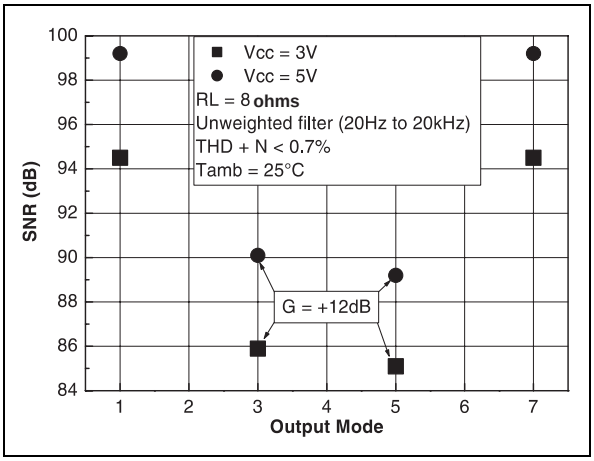


Figure 44: Spkout SNR vs. power supply voltage, weighted filter A, BW = 20 Hz to 20 kHz

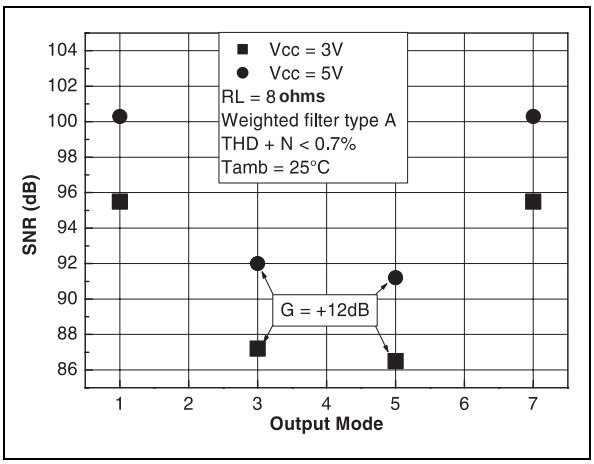


Figure 45: HDout SNR vs. power supply voltage, unweighted filter, BW = 20 Hz to 20 kHz

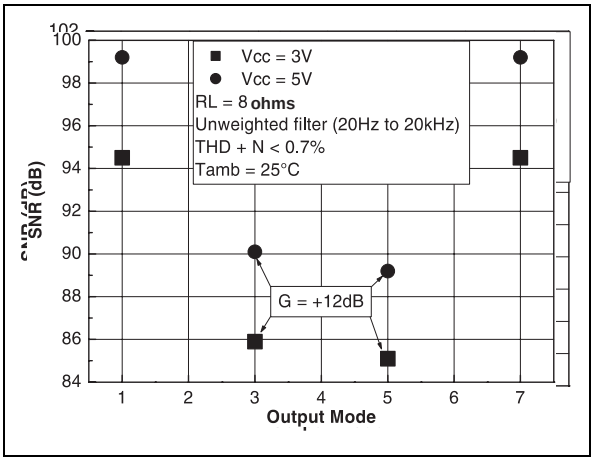


Figure 46: HDout SNR vs. power supply voltage, weighted filter A, BW = 20 Hz to 20 kHz

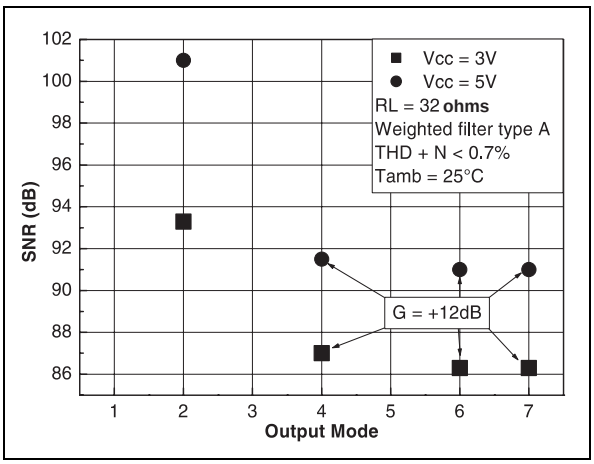


Figure 47: Crosstalk vs. frequency (output mode 4)

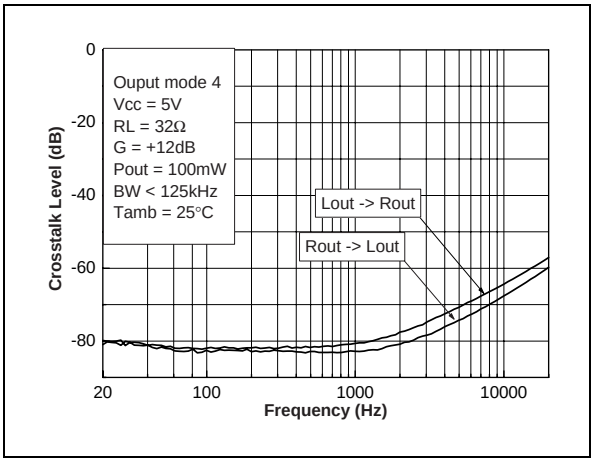


Figure 48: Crosstalk vs. frequency (output mode 4)

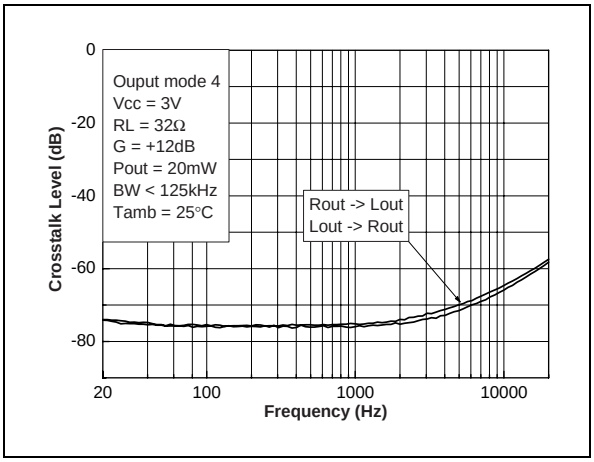


Figure 49: -3 dB lower cut off frequency vs. input capacitor

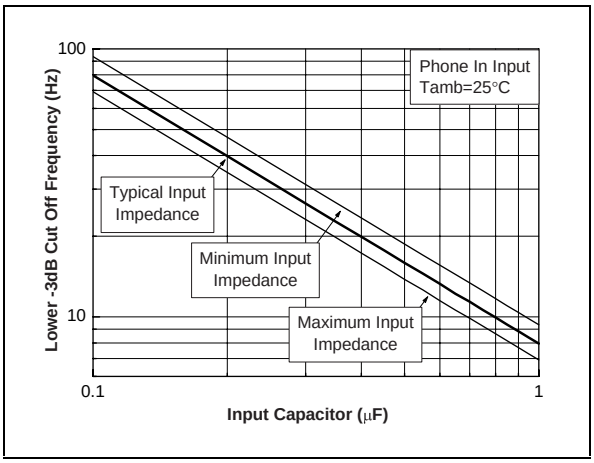


Figure 50: -3 dB lower cut off frequency vs. input capacitance

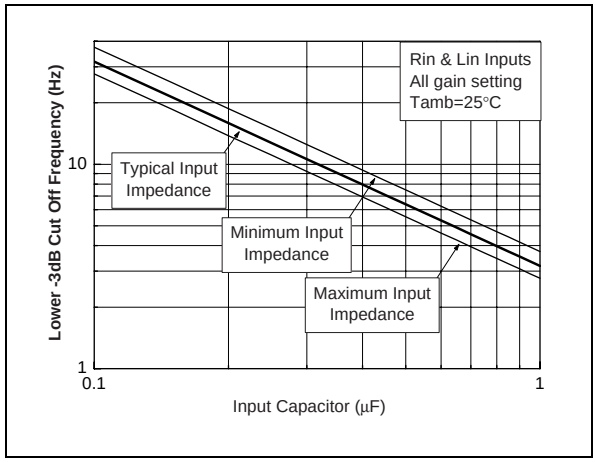


Figure 51: Current consumption vs. power supply voltage

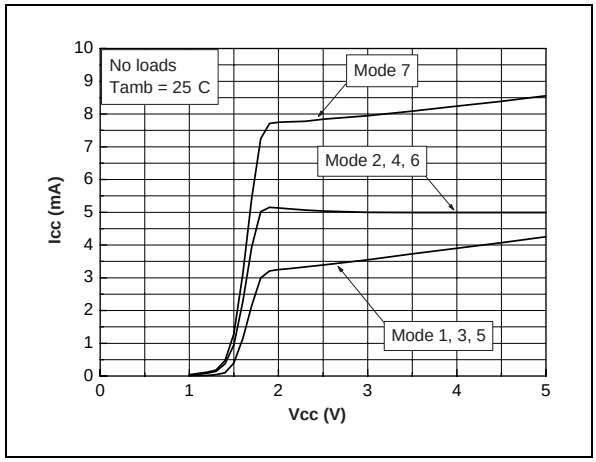


Figure 52: Power dissipation vs. output power (speaker output)

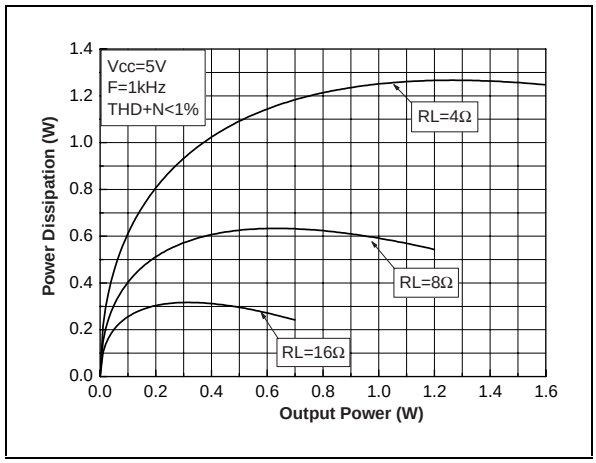


Figure 53: Power dissipation vs. output power (speaker output)

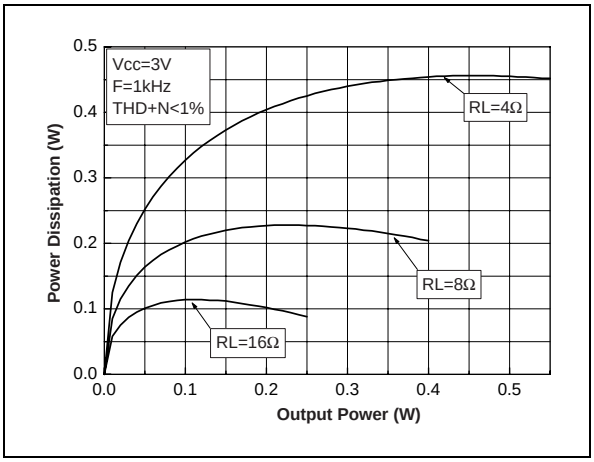


Figure 54: Power dissipation vs. output power (headphone output, one channel)

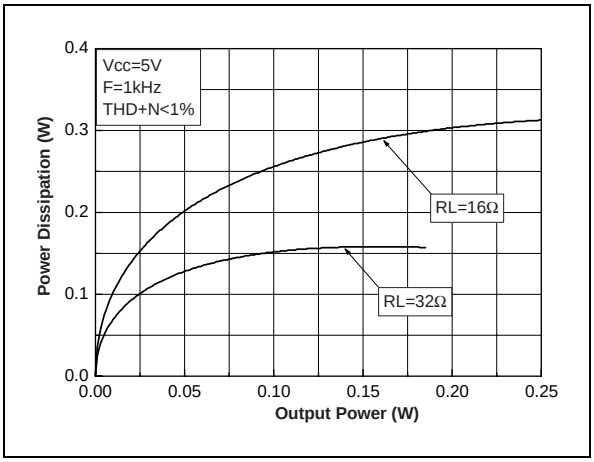


Figure 55: Power dissipation vs. output power (headphone output one channel)

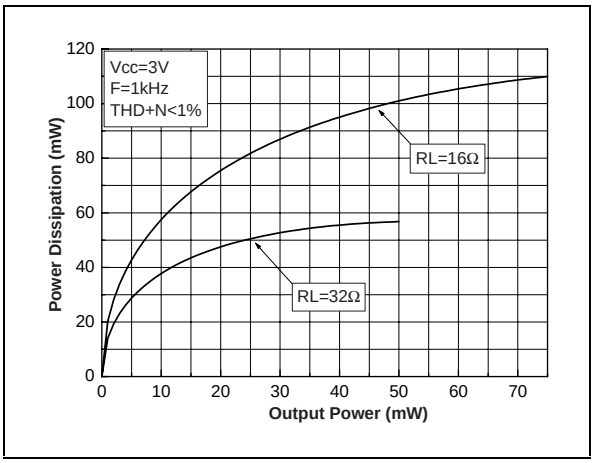


Figure 56: Power derating curves

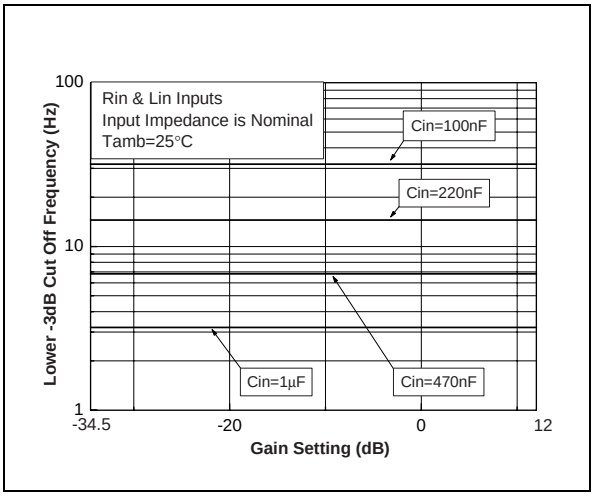


Figure 57: -3 dB lower cut off frequency vs. gain setting (output modes 3, 4, 5, 6, 7)

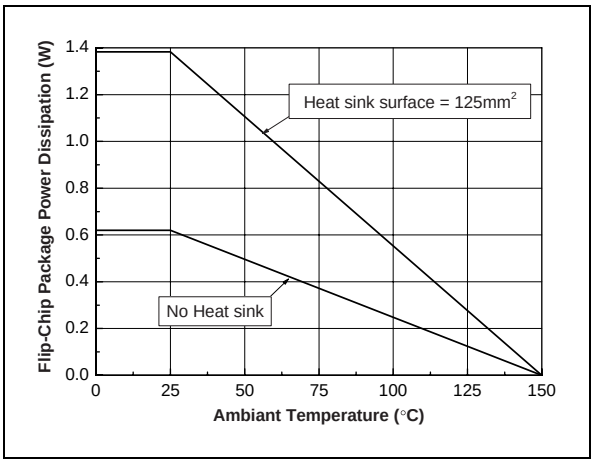


Table 6: Output noise (all inputs grounded)

Output Mode	Unweighted Filter from 3V to 5V	Weighted Filter (A) from 3V to 5V
1	23µVrms	20µVrms
2	20µVrms	17µVrms
3	70vVrms	60µVrms
4	53µVrms	45µVrms
5	79µVrms	67µVrms
6	60µVrms	51vVrms

6 APPLICATION INFORMATION

6.1 BTL configuration principles

The TS4851 integrates 3 monolithic power amplifier having BTL output. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)

Single ended output 2 = Vout2 = -Vout (V)

and

Vout1 - Vout2 = 2Vout (V)

The output power is:

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

6.2 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal (Vout and Iout).
- Supply voltage is a pure DC source (Vcc).

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin\omega t \ (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC\ AVG} = 2\frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is:

$$Psupply = Vcc\ Icc_{AVG} (W)$$

Then, the **power dissipated by each amplifier** is Pdiss = Psupply - Pout (W)

$$P_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Note: This maximum value is depends only on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{Psupply} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so:

$$\frac{\pi}{4} = 78.5\%$$

The TS4851 has three independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{diss\ speaker}$ = Power dissipation due to the speaker power amplifier.
- $P_{diss\ head}$ = Power dissipation due to the Headphone power amplifier
- Total P_{diss} = $P_{diss\ speaker}$ + $P_{diss\ head1}$ + $P_{diss\ head2}$ (W)

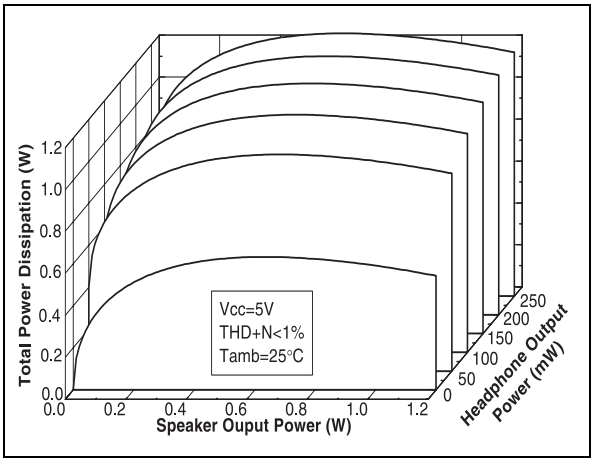
In most cases, $P_{diss\ head1} = P_{diss\ head2}$, giving:

Total $P_{diss} = P_{diss\ speaker} + 2P_{diss\ head}$ (W)

$$TotalP_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi}\left[\sqrt{\frac{P_{OUT\ SPEAKER}}{R_{L\ SPEAKER}}} + 2\sqrt{\frac{P_{OUT\ HEAD}}{R_{L\ HEAD}}}\right] - \left[P_{OUT\ SPEAKER} + 2P_{OUT\ HEAD}\right] \quad (W)$$

The following graph (*Figure 58*) shows an example of the previous formula, with Vcc set to +5 V, $R_{load\ speaker}$ set to 8 Ω and $R_{load\ headphone}$ set to 16 Ω.

Figure 58: Example of Total Power Dissipation vs. Speaker and Headphone Output Power



6.3 Low frequency response

In low frequency region, the effect of Cin starts. Cin with Zin forms a high pass filter with a -3 dB cut off frequency.

$$F_{CL} = \frac{1}{2\,\pi\,Zin\,Cin}(Hz)$$

Zin is the input impedance of the corresponding input:

- 20 kΩ for Phone In IHF input
- 50 kΩ for the 3 other inputs

Note: For all inputs, the impedance value remains constant for all gain settings. This means that the lower cut-off frequency doesn't change with gain setting. Note also that 20 kΩ and 50 kΩ are typical values and there are tolerances around these values (see Electrical Characteristics on page 7).

In *Figures 39* to *41*, you could easily establish the Cin value for a -3 dB cut-off frequency required.

6.4 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4851, a power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has especially an influence on the THD+N in high frequency (above 7 kHz) and indirectly on the power supply disturbances.

With 1 µF, you could expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 1 µF, THD+N increases in high frequency and disturbances on the power supply rail are less filtered.

To the contrary, if Cs is higher than 1 µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its value is critical on the final result of PSRR with input grounded in lower frequency:

- If Cb is lower than 1 µF, THD+N increases at lower frequencies and the PSRR worsens upwards.
- If Cb is higher than 1 µF, the benefit on THD+N and PSRR in the lower frequency range is small.

6.5 Startup time

When the TS4851 is controlled to switch from the full standby mode (output mode 0) to another output mode, a delay is necessary to stabilize the DC bias. This delay depends on the Cb value and can be calculated by the following formulas.

Typical startup time = 0.0175 x Cb (s)

Max. startup time = 0.025 x Cb (s)

(Cb is in µF in these formulas)

These formulas assume that the Cb voltage is equal to 0 V. If the Cb voltage is not equal to 0V, the startup time will be always lower.
The startup time is the delay between the negative edge of Enable input (see *Description of SPI operation* on page 3) and the power ON of the output amplifiers.

Note: When the TS4851 is set in full standby mode, Cb is discharged through an internal resistor. The time to reach 0 V of Cb voltage could be calculated by the following formula:

Tdischarge = 3 x Cb (s)

Note: Cb must be in µF in this formula.

6.6 Pop and Click performance

The TS4851 has internal Pop and Click reduction circuitry. The performance of this circuitry is closely linked with the value of the input capacitor Cin and the bias voltage bypass capacitor Cb.

The value of Cin is due to the lower cut-off frequency value requested. The value of Cb is due to THD+N and PSRR requested always in lower frequency.

The TS4851 is optimized to have a low pop and click in the typical schematic configuration (see *page 2*).

Note: The value of Cs is not an important consideration as regards pop and click.

6.7 Notes on PSRR measurement

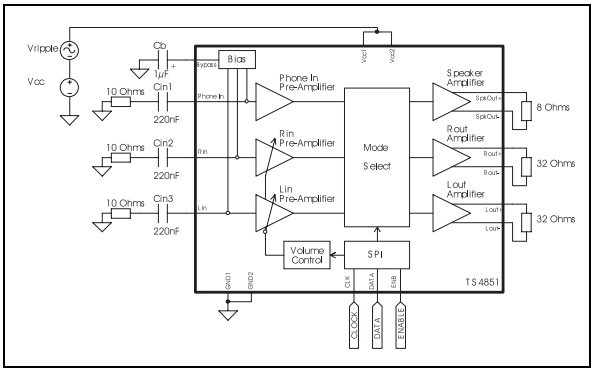
What is the PSRR?

The PSRR is the Power Supply Rejection Ratio. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How we measure the PSRR?

The PSSR was measured according to the schematic shown in *Figure 59*.

Figure 59: PSRR measurement schematic



Principles of operation

- The DC voltage supply (Vcc) is fixed.
- The AC sinusoidal ripple voltage (Vripple) is fixed.
- No bypass capacitor Cs is used.

The PSRR value for each frequency is:

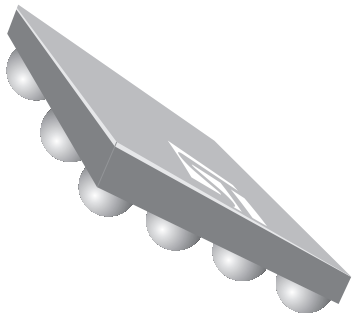
$$PSRR = 20 \times Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right] \quad (dB)$$

*Note: The measure of the Rms voltage is not an Rms selective measure but a full range (20 Hz to 125 kHz) Rms measure. This means that the effective **Rms signal + the Noise** is measured.*

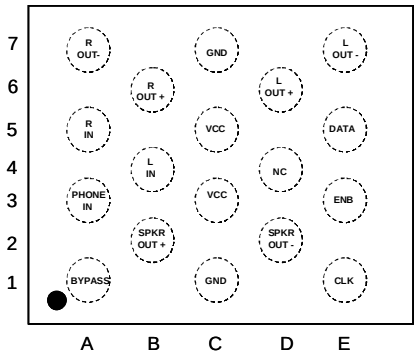
As the measurement is performed with a wide-band frequency range apparatus, we have to subtract **the Noise** part (quadratic operation) of the measurement to obtain the real Rms signal needed to calculate the PSRR, as shown in the formula above.

7 PACKAGE INFORMATION

Flip-chip - 18 bumps: TS4851JT



Pin out (top view)

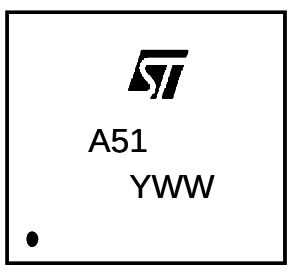


Note: The solder bumps are on the underside.

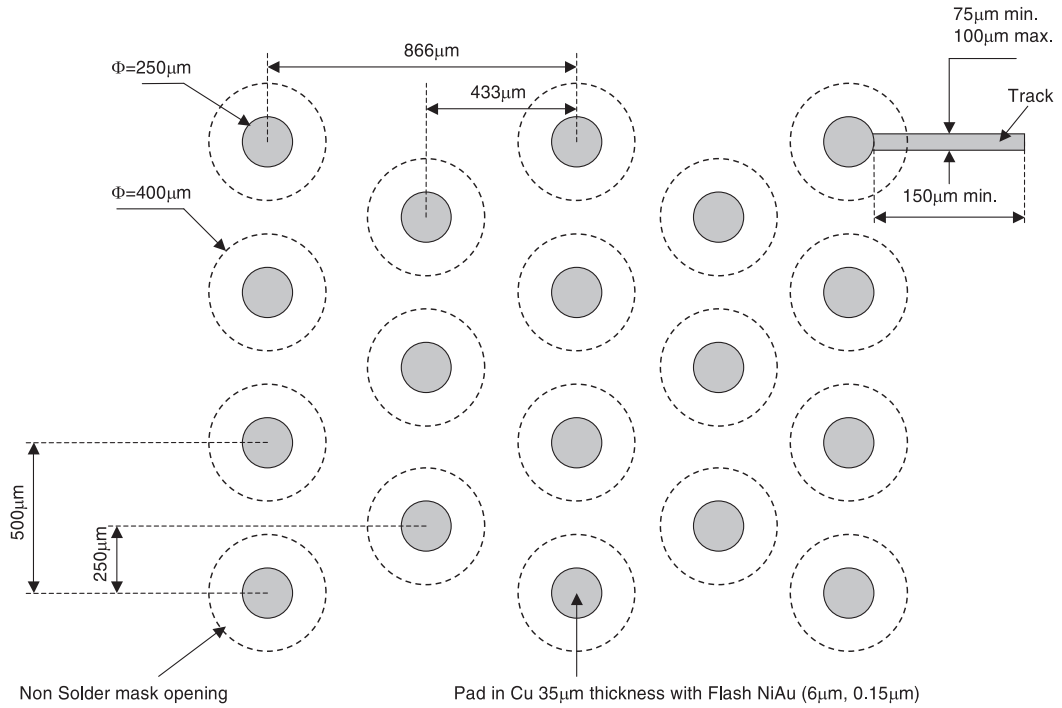
Marking (top view):

The following markings are present on the topside of the flip-chip:

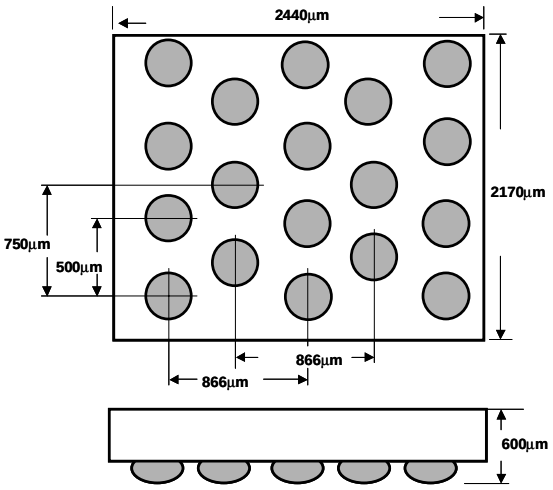
- The ST logo.
- The part number: A51.
- A 3-digit date code: YWW.
- A dot marking the location of Pin1A.



TS4851 Footprint recommendation



Package mechanical data



Die size: ***2170µm x 2440µm ±30µm***

Die height (including bumps): ***600µm ±30µm***

Bumps diameter: 300µm ±15µm

Bumps height: 250µm ±15µm

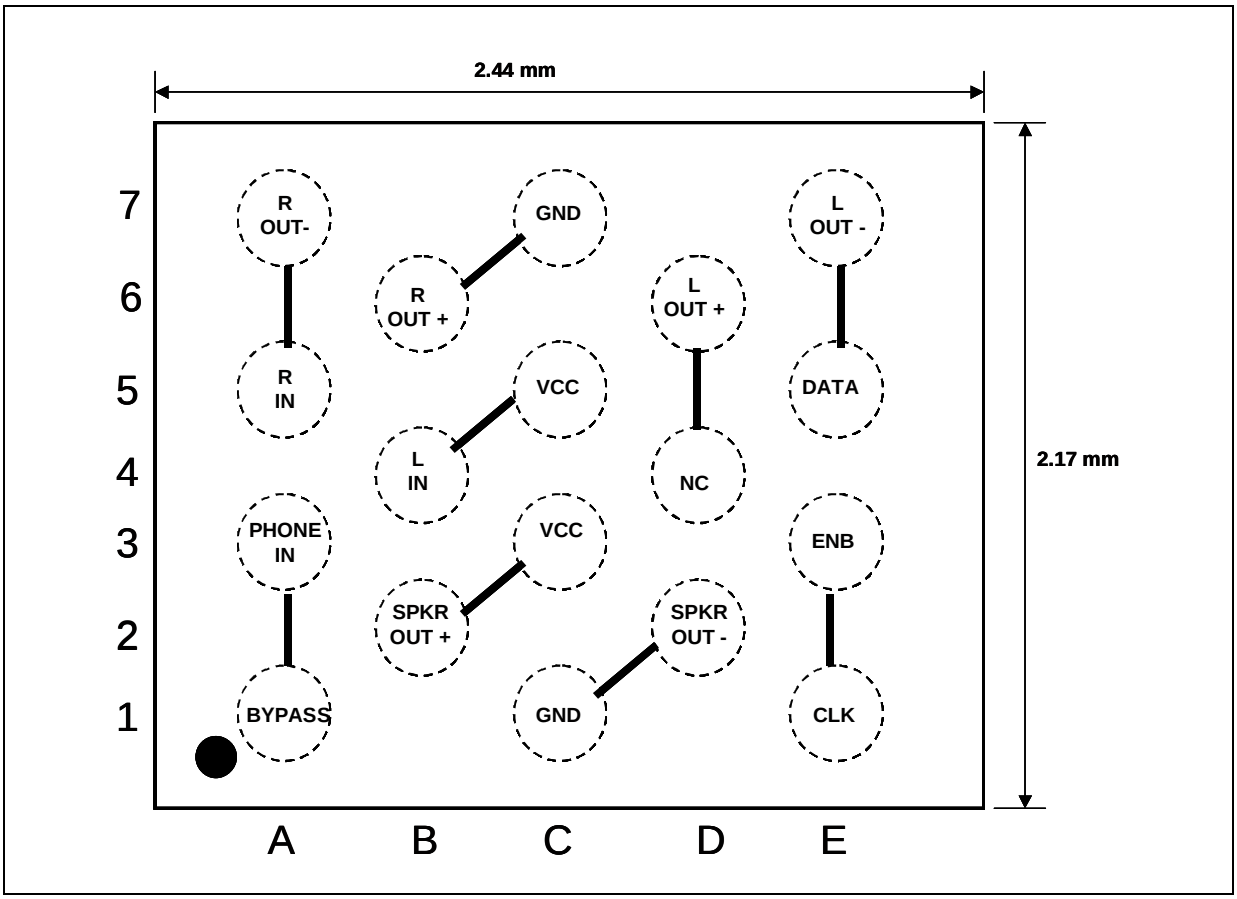
Pitch: 500µm ±10µm

8 DAISY CHAIN SAMPLES

A daisy chain sample is a “dummy” silicon chip that can be used to test your flip-chip soldering process and connection continuity. The daisy chain sample features paired connections between bumps, as shown in the schematic below. On your PCB layout, you should design the bump connections such that they are complementary to the above schema (meaning that different pairs of bumps are connected on the PCB side). In this way, by simply connecting an ohmmeter between pin 1A and pin 5A, you can test the continuity of your soldering process.

The order code for daisy chain samples is given below.

Figure 60: Daisy chain sample mechanical data

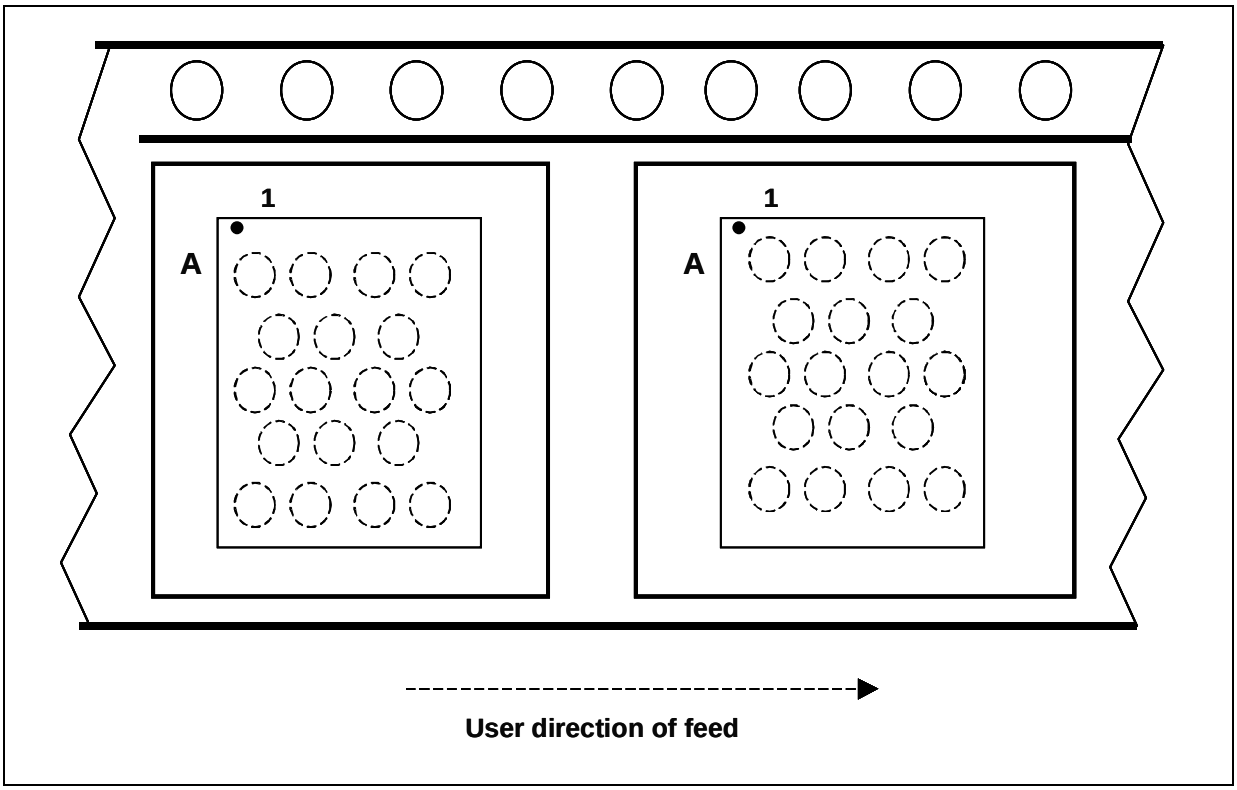


Order code for daisy chain samples

Part Number	Temperature Range	Package	Marking
		J	
TSDC02IJT	-40, +85°C	•	DC2

9 TAPE & REEL SPECIFICATION

Figure 61: Top view of tape and reel



Device orientation

The devices are oriented in the carrier pocket with pin number 1A adjacent to the sprocket holes.

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