

DAB One-Chip Channel- and Source / Data Decoder



Description

The U2739M is an integrated circuit in advanced CMOS technology for demodulation and decoding of a DAB signal according to ETS 300 401. The channel decoder part includes the main features OFDM demodulation and time and frequency synchronization synchronization algorithms on OAK DSP core platform. The audio source decoder supports ISO MPEG 1, 2 layer II half and full sampling rate. The data decoder part is realized on the integrated OAK DSP core and includes 2 packet mode

decoders. Several standard interfaces, like I2C/L3, I2S or RDI are implemented to offer a flexible utilization. The U2739M offers a user-defined implementation of the time and frequency synchronization by down-loading the corresponding software algorithms to the OAK DSP core.

Electrostatic sensitive device.
Observe precautions for handling.



Features

- Support of mode I, II, III and IV according to ETS 300 401
- Time and frequency synchronization with a wide-range parameter set
- Optional implementation of user-defined synchronization strategy by using OAK USE-bootmode
- Flexible software configuration (set 1 – (temic kernel), set 2 – (user extension) concept)
- Automatic mode detection (AMD)
- Generation of receiver status information
- Generation of tuner control signals
- Generation of pulse width modulated VCXO control signal
- Plastic TQFP100 package or plastic LQFP144 respectively ceramic QFP144 package for software development
- Power supply 3.3 V, master clock 24.576 MHz
- Digital AFC (frequency tolerance < 0.5 Hz for mode I)
- Digital AGC with a gain control range of 40 dB
- On-chip de-interleaver memory for full 1.8 Mbit/s decoding data rate
- Time and frequency synchronization on DSP OAK core
- FIC interpreter
- Support of AIC decoding (set 2)
- Support of TII decoding and corresponding RDI insertion (set 2)

Audio Source Decoder

- Audio source decoder ISO MPEG 1, 2 layer II (ISO/IEC 11172/3)
- Half (24 kHz according ISO/IEC 13818-3) and full (48 kHz) sampling rate
- I2S and SPDIF output interfaces
- Programmable fader
- Programmable DRC

Data Decoder

- Support 2 packet mode decoder on OAK DSP core
- FIC on-chip memory, acces via MC interface
- V24/RS232 output

Channel Decoder

- Demodulation and decoding of up to 64 UEP/EEP sub-channels
- Support of dynamic multiplex reconfiguration (DMR) without mute state
- Digital Null-Symbol detection (FSYNCH generation)
- Channel filtering (48 dB)
- Optional SAW filter equilization

Interfaces

- Source decoder output interface: I2S and SPDIF
- Data decoder output interface: V24/RS232
- Channel decoder output interface: RDI and SFCO
- Microcontroller interface: I2C/L3
- RDI
 - Extended high capacity mode
 - IEC 958 format
 - RDI control channel (RCC)
- SFCO simple full capacity output
 - Window-, serial sub-channel identifier (SbChld)-, data-, error- and clock line
 - 3.072 MHz burst mode interface
- 10-bit ADC interface
 - ADC sampling clock generation
 - ADC binary or 2’s complement format selection
 - Support of several intermediate frequencies
- DSP OAK core bootstrap ROM interface
- Voltage controlled reference oscillator (VCXO) interface
- Time deinterleaver SRAM (4 Mbit) interface
- High speed serial output HSSO (PAD, DD1, DD2, CIR) interface, 3-line serial burst mode interface

Block Diagram

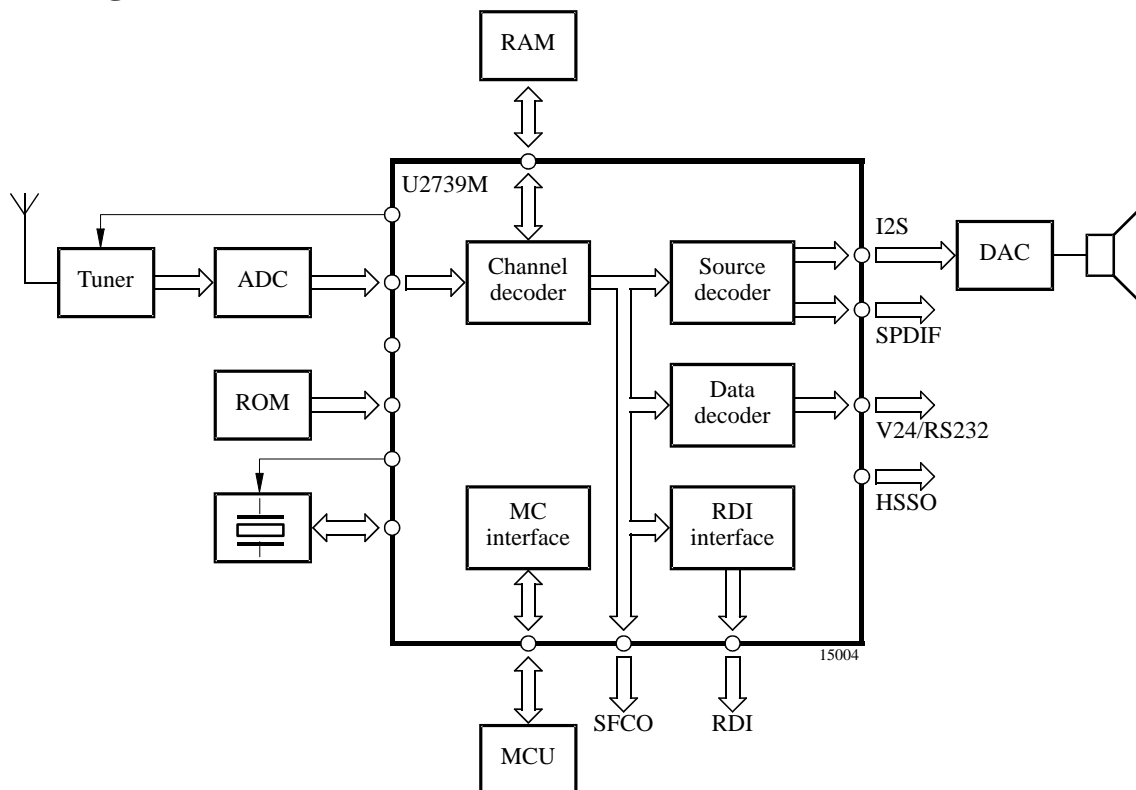


Figure 1. TEMIC DAB receiver concept

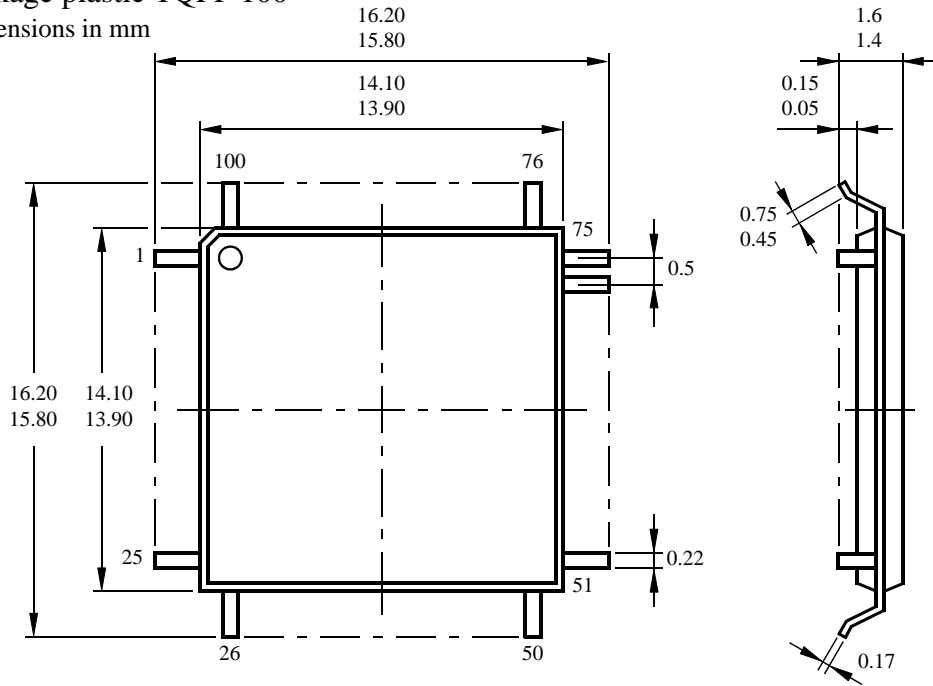
Ordering Information

Extended Type Number	Package	Remarks
U2739M	TQFP100	
U2739M	LQFP144	
U2739M	QFP144	

Package Information

Package plastic TQFP 100

Dimensions in mm



technical drawings
according to DIN
specifications

13051

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