

UC28023
UC28025

SLUS557B – MARCH 2003 – REVISED APRIL 2004

ECONOMY HIGH-SPEED PWM CONTROLLER

FEATURES

- Peak Current Mode, Average Current Mode, or Voltage Mode (with Feed-Forward) Control Methods
- Practical Operation Up to 1 MHz
- 50-ns Propagation Delay to Output
- ±1.5-A Peak Totem Pole Outputs
- 9-V to 30-V Nominal Operational Voltage Range
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Programmable Maximum Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Trimmed 5.1-V Reference with UVLO
- Same Functionality as UC3823 and UC3825

APPLICATIONS

- Off-Line and DC/DC Power Supplies
- Converters Using Voltage Mode, Peak Current Mode, or Average Current Mode Control Methods
- Single-Ended or Two-Switch Topology Designs

DESCRIPTION

The UC28023 and UC28025 are fixed-frequency PWM controllers optimized for high-frequency switched-mode power supply applications. The UC28023 is a single output PWM for single-ended topologies while the UC28025 offers dual alternating outputs for double-ended and full bridge topologies.

Targeted for cost effective solutions with minimal external components, UC2802x include an oscillator, a temperature compensated reference, a wide band width error amplifier, a high-speed current-sense comparator and high-current active-high totem-pole outputs to directly drive external MOSFETs.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start-up current. During undervoltage lockout, the outputs are high impedance. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier.

Devices are available in the industrial temperature range of -40°C to 105°C. Package offerings are 16-pin SOICW (DW), or 16-pin PDIP (N) packages.

ORDERING INFORMATION

| T _A = T _J | OUTPUT CONFIGURATION | EXTERNAL CURRENT LIMIT REFERENCE | PACKAGED DEVICES | |
|---------------------------------|----------------------|----------------------------------|------------------|---------------|
| | | | PDIP-16 (N) | SOICW-16 (DW) |
| -40°C to 105°C | Single | Yes | UC28023N | UC28023DW |
| | Dual Alternating | No | UC28025N | UC28025DW |

(1) The DW package are also available taped and reeled. Add an R suffix to the device type (i.e., UC28023DWR (2,000 devices per reel)).



UC28023 UC28025

SLUS557B – MARCH 2003 – REVISED APRIL 2004



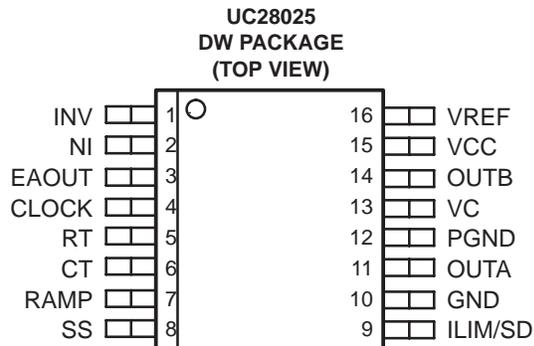
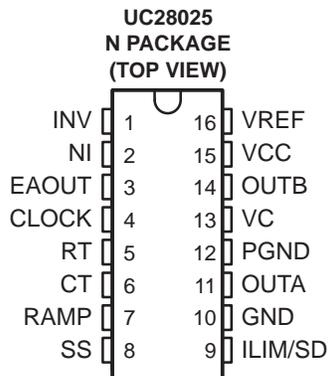
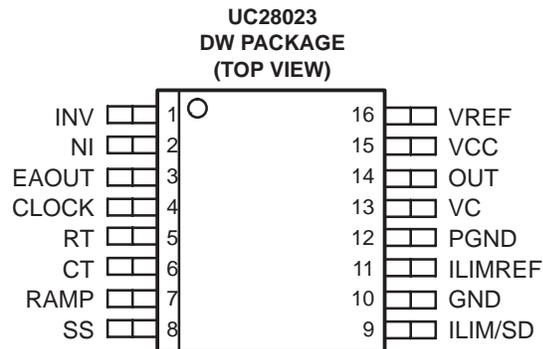
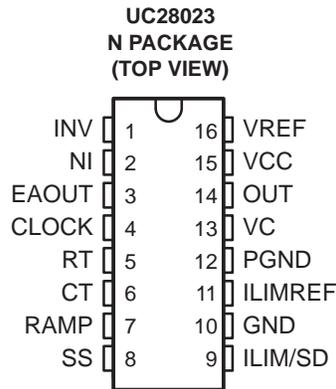
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | UC28023 | UC28025 | RATING | UNIT |
|---|---------------|---------------|---------------|------|
| Input voltage range, | V_C, V_{CC} | V_C, V_{CC} | 30 | V |
| Output current, $I_{OUT(DC)}$ | OUT | OUTA, OUTB | ± 0.5 | A |
| Peak output current, pulsed 0.5 ms $I_{OUT(pulsed)}$ | OUT | OUTA, OUTB | ± 2.0 | A |
| Capacitive load, C_{LOAD} | | | 200 | pF |
| Analog inputs | INV, NI, RAMP | INV, NI, RAM | -0.3 V to 7 V | A |
| | SS, ILIM/SD | SS, ILIM/SD | ± 2.0 | A |
| Output current, I_{REF} | VREF | VREF | 10 | mA |
| Output current, I_{CLOCK} | CLOCK | CLOCK | -5 | |
| Soft-start sink current, I_{SINK_SS} | SS | SS | 5 | |
| Output current, $I_{OUT(EA)}$ | EAOUT | EAOUT | 20 | |
| Oscillator charging current, I_{OSC_CHG} | RT | RT | -5 | |
| Power Dissipation at $T_A = 25^\circ\text{C}$ (all packages) | | | 1 | W |
| Operating junction temperature range, T_J | | | -55 to 150 | °C |
| Storage temperature, T_{stg} | | | -65 to 150 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, T_{sol} | | | 300 | |

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. All currents are positive into and negative out of the specified terminal.



ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 105°C , $T_J = T_A$, $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 15\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|--|------|------|------|------------------------|
| REFERENCE | | | | | | |
| V_{REF} | Reference voltage | $T_J = 25^{\circ}\text{C}$, $I_{REF} = 1\text{ mA}$ | 5.05 | 5.10 | 5.15 | V |
| | Line regulation voltage | $10\text{ V} \leq V_{CC} \leq 30\text{ V}$ | | 2 | 15 | mV |
| | Load regulation voltage | $1\text{ mA} \leq I_{REF} \leq 10\text{ mA}$ | | 5 | 15 | |
| | Temperature stability ⁽¹⁾ | $T_{(\text{min})} < T_A < T_{(\text{max})}$ | | 0.2 | 0.4 | mV/ $^{\circ}\text{C}$ |
| | Total output voltage variation ⁽¹⁾ | Line, load, temperature | 4.95 | | 5.25 | V |
| | Output noise voltage ⁽¹⁾ | $10\text{ Hz} < f < 10\text{ kHz}$ | | 50 | | μV |
| | Long term stability voltage ⁽¹⁾ | $T_J = 125^{\circ}\text{C}$, 1000 hours | | 5 | 25 | mV |
| I_{SS} | Short circuit current | $V_{REF} = 0\text{ V}$ | -20 | -50 | -100 | mA |
| OSCILLATOR | | | | | | |
| f_{OSC} | Initial accuracy ⁽¹⁾ | $T_J = 25^{\circ}\text{C}$ | 360 | 400 | 440 | kHz |
| | Voltage stability ⁽¹⁾ | $10\text{ V} \leq V_{CC} \leq 30\text{ V}$ | | 0.2% | 2.0% | |
| | Temperature stability ⁽¹⁾ | $T_{(\text{min})} < T_A < T_{(\text{max})}$ | | 5% | | kHz |
| | Total voltage variation ⁽¹⁾ | Line, temperature | 340 | | 460 | |
| V_{CLOCK_H} | High-level clock output voltage | | 3.9 | 4.5 | | V |
| V_{CLOCK_L} | Low-level clock output voltage | | | 2.3 | 2.9 | |
| $V_{RAMP(p)}$ | Ramp peak voltage ⁽¹⁾ | | 2.6 | 2.8 | 3.0 | |
| $V_{RAMP(v)}$ | Ramp valley voltage ⁽¹⁾ | | 0.70 | 1.00 | 1.25 | |
| $V_{RAMP(vp)}$ | Ramp valley-to-peak voltage ⁽¹⁾ | | 1.6 | 1.8 | 2.0 | |
| | | | | | | |
| ERROR AMPLIFIER | | | | | | |
| V_{IN} | Input offset voltage | | | | 15 | mV |
| I_{BIAS} | Input bias current | | | 0.6 | 3.0 | |
| I_{IN} | Input offset current | | | 0.1 | 1.0 | μA |
| A_{VOL} | Open loop gain | $1\text{ V} \leq V_{OUT} \leq 4\text{ V}$ | 60 | 95 | | dB |
| CMRR | Common mode rejection ratio | $1.5\text{ V} \leq V_{CM} \leq 5.5\text{ V}$ | 75 | 95 | | |
| PSRR | Power supply rejection ratio | $10\text{ V} \leq V_{CC} \leq 30\text{ V}$ | 85 | 110 | | |
| $I_{OUT(sink)}$ | Output sink current | $V_{(EAOUT)} = 1\text{ V}$ | 1.0 | 2.5 | | mA |
| $I_{OUT(src)}$ | Output source current | $V_{(EAOUT)} = 4\text{ V}$ | -0.5 | -1.3 | | |
| V_{OH} | High-level output voltage | $I_{(EAOUT)} = -0.5\text{ mA}$ | 4.0 | 4.7 | 5.0 | V |
| V_{OL} | Low-level output voltage | $I_{(EAOUT)} = 1\text{ mA}$ | 0 | 0.5 | 1.0 | |
| | Unity gain bandwidth ⁽¹⁾ | | 3.0 | 5.5 | | MHz |
| | Slew rate ⁽¹⁾ | | 6 | 12 | | V/ μs |
| PWM COMPARATOR | | | | | | |
| I_{BIAS} | RAMP bias current | $V_{RAMP} = 0\text{ V}$ | | -1 | -5 | μA |
| Maximum duty cycle | UC28023 | | 80% | 90% | | |
| | UC28025 | (2) | 40% | 45% | | |
| Minimum duty cycle | UC28023 | | | | 0% | |
| | UC28025 | | | | 0% | |
| | EAOUT zero DC threshold | $V_{RAMP} = 0\text{ V}$ | 1.10 | 1.25 | 1.40 | V |
| t_{DELAY} | Delay to output time ⁽¹⁾ | | | 50 | 100 | ns |

(1) Ensured by design. Not production tested.

(2) Tested as 80% minimum for the oscillator which is the equivalent of 40% for UC28025.

UC28023 UC28025

SLUS557B – MARCH 2003 – REVISED APRIL 2004

ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to 105°C , $T_J = T_A$, $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 15\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--------------------------------------|---|------|------|----------|---------------|
| SOFT-START | | | | | | |
| I_{CHG} | Charge current | $V_{SS} = 0.5\text{ V}$ | 3 | 9 | 20 | μA |
| I_{DISCHG} | Discharge current | $V_{SS} = 1.0\text{ V}$ | 1.0 | 7.5 | | mA |
| CURRENT LIMIT/SHUTDOWN | | | | | | |
| I_{LIMIT} | Current limit bias current | $0\text{ V} < V_{(ILIM/SD)} < 4\text{ V}$ | | | ± 10 | μA |
| I_{LIMIT} | Offset voltage | UC28023 | | | 15 | mV |
| I_{LIMREF} | Common mode range ⁽¹⁾ | UC28023 | 1.00 | | 1.25 | V |
| | Current limit threshold voltage | UC28025 | 0.9 | 1.0 | 1.1 | |
| | Shutdown threshold voltage | | 1.25 | 1.40 | 1.55 | |
| t_{DELAY} | Delay to output time ⁽¹⁾ | | | 50 | 80 | ns |
| OUTPUT | | | | | | |
| V_{OL} | Low-level output voltage | $I_{OUT} = 20\text{ mA}$ | | 0.25 | 0.40 | V |
| | | $I_{OUT} = 200\text{ mA}$ | | 1.2 | 2.2 | |
| V_{OH} | High-level output voltage | $I_{OUT} = -20\text{ mA}$ | 13.0 | 13.5 | | |
| | | $I_{OUT} = -200\text{ mA}$ | 12 | 13 | | |
| | Collector leakage | $V_C = 30\text{ V}$ | 100 | 500 | | μA |
| | Rise time / Fall time ⁽¹⁾ | $C_{LOAD} = 1\text{ nF}$ | 30 | 60 | | ns |
| UNDERVOLTAGE LOCKOUT (UVLO) | | | | | | |
| | Start threshold voltage | | 8.8 | 9.2 | 9.6 | V |
| | Hysteresis | | 0.4 | 0.8 | 1.2 | |
| SUPPLY CURRENT | | | | | | |
| | Start-up current | $V_{CC} = 8\text{ V}$ | | 1.1 | 2.0 | mA |
| I_{CC} | Operating current | $V_{INV} = V_{RAMP} = V_{ILIM} = 0\text{ V}$, $V_{INV} = 1\text{ V}$ | | 25 | 35 | |

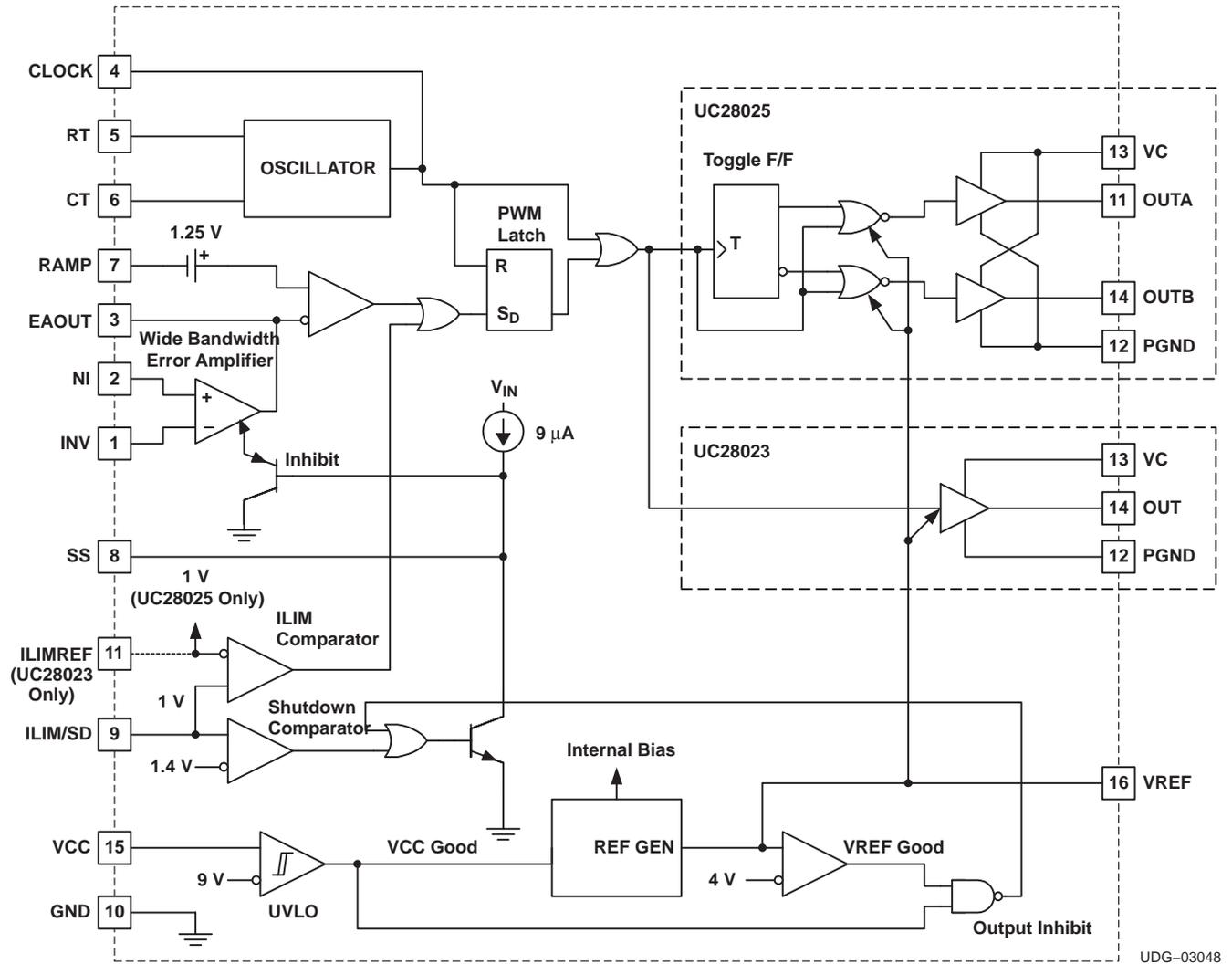
⁽¹⁾ Ensured by design. Not production tested.

THERMAL RESISTANCE

| PACKAGE | θ_{JA} ($^\circ\text{C/W}$) | θ_{JC} ($^\circ\text{C/W}$) |
|-------------------|--------------------------------------|--------------------------------------|
| N ⁽²⁾ | 90 ⁽²⁾ | 45 |
| DW ⁽²⁾ | 50–100 ⁽²⁾ | 27 |

⁽²⁾ Specified θ_{JA} (junction-to-ambient) is for devices mounted to 5-square-inch FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-square-inch aluminum PC board. Test PWB is 0.062 inches thick and typically uses 0.635 mm trace width for power packages and 1.3 mm trace widths for non-power packages with a 100x100 mil probe land area at the end of each trace.

FUNCTIONAL BLOCK DIAGRAM



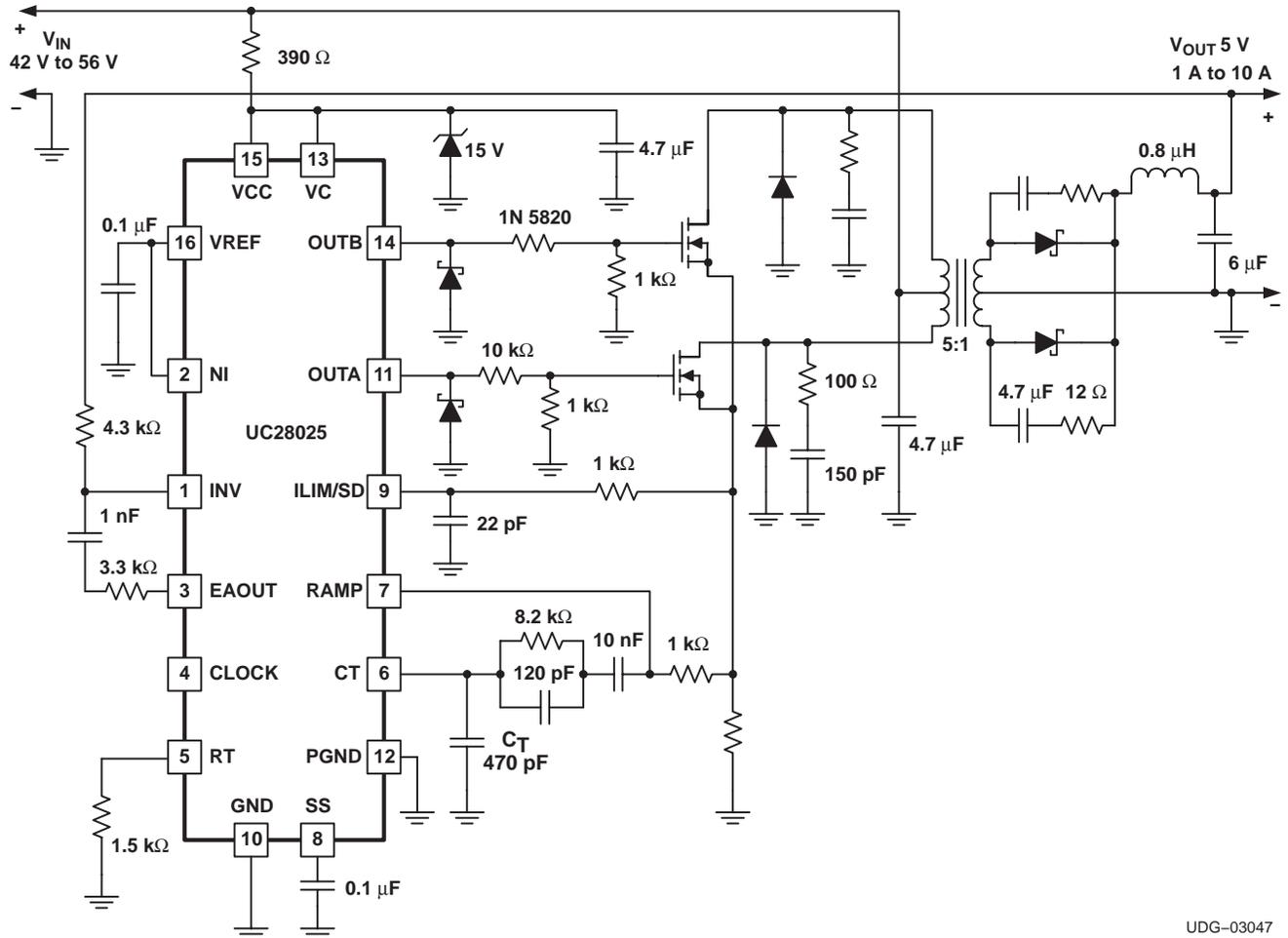
UC28023 UC28025

SLUS557B – MARCH 2003 – REVISED APRIL 2004

TERMINAL FUNCTIONS

| NAME | TERMINAL | | I/O | DESCRIPTION |
|---------|----------|---------|-----|--|
| | UC28023 | UC28025 | | |
| CLOCK | 4 | 4 | O | Output of the internal oscillator |
| CT | 6 | 6 | I | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length. |
| EAOUT | 3 | 3 | O | Output of the error amplifier for compensation |
| GND | 10 | 10 | – | Analog ground return pin. |
| ILIM/SD | 9 | 9 | I | Input to the current limit comparator and the shutdown comparator. |
| ILIMREF | 11 | – | I | Pin to set the current limit threshold externally. |
| INV | 1 | 1 | I | Inverting input to the error amplifier |
| NI | 2 | 2 | I | Non-inverting input to the error amplifier |
| OUT | 14 | – | O | High current totem pole output of the on-chip drive stage. |
| OUTA | – | 11 | O | High current totem pole output A of the on-chip drive stage. |
| OUTB | – | 14 | O | High current totem pole output B of the on-chip drive stage. |
| PGND | 12 | 12 | – | Ground return pin for the output driver stage |
| RAMP | 7 | 7 | I | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| RT | 5 | 5 | I | Timing resistor connection pin for oscillator frequency programming |
| SS | 8 | 8 | I | Soft-start input pin which also doubles as the maximum duty cycle clamp. |
| VC | 13 | 13 | – | Power supply pin for the output stage. This pin should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor with minimal trace lengths. |
| VCC | 15 | 15 | – | Power supply pin for the device. This pin should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor with minimal trace lengths |
| VREF | 16 | 16 | O | 5.1-V reference. For stability, the reference should be bypassed with a 0.1- μ F monolithic ceramic low ESL capacitor and minimal trace length to the ground plane. |

APPLICATION INFORMATION



UDG-03047

Figure 1. Typical Application: 1.5 MHz, 48-V to 5-V DC/DC Push-Pull Converter Using UC28025

APPLICATION INFORMATION

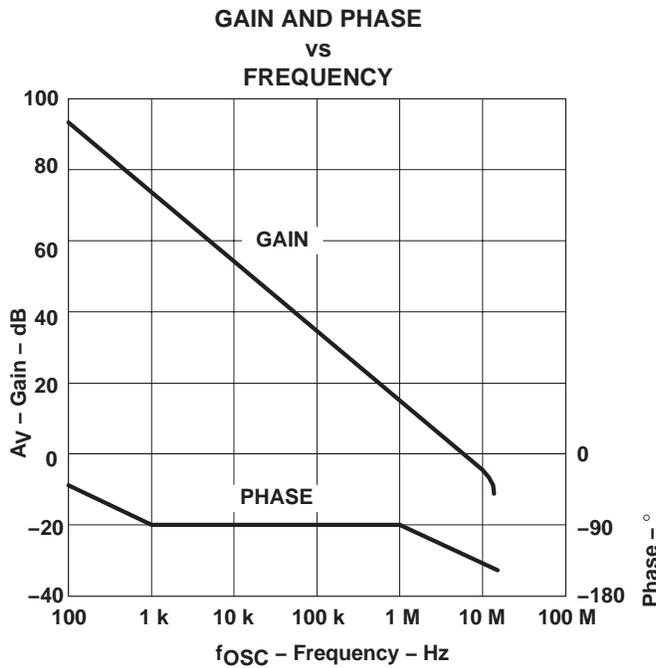


Figure 3. Open Loop Frequency Response

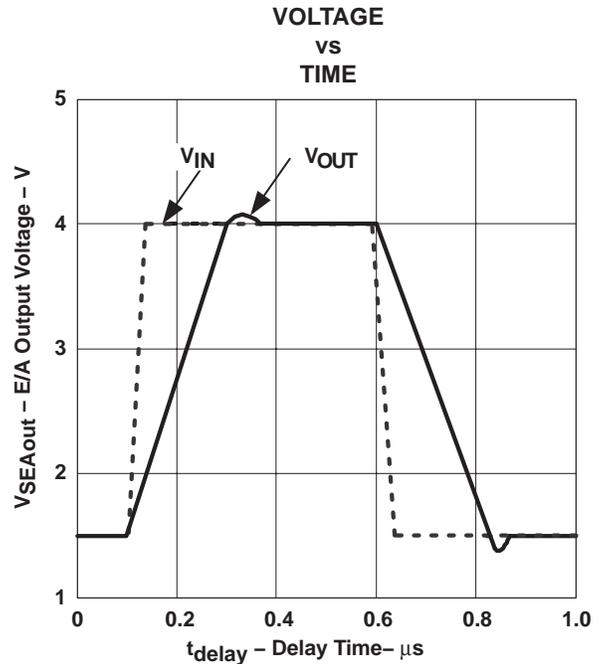


Figure 4. Unity Gain Slew Rate

CONTROL METHODS

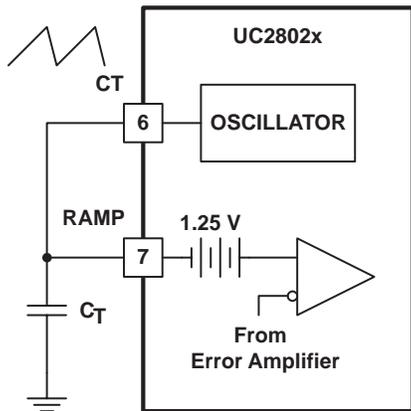
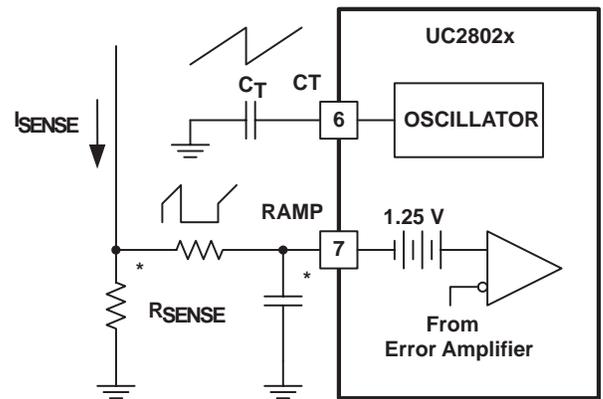


Figure 5. Voltage Mode Control

UDG-03050



* A small filter may be required to suppress switch noise.

UDG-03050

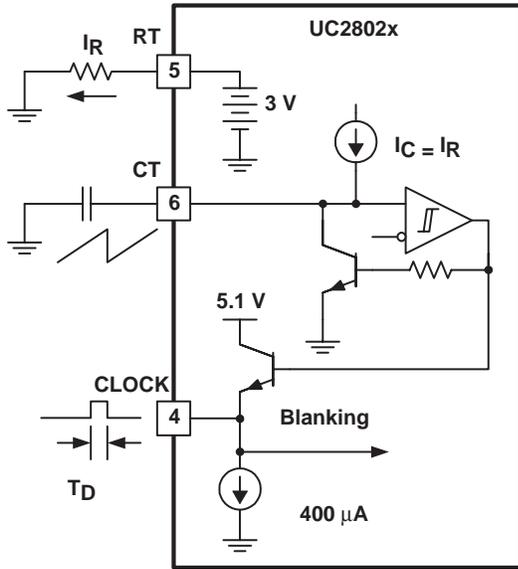
Figure 6. Peak Current Mode Control

**UC28023
UC28025**

SLUS557B – MARCH 2003 – REVISED APRIL 2004

APPLICATION INFORMATION

OSCILLATOR



UDG-03052

Figure 7. Oscillator Circuit

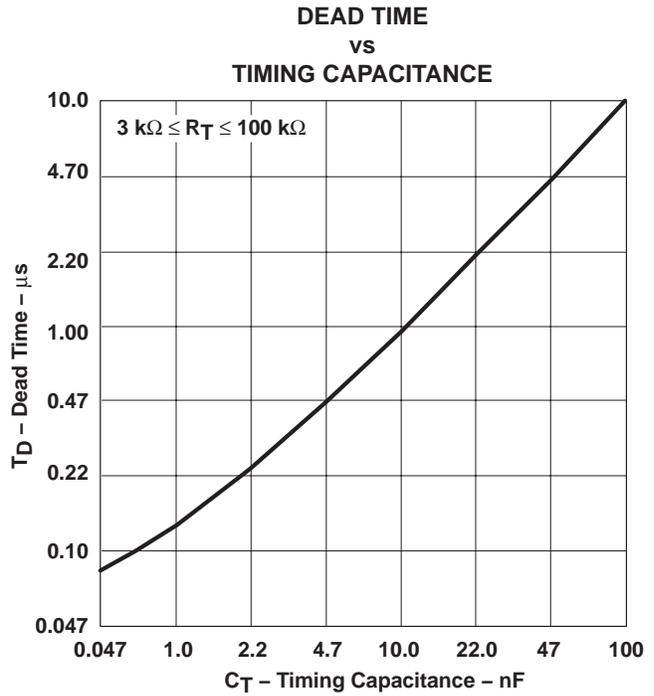


Figure 8.

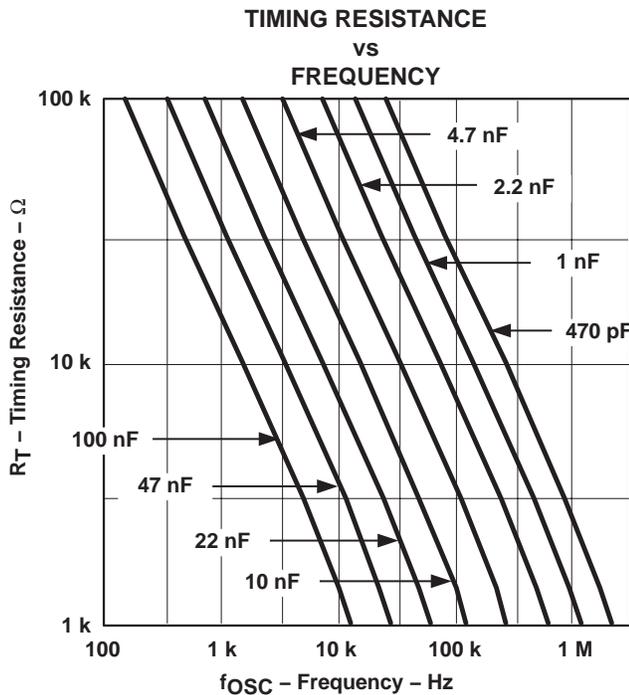


Figure 9. Oscillator Circuit

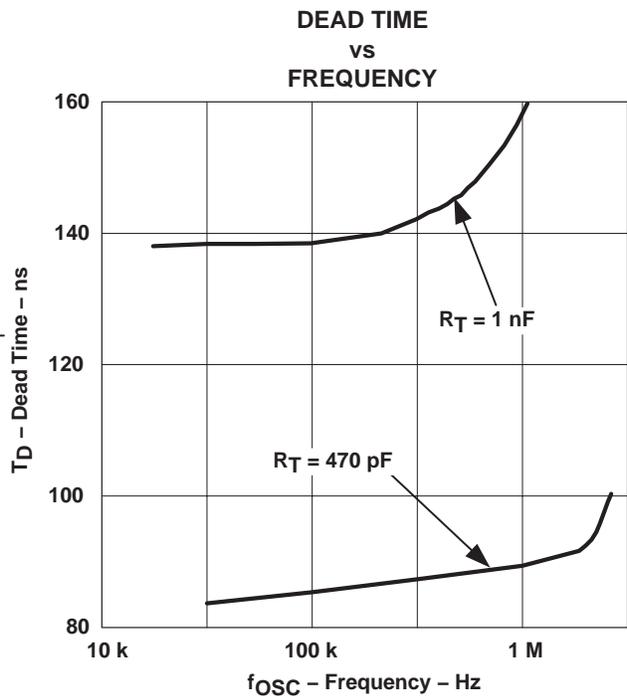
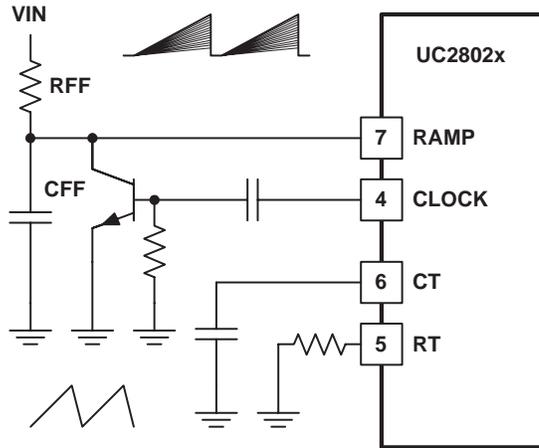


Figure 10.

APPLICATION INFORMATION

FEEDFORWARD CIRCUIT

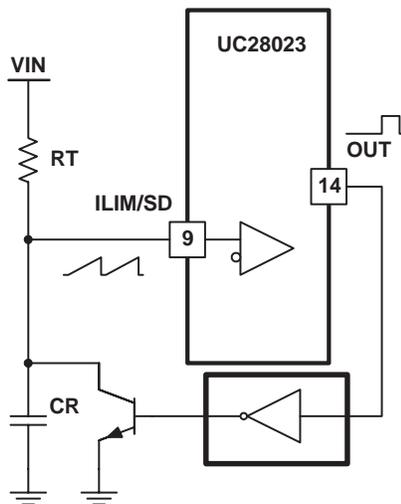


UDG-03050

Figure 13. Feedforward Technique for Off-Line Voltage-Mode Applications

CONSTANT VOLT-SECOND CLAMP CIRCUIT

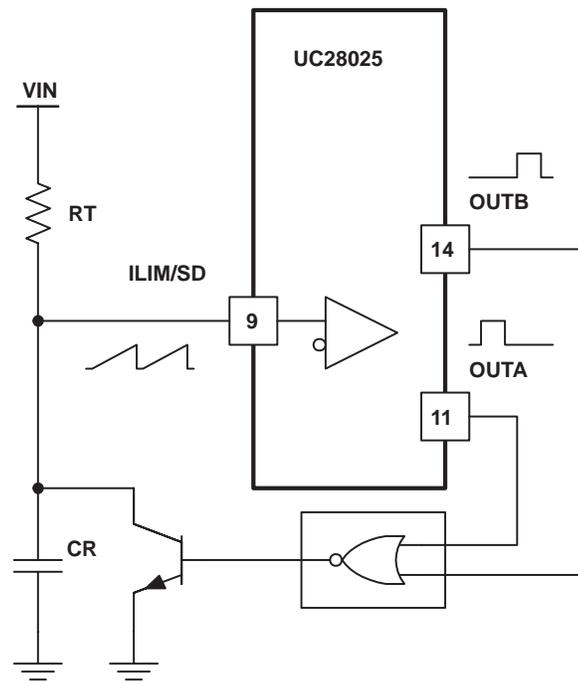
The circuit for the UC28023 shown in Figure 14 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



UDG-03050

Figure 14. Achieving Constant Volt-Second Product Clamp with the UC28023

The circuit for the UC28025 shown in Figure 15 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



UDG-03050

Figure 15. Achieving Constant Volt-Second Product Clamp with the UC28025

UC28023
UC28025

SLUS557B – MARCH 2003 – REVISED APRIL 2004

APPLICATION INFORMATION

OUTPUTS

UC28023 has one output and UC28025 has dual alternating outputs.

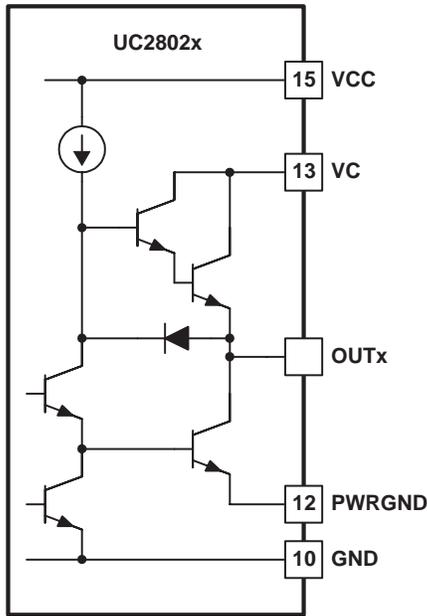


Figure 16. Simplified Schematic

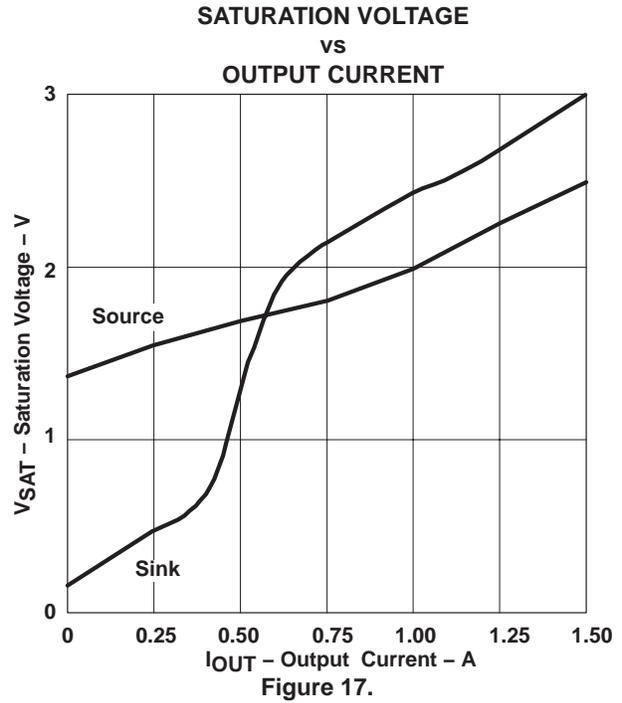


Figure 17.

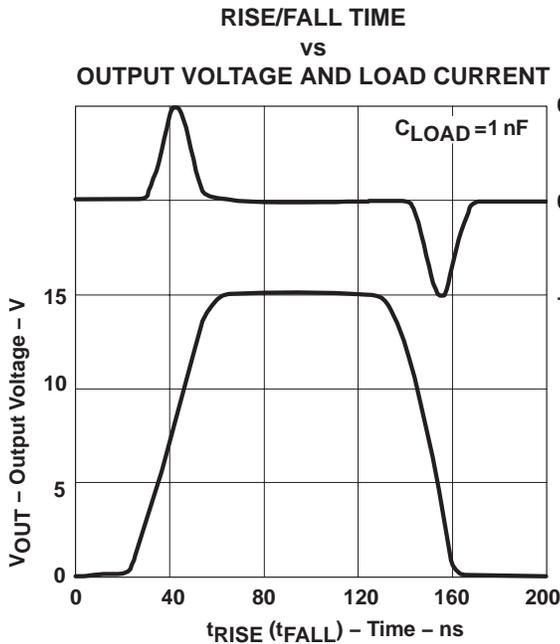


Figure 18.

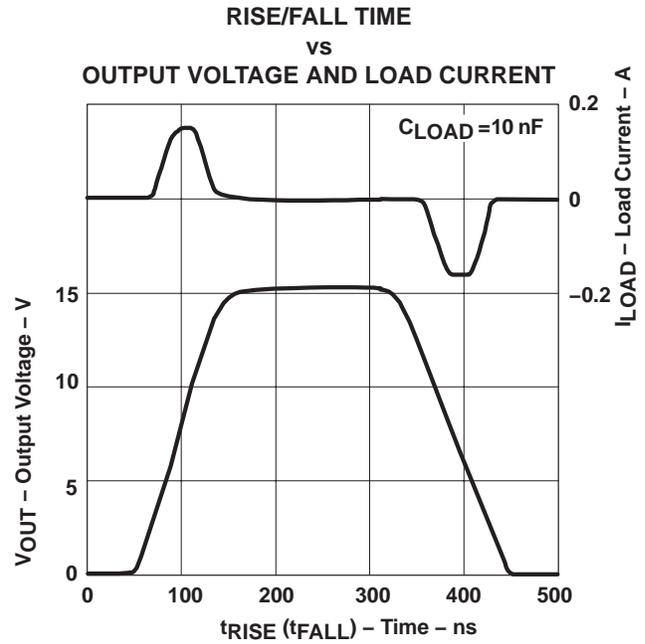
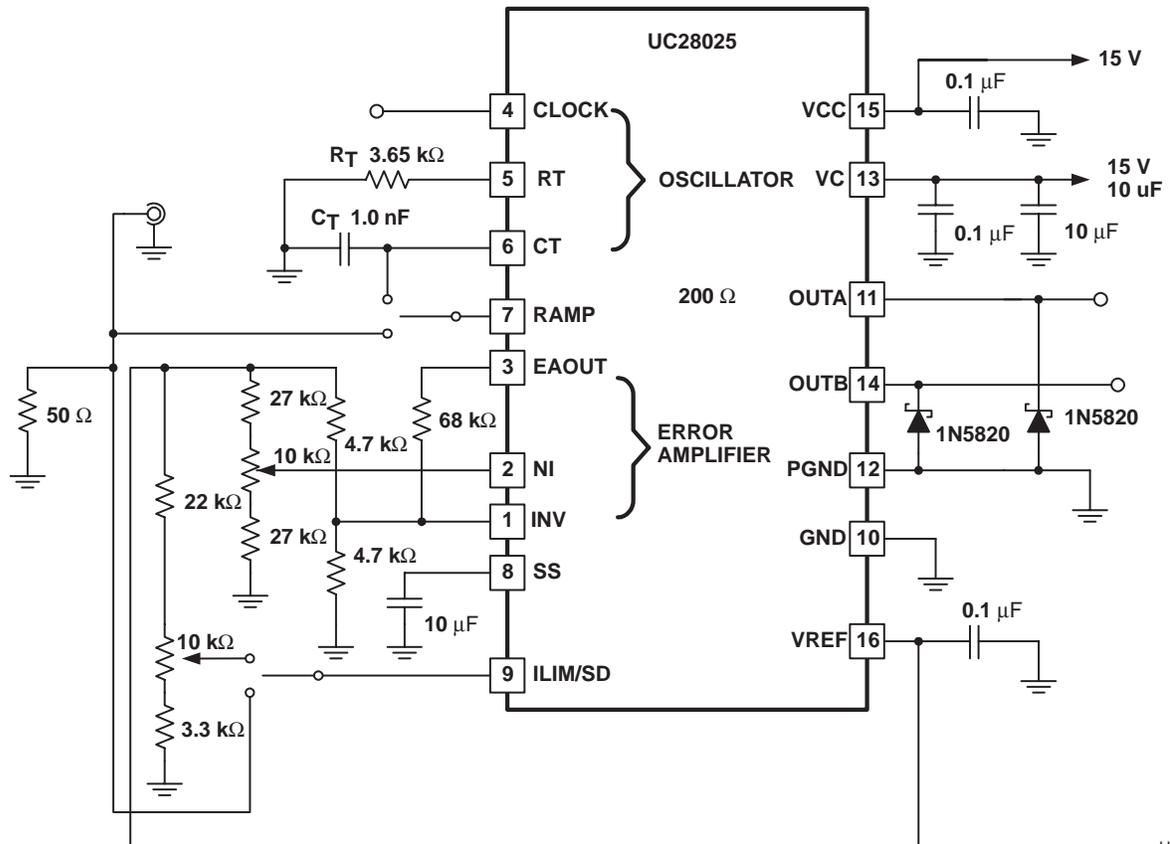


Figure 19.

APPLICATION INFORMATION

Open Loop Laboratory Test Fixture

The following test fixture is useful for exercising many of the UC28025's functions and measuring their specifications. As with any wideband circuit, careful ground and by-pass procedures should be followed. The use of a ground plane is highly recommended.



UDG-03051

Figure 20. Laboratory Test Fixture

References

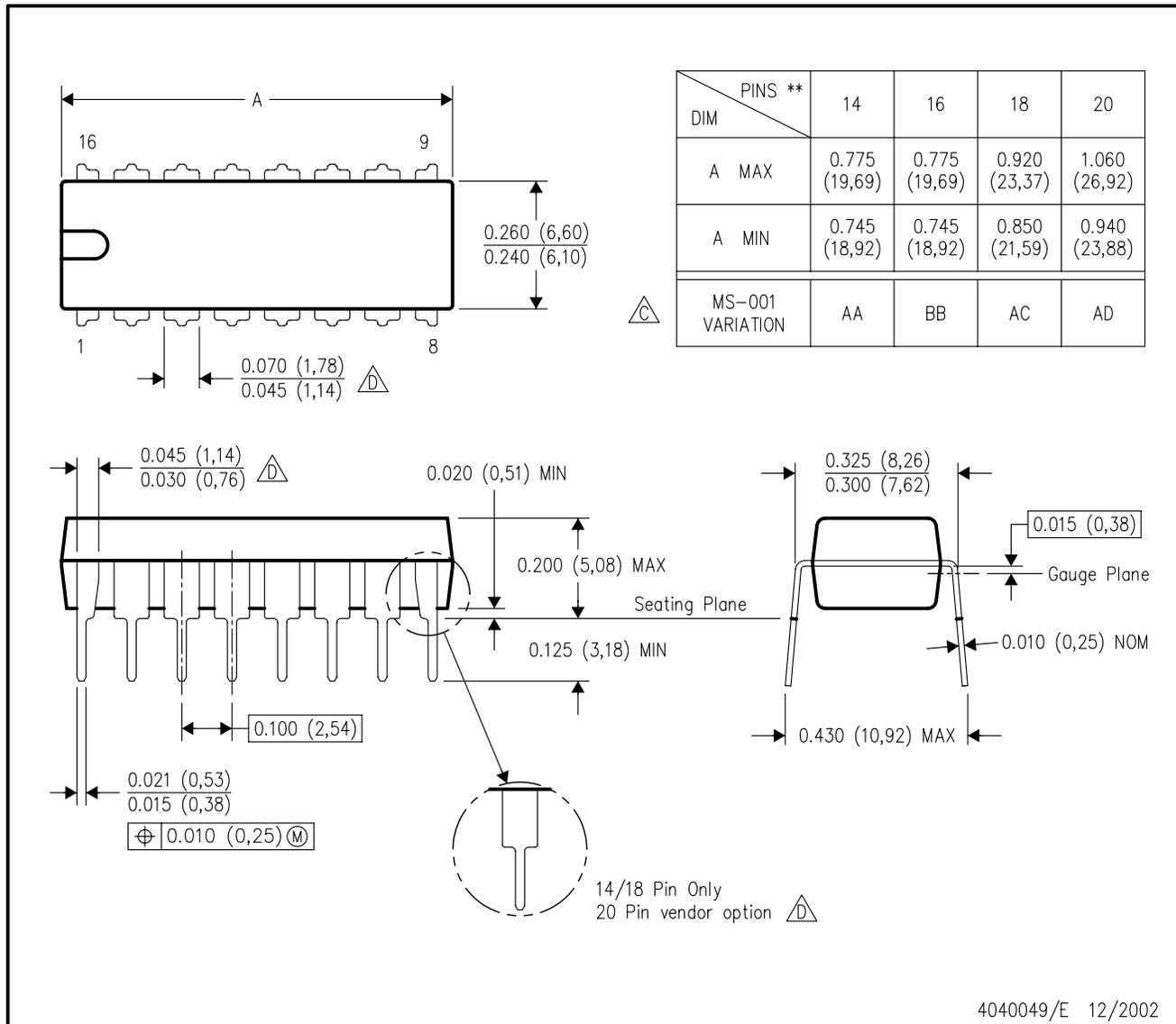
1. *1.5-MHz Current Mode IC Controlled 50-Watt Power Supply*, Texas Instruments Application Note Literature No. SLUA053.
2. *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, Texas Instruments Application Note Literature No. SLUA125.

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

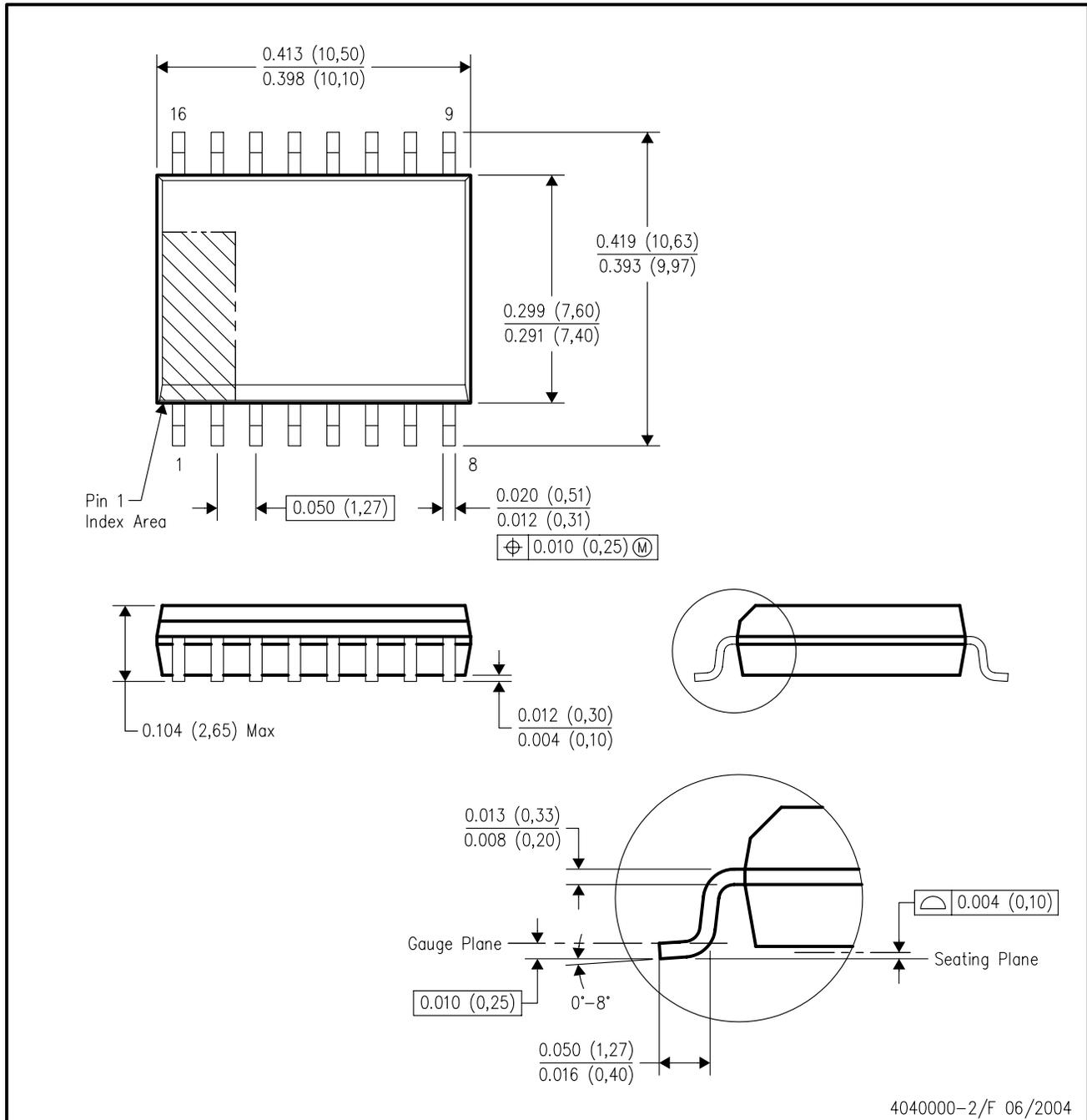


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265