

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

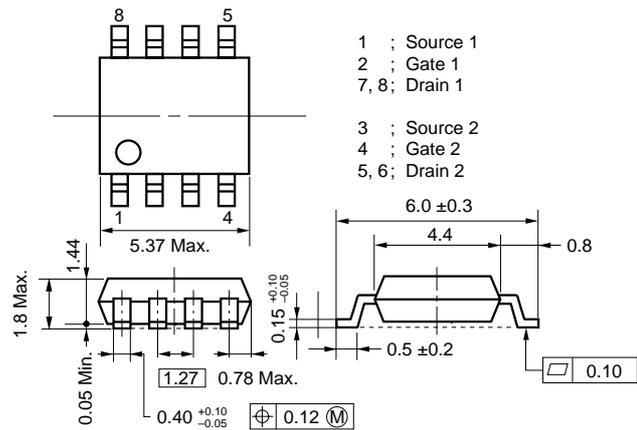
FEATURES

- Dual MOS FET chips in small package
- 2.5-V gate drive type and low on-resistance
 $R_{DS(on)1} = 30 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 3.0 \text{ A)}$
 $R_{DS(on)2} = 40 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_D = 3.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 800 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1756G	Power SOP8

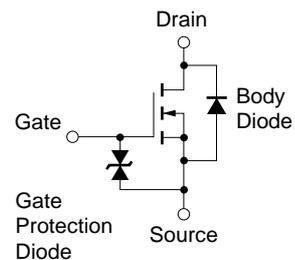
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	20	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±12.0	V
Drain Current (DC)	I _{D(DC)}	±6.0	A
Drain Current (Pulse) ^{Note1}	I _{D(pulse)}	±24	A
Total Power Dissipation (1 unit) ^{Note2}	P _T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. T_A = 25 °C, Mounted on ceramic substrate of 2000 mm² x 1.1 mm

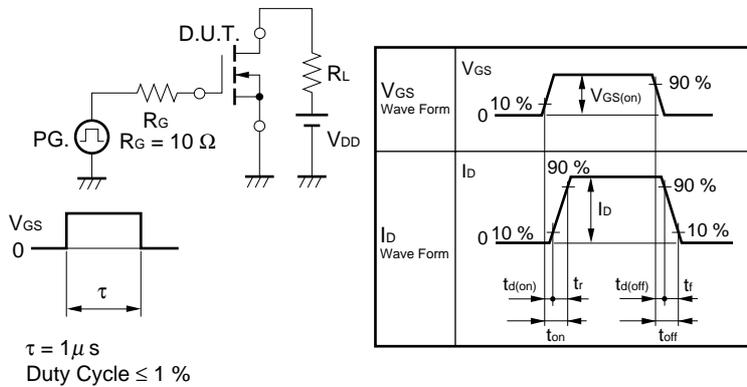
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

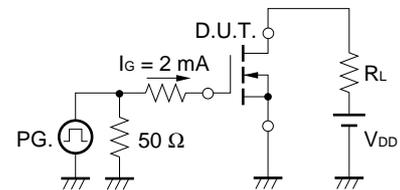
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 3.0 A		20.0	30	mΩ
	R _{DS(on)2}	V _{GS} = 2.5 V, I _D = 3.0 A		25.8	40	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	0.5	0.7	1.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.0 A	4.0	12		S
Drain Leakage Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±12.0 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		800		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		360		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	t _{d(on)}	I _D = 3.0A		110		ns
Rise Time	t _r	V _{GS(on)} = 4.0 V		425		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 10 V		1050		ns
Fall Time	t _f	R _G = 10 Ω		1200		ns
Total Gate Charge	Q _G	I _D = 6.0 A		11		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 16 V		2.0		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 4.0 V		4.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 6.0 A, V _{GS} = 0 V		0.8		V

TEST CIRCUIT 1 SWITCHING TIME

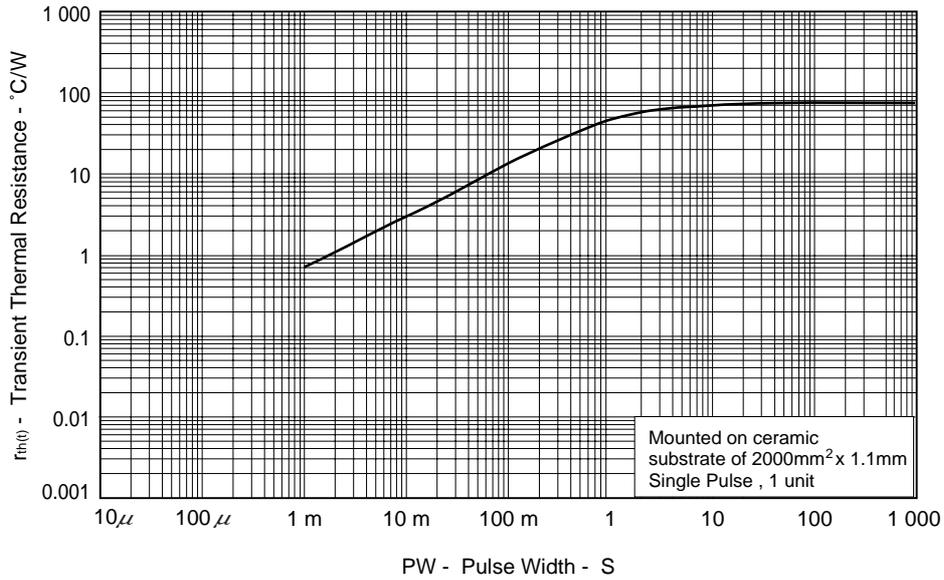


TEST CIRCUIT 2 GATE CHARGE

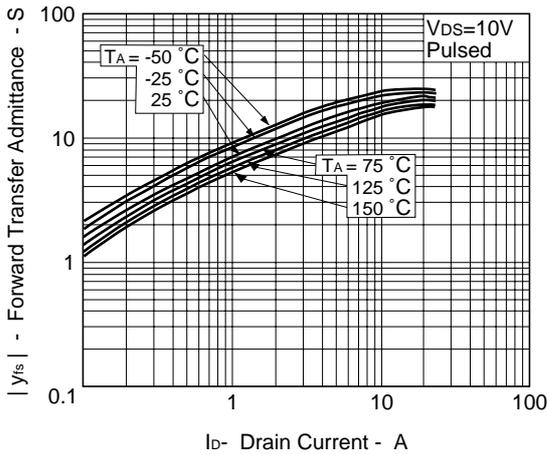


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

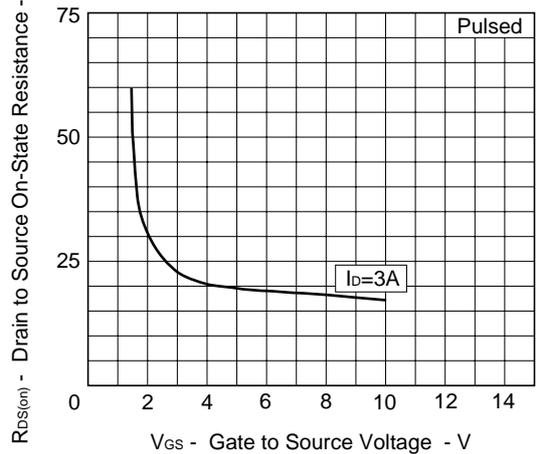
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



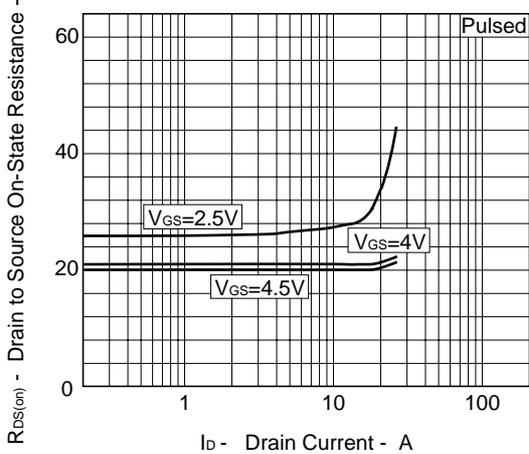
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



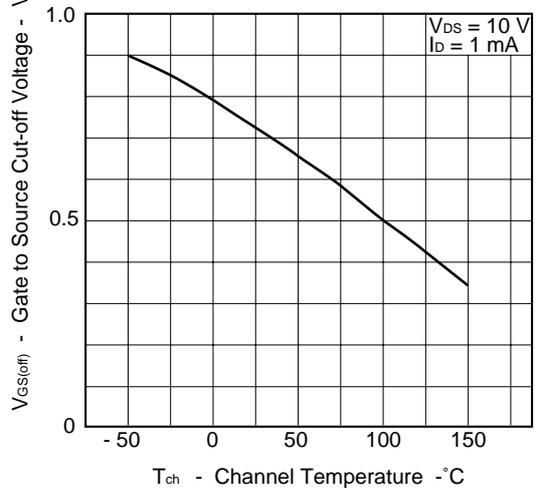
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



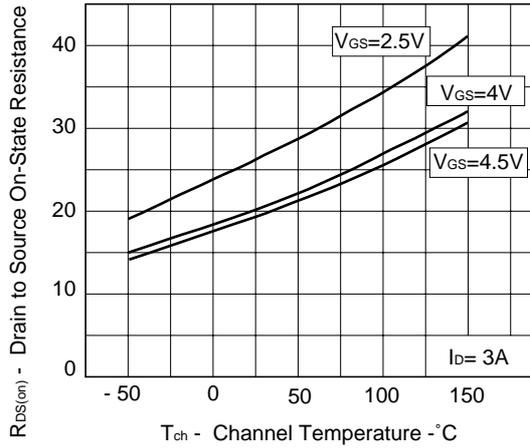
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



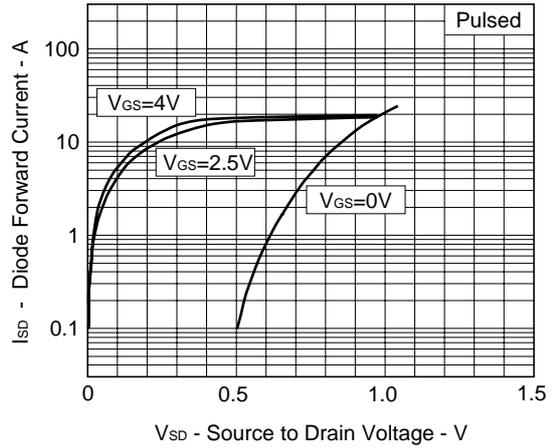
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



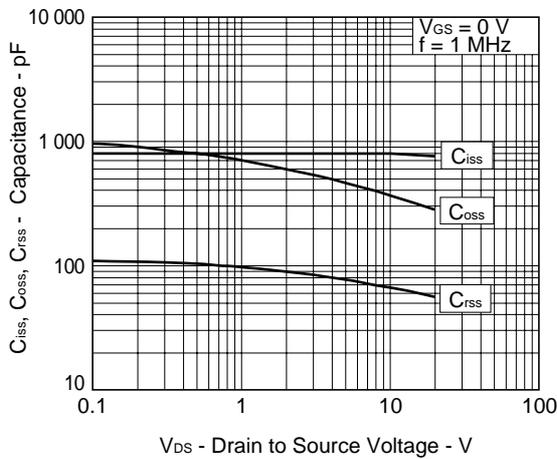
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



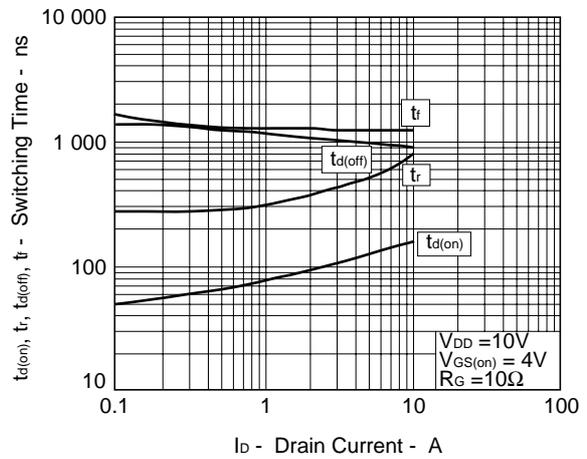
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



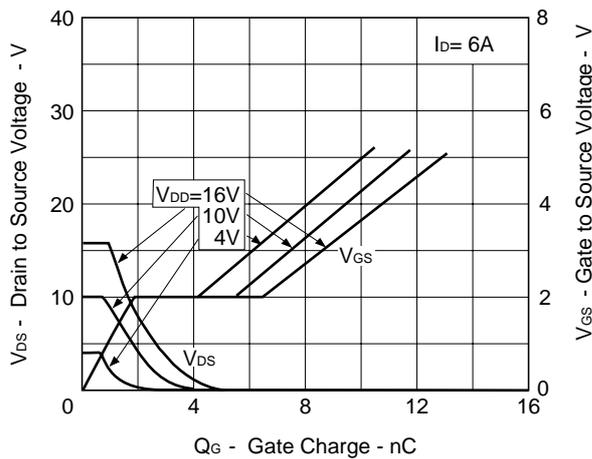
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



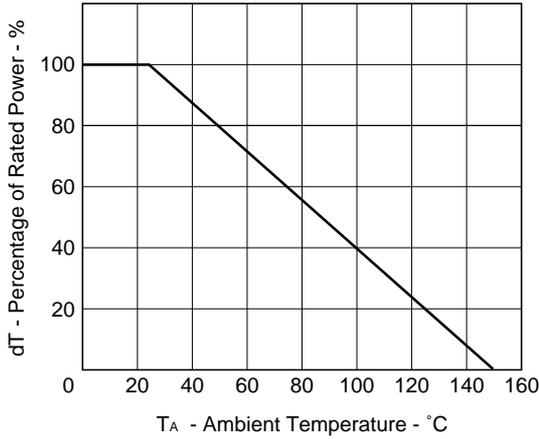
SWITCHING CHARACTERISTICS



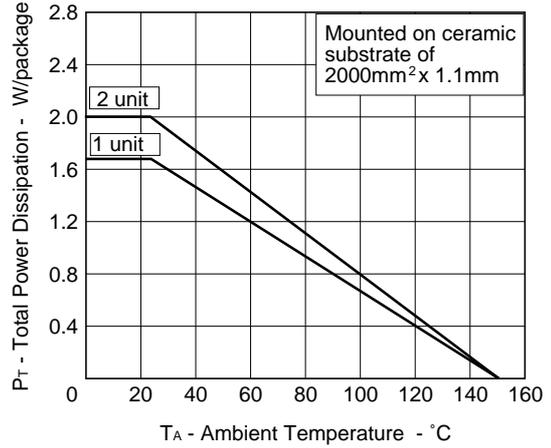
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



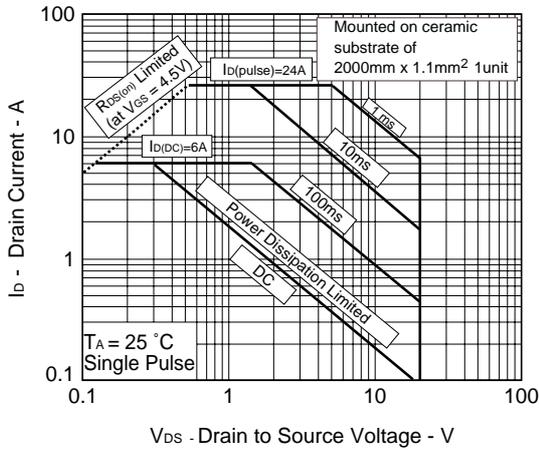
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



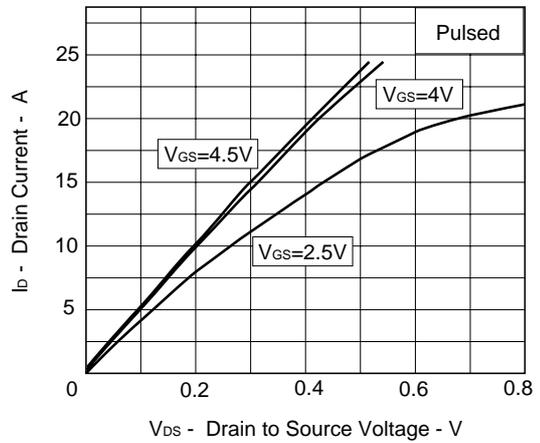
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



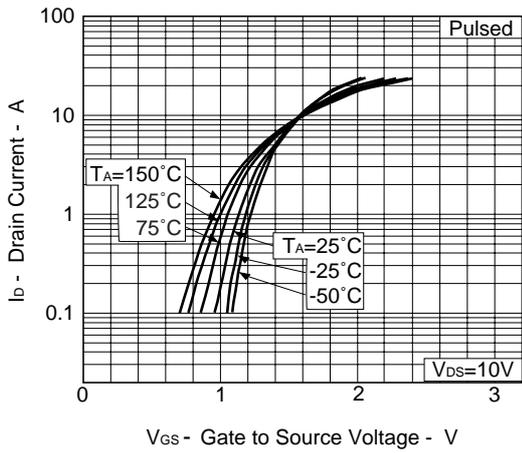
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



[MEMO]

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