CEL

NEC's LOW POWER GPS RF RECEIVER

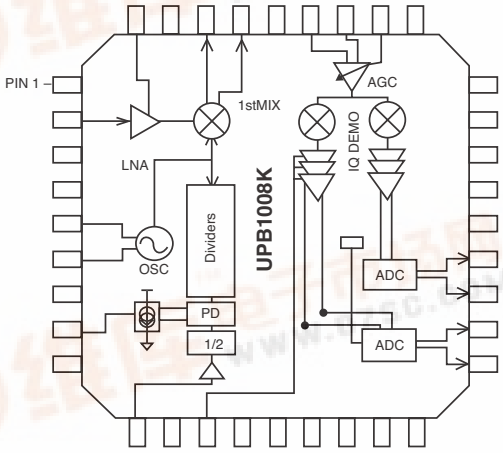
UPB1008K

FEATURES

- **LOW POWER CONSUMPTION:** 52 mW
- **DUAL-CONVERSION IQ DOWN CONVERTER[1]:** Reference frequency: REFin = 27 MHz
- **PSEUDO-BASEBAND WITH 2-BIT DIGITIZED OUTPUT**
- **ON-CHIP LNA, ON-CHIP FREQUENCY SYNTHESIZER, IF AGC AMPLIFIER:** with 45 dB typical range of adjustable gain
- **SMALL 36 PIN QFN PACKAGE:** Flat lead style for better RF performance

Note:
1. Based on eRide's proprietary GPS DSP architecture

BLOCK DIAGRAM



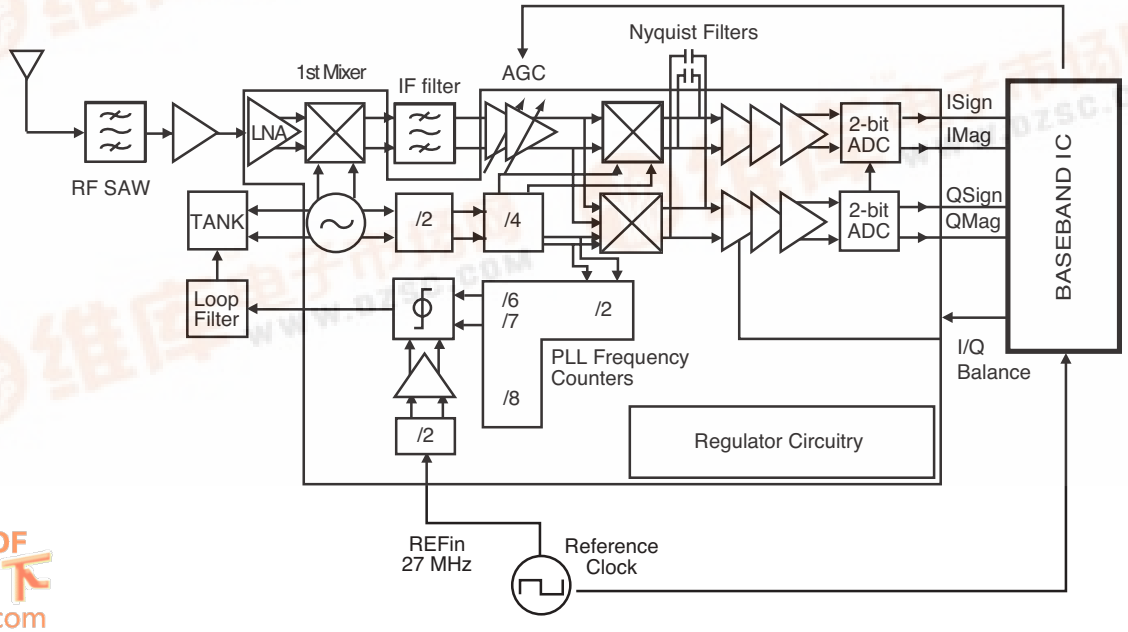
APPLICATIONS

- **E911 ENABLED MOBILE PHONE**
- **IN-VEHICLE NAVIGATION SYSTEMS**
- **LOW POWER HANDHELD GPS RECEIVER**
- **PC/PDA+GPS INTEGRATION**
- **ASSET TRACKING**

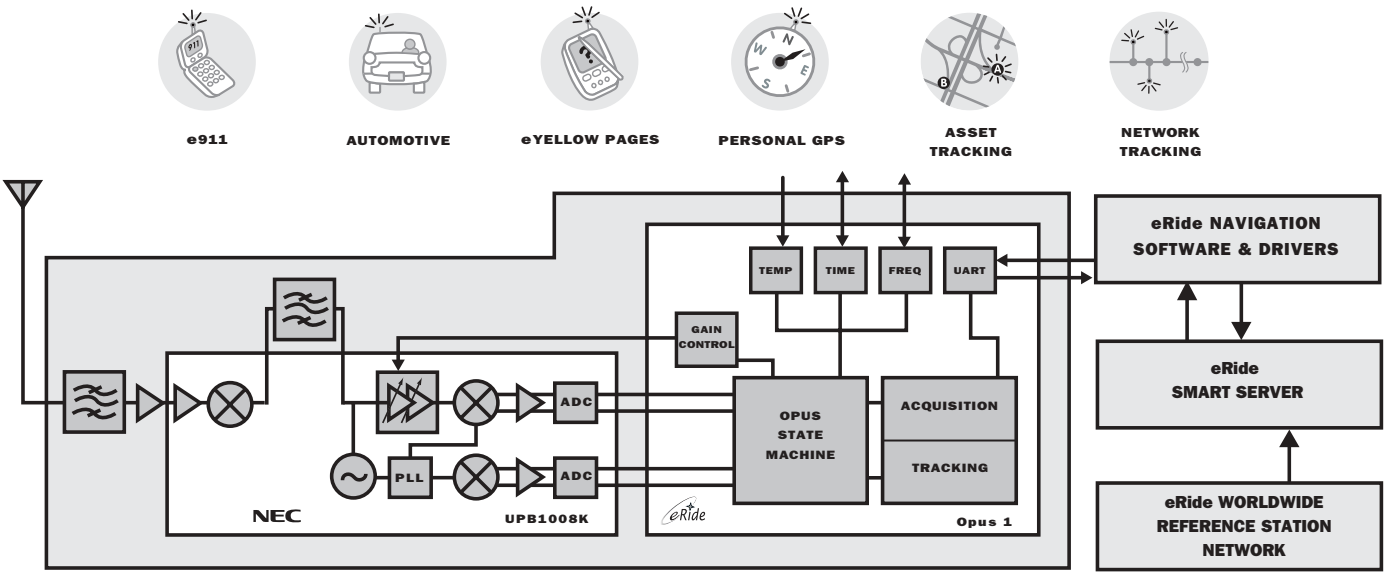
DESCRIPTION

NEC's UPB1008K is a Silicon RFIC especially designed for handheld low power/low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The second IF Freqency is a pseudo- baseband signal into a on-chip 2-bit A/D converters.The device can operate on a supply voltage as low as 2.7 V, and is a housed in a small 36 pin QFN (Quad, Flat, No-lead) package, resulting in a very low power consumption and reduced board space.
NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

RF APPLICATION DIAGRAM



ADVANCED GPS COMPLETE SOLUTION



ADVANCED GPS COMPLETE SOLUTION

"NEC Corporation and eRide, Inc. have teamed to provide an advanced positioning solution delivering high GPS performance, accuracy, integration and architecture flexibility. The chip set combines CEL's **UPB1008K** receiver IC with eRide's **Opus One** SOC (System-on-a-Chip) Baseband ASIC and is suitable for standard GPS products as well as Cellular Handset applications. Also provided are scalable client navigation software and drivers, plus location-aiding data from eRide's Smart Server. Together, they offer a complete hardware/infrastructure solution.

The chip set's design allows it to operate independently of wireless interface standards - and independently of the host product's CPU and Operating System. This unique approach to system integration makes it easy to deploy the chip set into an wireless application, in any wireless network. A "Universal Hardware" solution, the design promises lower manufacturing costs and, ultimately lower cost to the consumer.

The chip set's advanced positioning architecture offers unmatched sensitivity providing fast, accurate positioning architecture offers unmatched sensitivity providing fast and accurate position fixes, even when indoors or in deep in urban canyons."

HIGH PERFORMANCE GPS OMNI MODE

LI, C/A code receiver

Performance	Indoor	Outdoor
Time to First Fix w/ aiding	5-7sec	1-3sec
Time to First Fix w/o aiding	10-20sec	3-5sec
Accuracy	10-25m cep	2-5m cep
Sensitivity	-155dBm in 1sec dwells	-142dBm in two 10msec dwells

Superior performance in high reflection indoor environments and in urban canyon types of outdoor environments

POWER DISSIPATION

First Fix	400 mW
Tracking	200-300 mW
Stand By	30 mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, unless otherwise specified)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{CC}	Total Circuit Current, No Signals	mA	14	18	23.5
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
I_{CC_PD}	Power down current, PIN 13 = V_{IL}	μA	–	1	10
I_{CC} rf	RF Block Circuit Current (pin 3), No signal	μA	0.4	0.5	0.7
I_{CC} lo	VCO Block Circuit Current (pin 7), No signal	mA	4.1	5.6	7.2
ICC pll	PLL Block Circuit Current (pin 9), No signal	mA	2.7	3.6	4.7
ICC bb	Baseband Block Circuit Current (pin 23), No signal, open load	mA	2.5	3.4	4.3
ICC if	IF Block Circuit Current (pin 28) , No signal	mA	2.7	3.7	4.7
ICC lna	Pre-Amplifier Open Connector Current (pin 36), No signal	mA	1.0	1.4	1.8

LNA/RF DOWNCONVERTER

(f_{RFin} = 1575.42 MHz, $f_{1stLOin}$ = 1400 MHz, P_{LO} = -10 dBm, f_{1stIF} = 175 MHz, Pin 13: V_{IL} = 3 V, Z_L differential = 32Ω & Z_S = Γopt)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
CG_{LNA_MIX}	Power conversion gain from 2nd LNA/mixer to 1st IF, P_{RFin} = -50 dBm	dB	18	23	28
NF_{LNA_MIX}	Noise Figure of 2nd LNA/mixer(SSB), Input matched	dB	–	5	–
P_{1dBLNA_MIX}	1 dB Compression refer to source, Input matched	dBm	–	-38	–
Z_{LNAin}	RF Input Impedance of LNA	Ohm	–	31	–
Z_{MIXout}	IF Output Impedance of Mixer	Ohm		32	
A_{LO-IF}	Local Signal Leak to IF, $f_{1stLOin}$=1400 MHz, P_{LO} = 0 dBm	dBm	–	-35	–
A_{LO-RF}	Local Signal Leak to RF, $f_{1stLOin}$=1400 MHz, P_{LO} = 0 dBm	dBm	–	-50	–

PLL

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{CPOH}	PLL Charge Pump High Side Current @ V_{CPout} = V_{CC}/2	μA	–	200	–
I_{CPOL}	PLL Charge Pump Low Side Current @ V_{CPout} = V_{CC}/2	μA	–	-200	–
f_{PD}	Phase Comparison Frequency	MHz	–	13.5	–

CRYSTAL OSCILLATOR/REVERENCE AMPLIFIER BLOCK

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
V_{REFin}	Reference input minimum level	mVpp	50	200	–
f_{REF}	Input Frequency of Reference Input	MHz	–	27	–
VT	VCO Control Voltage, PLL Locked	V	0.8	1.5	2.2
C/N	VCO C/N, ⊿1kHz, Loop band width = 5 kHz	dBc/Hz	57	62	–

AGC AMPLIFIER, I-Q DEMODULATOR, and ADC BLOCK($f_{1stIFin}$ = 175 MHz, Z_{in} = 600Ω)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
$CG_{AGC/MIX}$	Maximum voltage conversion gain of AGC amplifier/ I-Q mixer, P_{in} = -60 dBm, V_{AGC} = 0.5 V, Unmatched	dB	–	30	–
	Minimum voltage conversion gain of AGC amplifier/ I-Q mixer, P_{in} = -60 dBm, V_{AGC} = 2.0 V, Unmatched	dB	–	-15	–
$A_{AGC/MIX}$	AGC control range, V_{AGC} = 0.5 V to 2 V	dB	25	45	–
P_{1dBAGC}	1 dB compression input to AGC amplifier, set voltage gain = 30 dB	dBm	–	-45	–
V_{AGC}	AGC control voltage	V	0.5	–	2.0
BW	3dB Mixer Bandwidth	MHz	–	10	–
V_{IQ-C}	IQ BalanceControl Voltage, Gain(Ich) = Gain (Qch)	V	–	2.1	2.8
A_{IQ-C}	IQ Balance Control Gain Range, V_{IQ-C} = 0 to 3 V	dB	4.0	6.5	–
Duty Ich	Ich Mag Bit Output Pulse Duty, P1stIFin = -84 dBm V_{AGC} = 0.5 V, V_{IQ-C} = 0 V	%	50	–	–
Duty Qch	Qch Mag Bit Output Pulse Duty, PIF2in = -88 dBm V_{AGC} = 0.5 V, V_{IQ-C} = 0 V	%	50	–	–

BASEBAND AMPLIFIER BLOCK (Z_S = 2kΩ & Z_L = 2 kΩ)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
V_{BBOH}	Baseband output logic high, C_L = 10 pF	V	2.0	–	–

ABSOLUTE MAXIMUM RATINGS[1,2] (T_A = 25°C)

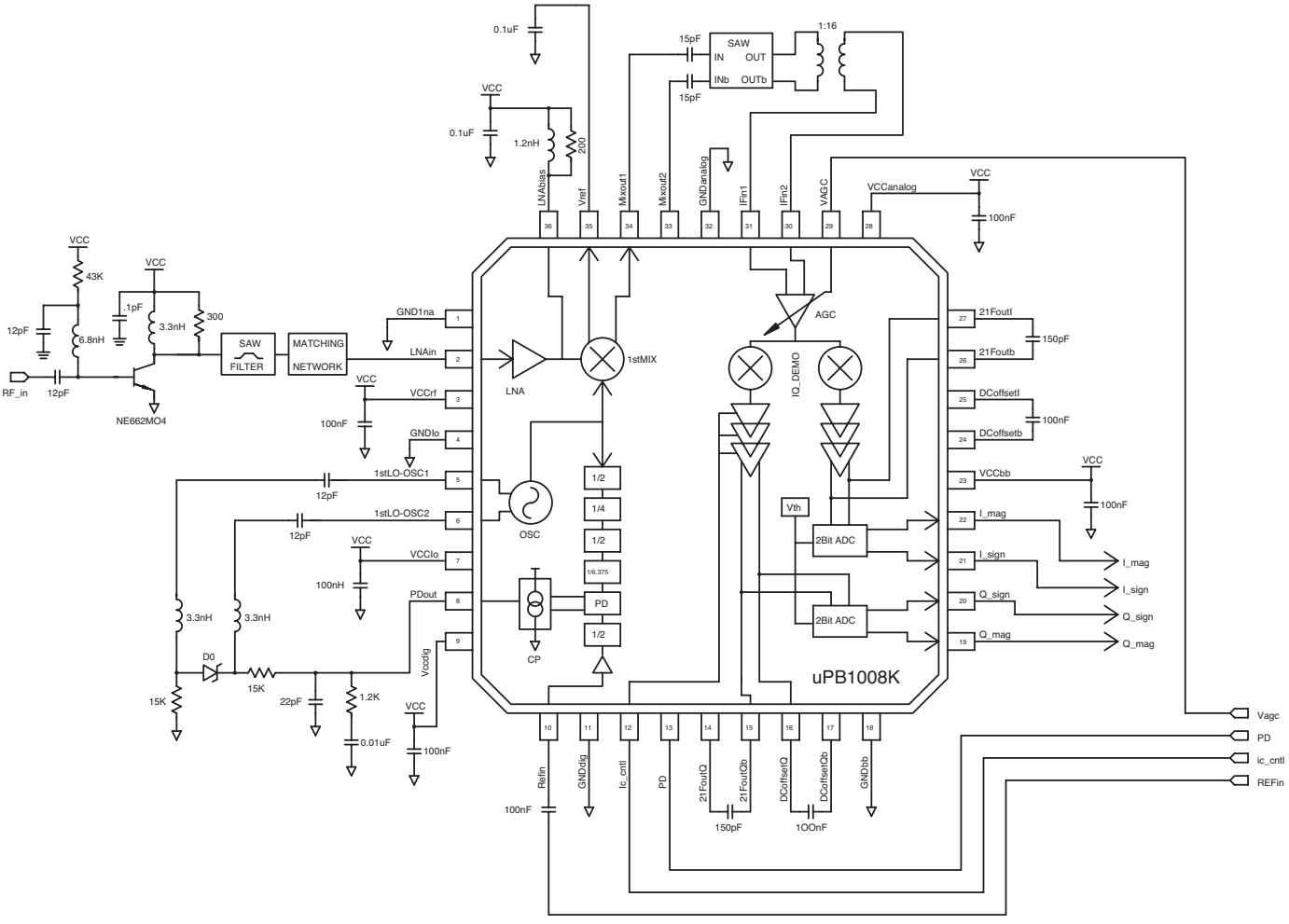
SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage[4]	V_{CC}	3.6
P_D	Total Power Dissipation[3]	mW	361
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150
I_{CC_total}	Total Circuit Current[4]		

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. More than two items must not be reached simultaneously.
3. T_A = +85°C, mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.
4. T_A = 25°C

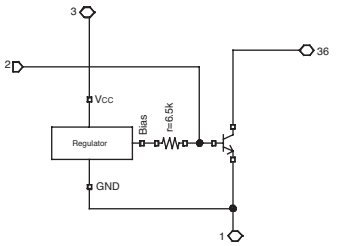
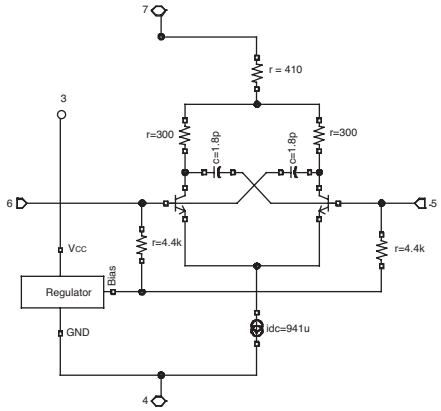
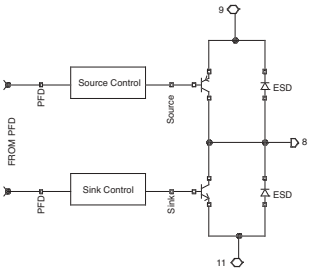
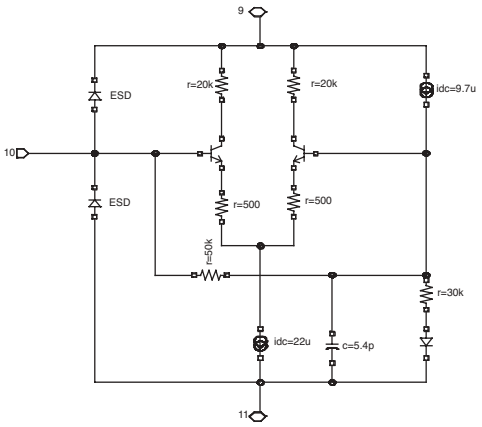
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{RFin}	RF Input Frequency	MHz		1575	
f_{REFin}	Reference Frequency	MHz		27	
f_{1stLO}	1st LO Oscillating Frequency	MHz		1400	
$f_{1stIFin}$	1st IF Input Frequency	MHz		175	
$f_{2ndLOin}$	2nd LO Input Frequency	MHz		175	
V_{IH}	Power Down Control Voltage "High"	V	2		V_{CC}
V_{IL}	Power Down Control Voltage "Low"	V	0		0.5

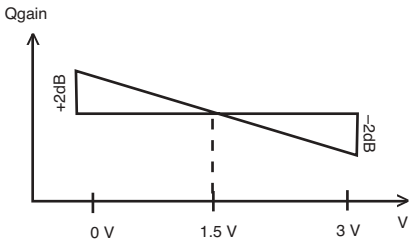
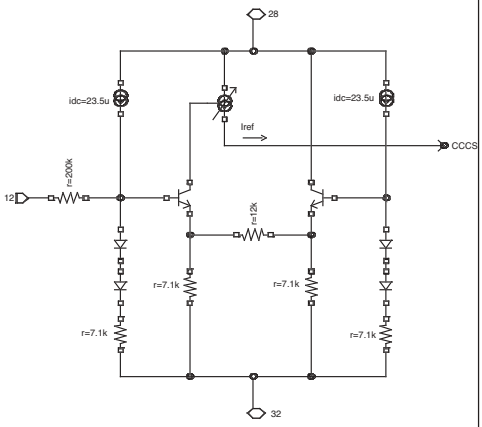
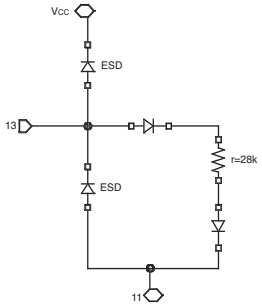
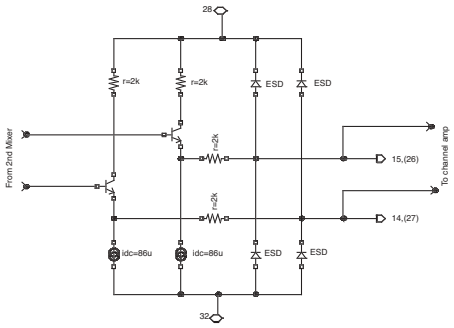
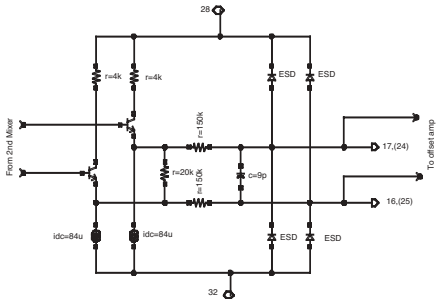
APPLICATION CIRCUIT



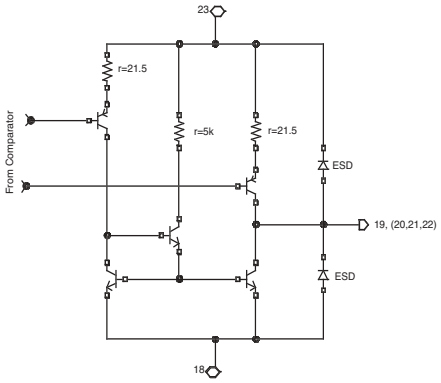
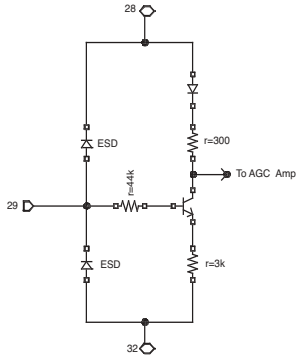
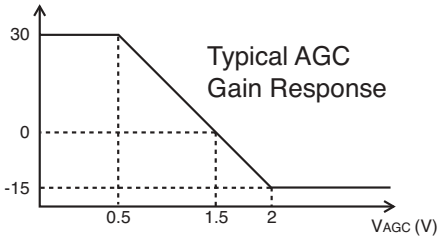
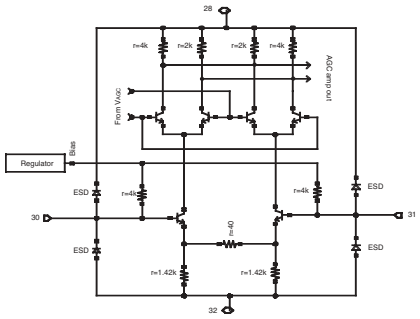
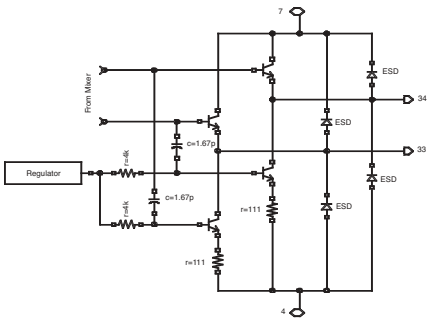
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
1	GNDlna	Ground pin of LNA	
2	LNAin	Input pin of low noise amplifier. It is a single-ended open collector design. Capacitive coupling is required; external matching will improve gain or NF.	
3	VCCrf	Supply voltage pin of LNA, RF mixer and VCO voltage regulator.	
4	GNDlo	Ground pin of 1st LO Oscillator circuit and RF Mixer.	
5	1stLO-OSC1	Pin 5 & 6 are base pins of the differential amplifier for 1st LO oscillator. These pins require an LC (varacator) tank circuit to oscillate at around 1400 MHz.	
6	1stLO-OSC2		
7	VCClo	Supply voltage pin of oscillator circuit for 1st LO Oscillator and RF mixer	
8	PDout	This is a current mode charge pump output. For connection to a passive RC loop filter for driving external varactor diode of 1stLO-OSC.	
9	VCCdig	Supply voltage pin of digital portion of the chip.	
10	REFin	Input pin of reference frequency buffer. This pin should be equipped with external 27 MHz oscillator (e.g. TCXO).	
11	GNDdig	Ground pin of digital portion of the chip.	

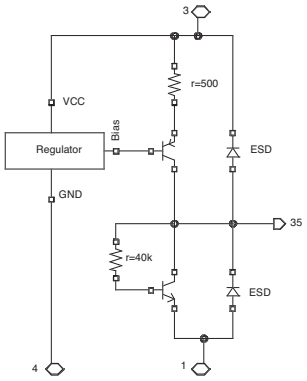
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
12	I/Q Balance Control	The voltage on this pin controls the Q channel IF Amplifier Gain. Gain control of ±2 dB can be achieved for 0~3 V. Leave open-circuited if not used. 	
13	PD1	Standby mode control. Low=whole chip OFF & High=Whole chip ON.	
14 15	2IFout-Q 2IFout-Qb	Differential ouptut pins of quadrature demodulator Q output. Adding a lowpass shunt capacitor between these pins will define the IF Bandwidth.	
16 17	DC offset Q DC offset Qb	DC offset compensation pin for C arm. A low pass capacitor shunt to Pin 17 is required. DC offset compensation pin for Q-bar arm. A low pass capacitor shunt to Pin 16 is required.	

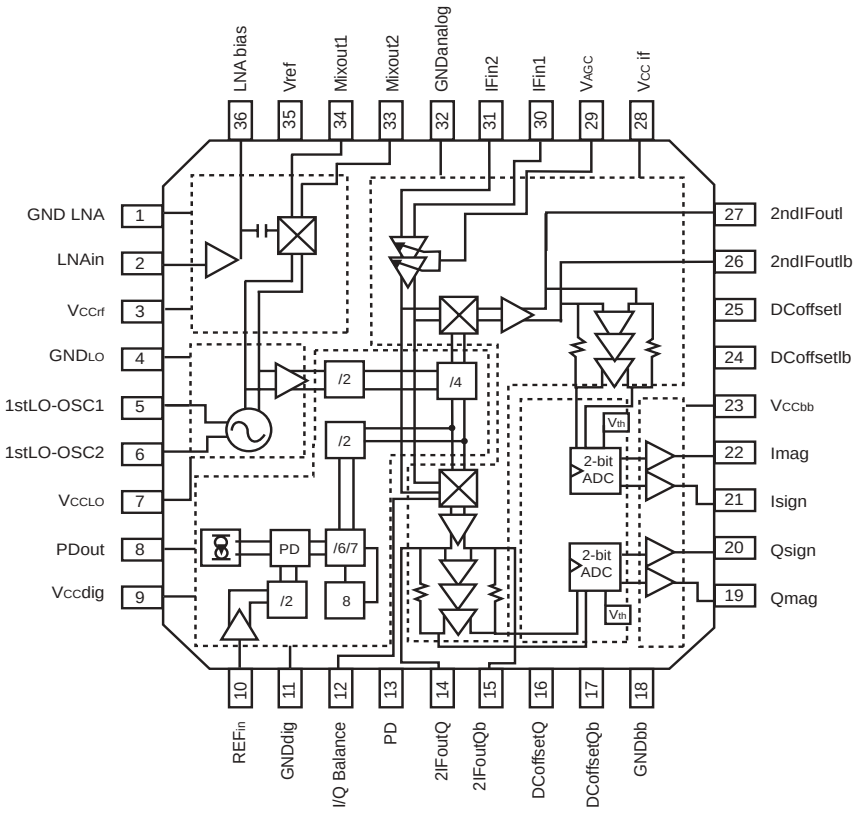
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
18	GNDbb	Ground pin of CMOS output driver.	
19	Qmag	Digitized Q signal. Magnitude bit of 2-bit ADC output.	
20	Qsign	Digitized Q signal. Sign bit of 2-bit ADC output	
21	Isign	Digitized I signal. Sign bit of 2-bit ADC output.	
22	Imag	Digitized I signal. Magnitude bit of 2-bit ADC output.	
23	VCCbb	Supply voltage pin of CMOS output driver.	
24	DCoffsetIb	DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required.	See pin 16 & 17 schematic
25	DCoffsetI	DC offset compensation pin for I arm. A low pass capacitor shunt to Pin 24 is required.	
26	2IFout-Ib	Differential output pins of quadrature demodulator I output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.	See pin 14 & 15 schematic
27	2IFout-I		
28	VCC if	Supply voltage pin of analog portion of the chip.	
29	V_{AGC}	Gain control voltage pin of IF amplifier. This voltage performs reverse control,(i.e., V_{AGC} up → gain down). If this pin is left open, then it is default at maximum gain. 	
30	IF-in1	Differential input pins of 1st IF AGC amplifier	
31	IF-in2		
32	GNDanalog	Ground pin of analog portion of the chip.	
33	Mixout2	Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.	
34	Mixout1		

PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
35	Vref	Base-emitter junction voltage wth respect to ground. May be used for biasing an external discrete transistor. Regulation will develop PTAT current.	
36	LNAbias	LNA output pin. External bias (Vcc) and matching for gain is required.	See pin 2 schematic

INTERNAL BLOCK DIAGRAM

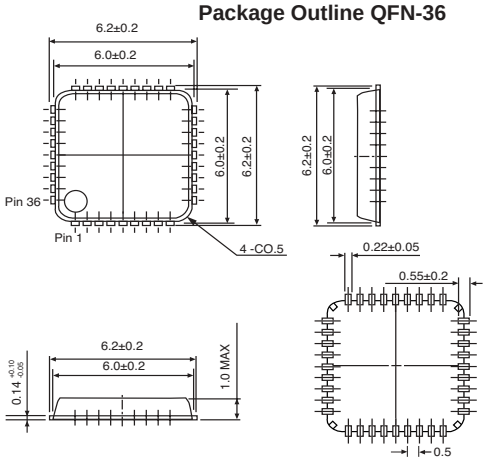


ORDERING INFORMATION

Part Number	Package
UPB1008K	36 Pin plastic QFN

OUTLINE DIMENSIONS (Units in mm)

Package Outline QFN-36



Actual size

Caution:
The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function.

Consequently the island pins should not be soldered and should remain non-connection pins.