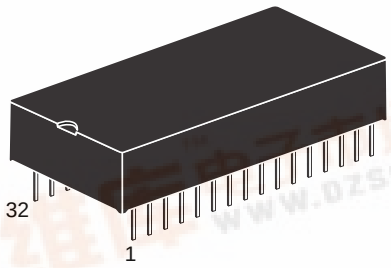
# M48T248Y
# M48T248V

## 5.0 or 3.3V, 1024K TIMEKEEPER® SRAM with PHANTOM

### FEATURES SUMMARY

- 5.0V OR 3.3V OPERATING VOLTAGE
- REAL TIME CLOCK KEEPS TRACK OF TENTHS/HUNDREDTHS OF SECONDS, SECONDS, MINUTES, HOURS, DAYS, DATE OF THE MONTH, MONTHS, and YEARS
- AUTOMATIC LEAP YEAR CORRECTION VALID UP TO THE YEAR 2100
- AUTOMATIC SWITCH-OVER and DESELECT CIRCUITRY
- CHOICE OF POWER-FAIL DESELECT VOLTAGES:
  ($V_{PFD}$ = Power-fail Deselect Voltage):
  - M48T248Y: 4.25V ≤ $V_{PFD}$ ≤ 4.50V
  - M48T248V: 2.80V ≤ $V_{PFD}$ ≤ 2.97V
- FULL 10% $V_{CC}$ OPERATING RANGE
- OVER 10 YEARS' DATA RETENTION IN THE ABSENCE OF POWER
- WATCH FUNCTION IS TRANSPARENT TO RAM OPERATION
- 128K x 8 NV SRAM DIRECTLY REPLACES VOLATILE STATIC RAM OR EEPROM

**Figure 1. 32-pin, DIP Package**




PMDIP32 (PM)

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## SUMMARY DESCRIPTION

The M48T248Y/V TIMEKEEPER® RAM is a 128Kbit x 8 non-volatile static RAM and real time clock organized as 131,072 words by 8 bits. The special DIP package provides a fully integrated battery back-up memory and real time clock solution. In the event of power instability or absence, a self-contained battery maintains the timekeeping operation and provides power for a CMOS static RAM. Control circuitry monitors $V_{CC}$ and invokes write protection to prevent data corruption in the memory and RTC.

The clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction.

The clock operates in one of two formats:

– a 12-hour mode with an AM/PM indicator; or

– a 24-hour mode

The M48T248Y/V is a 32-pin (PM) DIP module that integrates the RTC, the battery, and SRAM in one package.

The modules are shipped in plastic, anti-static tubes (see Table 14, page 22).

**Figure 2. Logic Diagram**

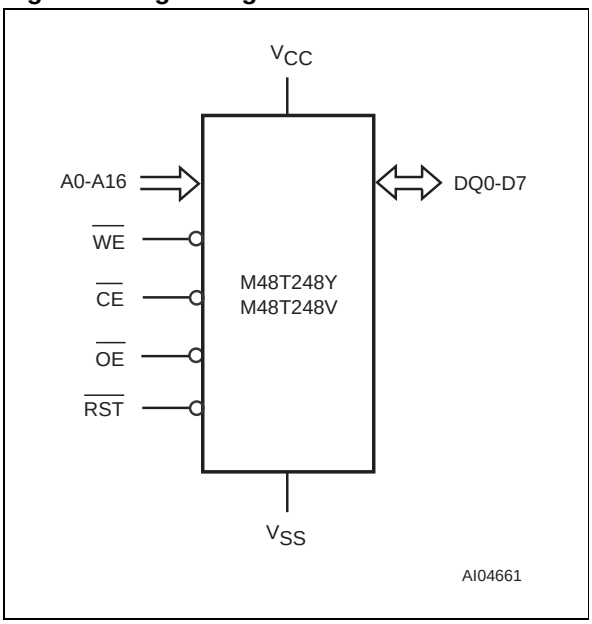



**Table 1. Signal Names**

| | |
|---|---|
| A0–A16 | Address Input |
| $\overline{RST}$ | Reset Input |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | WRITE Enable Input |
| DQ0–DQ7 | Data Inputs/Outputs |
| $V_{CC}$ | Supply Voltage Input |
| $V_{SS}$ | Ground |

**Figure 3. DIP Connections**

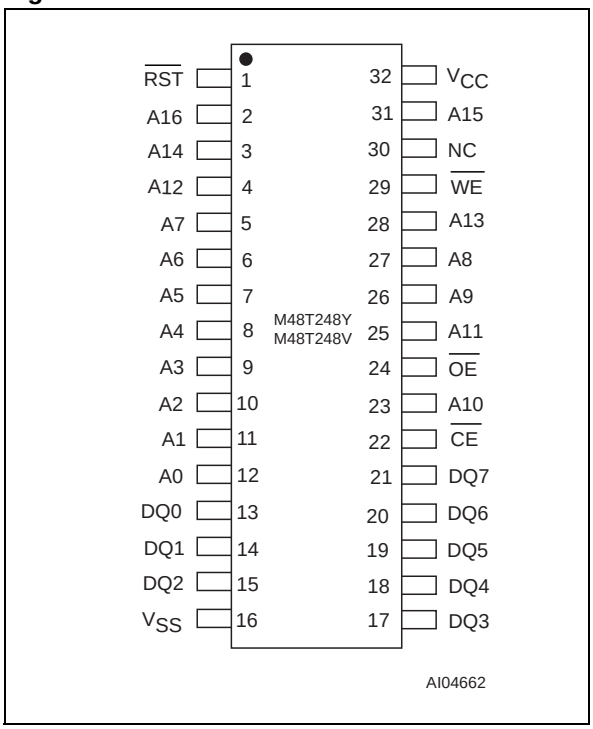
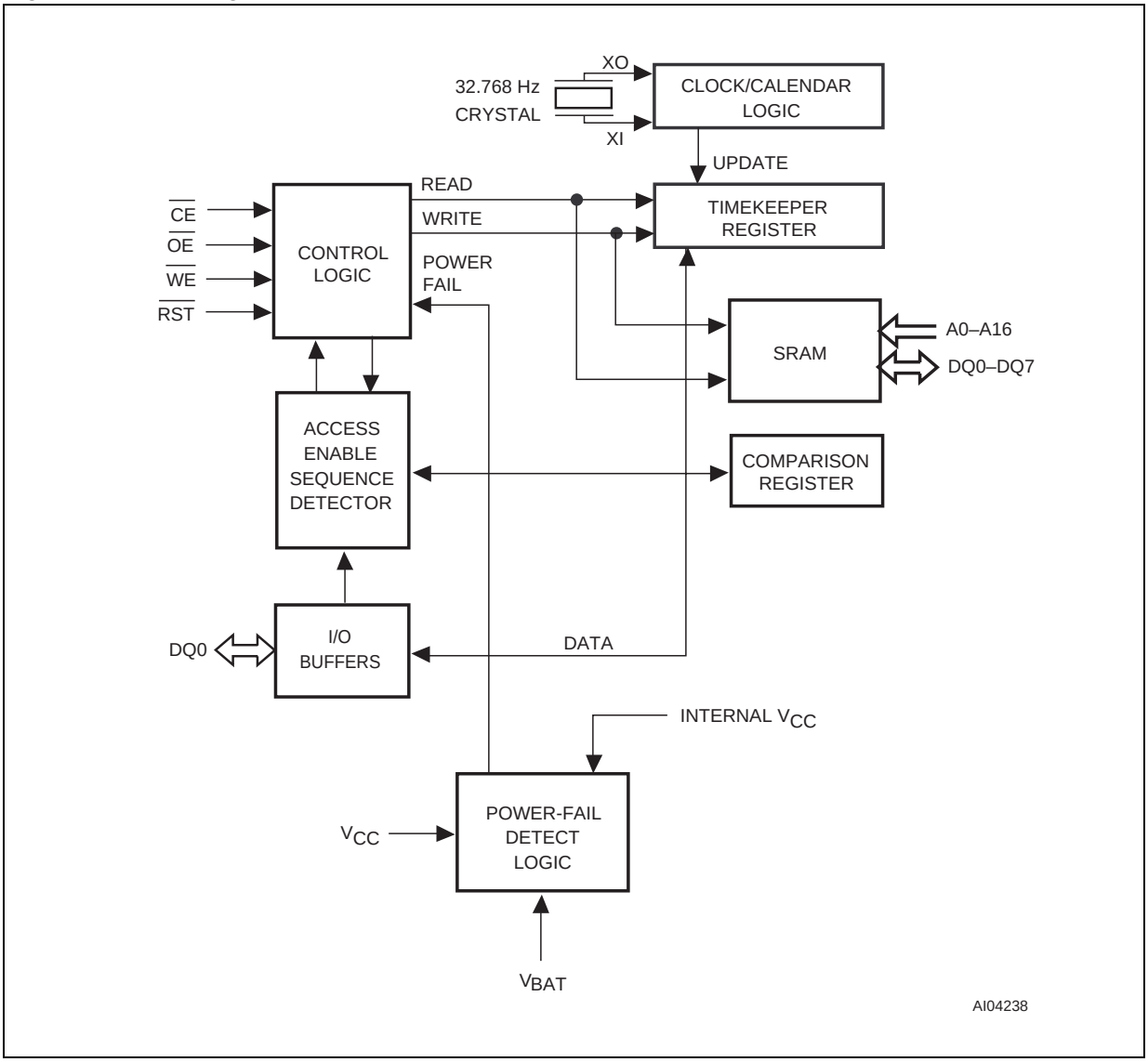


**Figure 4. Block Diagram**



## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_A$ | Operating Temperature | | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$, Oscillator Off) | | –40 to 85 | °C |
| $T_{SLD}$(1) | Lead Solder Temperature for 10 seconds | | 260 | °C |
| $V_{CC}$ | Supply Voltage (on any pin relative to Ground) | M48T248Y | –0.3 to +7.0 | V |
| | | M48T248V | –0.3 to +4.6 | V |
| $V_{IO}$ | Input or Output Voltages | | –0.3 to $V_{CC}$ + 0.3 | V |
| $I_O$ | Output Current | | 20 | mA |
| $P_D$ | Power Dissipation | | 1 | W |

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

***CAUTION!*** *Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up Mode.*

## DC AND AC PARAMETERS

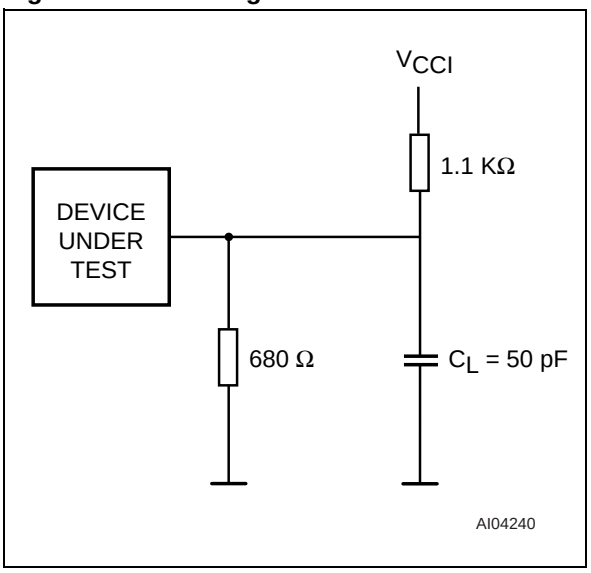
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. DC and AC Measurement Conditions**

| Parameter | M48T248Y | M48T248V |
|---|---|---|
| $V_{CC}$ Supply Voltage | 4.5 to 5.5V | 3.0 to 3.6V |
| Ambient Operating Temperature | 0 to 70°C | 0 to 70°C |
| Load Capacitance ($C_L$) | 100pF | 50pF |
| Input Rise and Fall Times | ≤ 5ns | ≤ 5ns |
| Input Pulse Voltages | 0 to 3V | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V | 1.5V |

Note: Output High Z is defined as the point where data is no longer driven (see Table 3, page 7).

**Figure 5. AC Testing Load Circuit**




Note: 50pF for M48T248V.

**Table 4. Capacitance**

| Symbol | Parameter[1,2] | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF |
| $C_{IO}$[3] | Input / Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V. Sampled only; not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs were deselected.

**Table 5. DC Characteristics**

| Sym | Parameter | Test Condition(1) | M48T248Y | | | M48T248V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –70 | | | –85 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{LI}$(2) | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | | | ±1 | µA |
| $I_{CC1}$ | Supply Current | | | | 85 | | | 50 | mA |
| $I_{CC2}$ | Supply Current (TTL Standby) | $\overline{CE} = V_{IH}$ | | 5 | 10 | | 5 | 7 | mA |
| $I_{CC3}$ | $V_{CC}$ Power Supply Current | $\overline{CE} = V_{CCI} – 0.2$ | | 3 | 5 | | 2 | 3 | mA |
| $V_{IL}$(3) | Input Low Voltage | | –0.3 | | 0.8 | –0.3 | | 0.6 | V |
| $V_{IH}$(3) | Input High Voltage | | 2.2 | | $V_{CC}$ + 0.3 | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | | 0.4 | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1.0 mA | 2.4 | | | 2.4 | | | V |
| $V_{PFD}$(3) | Power Fail Deselect | | 4.25 | 4.37 | 4.50 | 2.80 | 2.86 | 2.97 | V |
| $V_{SO}$(3) | Battery Back-up Switchover | | | $V_{BAT}$ | | | 2.5 | | V |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.
3. All voltages are referenced to Ground.

## OPERATION MODES

**Table 6. Operating Modes**

| Mode | $V_{CC}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | DQ7-DQ0 | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.5V to 5.5V or 3.0V to 3.6V | $V_{IH}$ | X | X | High-Z | Standby |
| WRITE | | $V_{IL}$ | X | $V_{IL}$ | $D_{IN}$ | Active |
| READ | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Active |
| READ | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High-Z | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min)(1) | X | X | X | High-Z | CMOS Standby |
| Deselect | $\leq V_{SO}$(1) | X | X | X | High-Z | Battery Back-Up |

Note: X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage
1. See Table 9, page 14 for details.

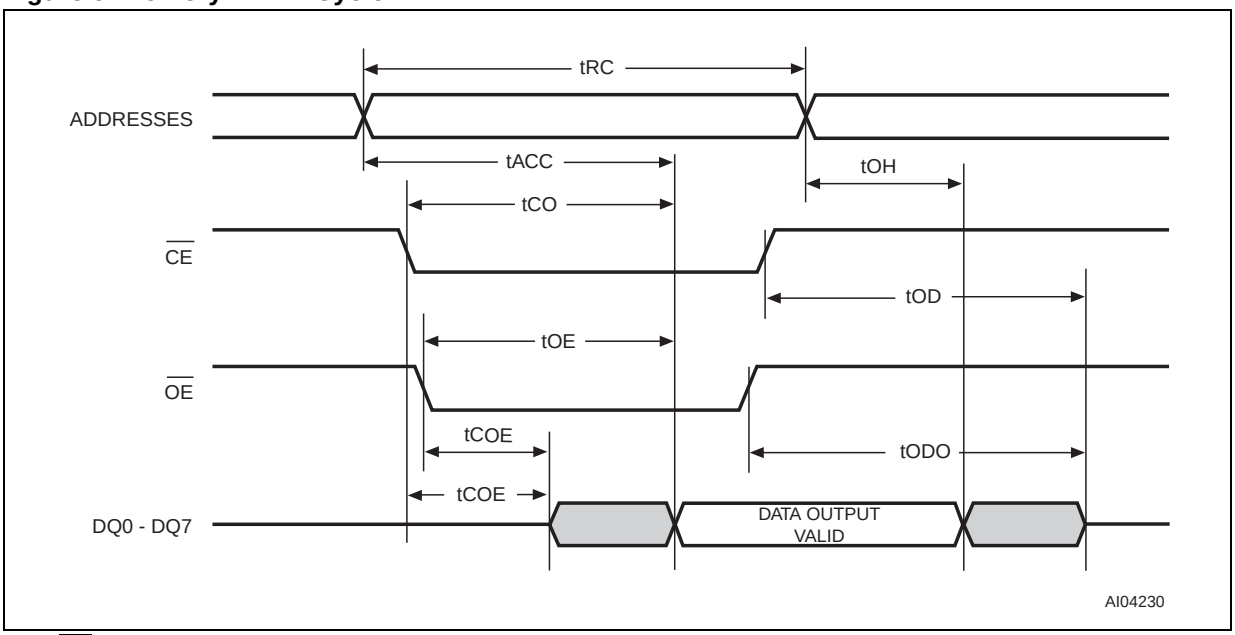
### READ

A READ cycle executes whenever WRITE Enable ($\overline{WE}$) is high and Chip Enable ($\overline{CE}$) is low (see Figure 6). The distinct address defined by the 19 address inputs (A0-A18) specifies which of the 512K bytes of data is to be accessed. Valid data will be accessed by the eight data output drivers within the specified Access Time ($t_{ACC}$) after the last address input signal is stable, the $\overline{CE}$ and $\overline{OE}$ access times, and their respective parameters are satisfied. When $\overline{CE}$ $t_{ACC}$ and $\overline{OE}$ $t_{ACC}$ are not satisfied, then data access times must be measured from the more recent $\overline{CE}$ and $\overline{OE}$ signals, with the limiting parameter being $t_{CO}$ (for $\overline{CE}$) or $t_{OE}$ (for $\overline{OE}$) instead of address access.

### WRITE

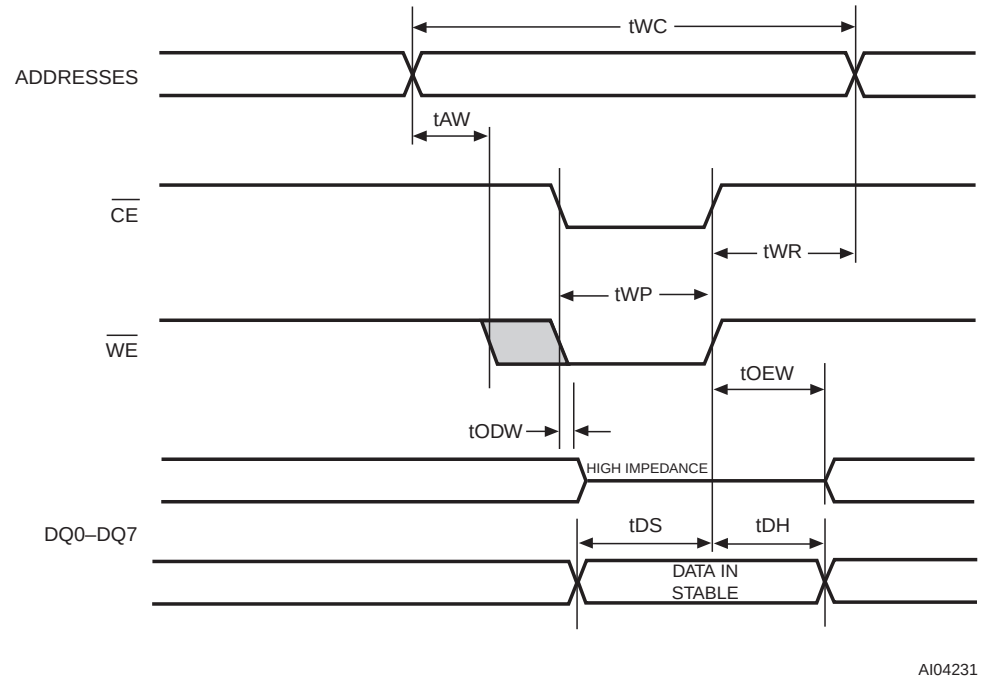
WRITE Mode (see Figure 7, page 10 and Figure 8, page 11) occurs whenever $\overline{CE}$ and $\overline{WE}$ signals are low (after address inputs are stable). The most recent falling edge of $\overline{CE}$ and $\overline{WE}$ will determine when the WRITE cycle begins (the earlier, rising edge of $\overline{CE}$ or $\overline{WE}$ determines cycle termination). All address inputs must be kept stable throughout the WRITE cycle. $\overline{WE}$ must be high (inactive) for a minimum recovery time ($t_{WR}$) before a subsequent cycle is initiated. The $\overline{OE}$ control signal should be kept high (inactive) during the WRITE cycles to avoid bus contention. If $\overline{CE}$ and $\overline{OE}$ are low (active), $\overline{WE}$ will disable the outputs for Output Data WRITE Time ($t_{ODW}$) from its falling edge.

**Figure 6. Memory READ Cycle**



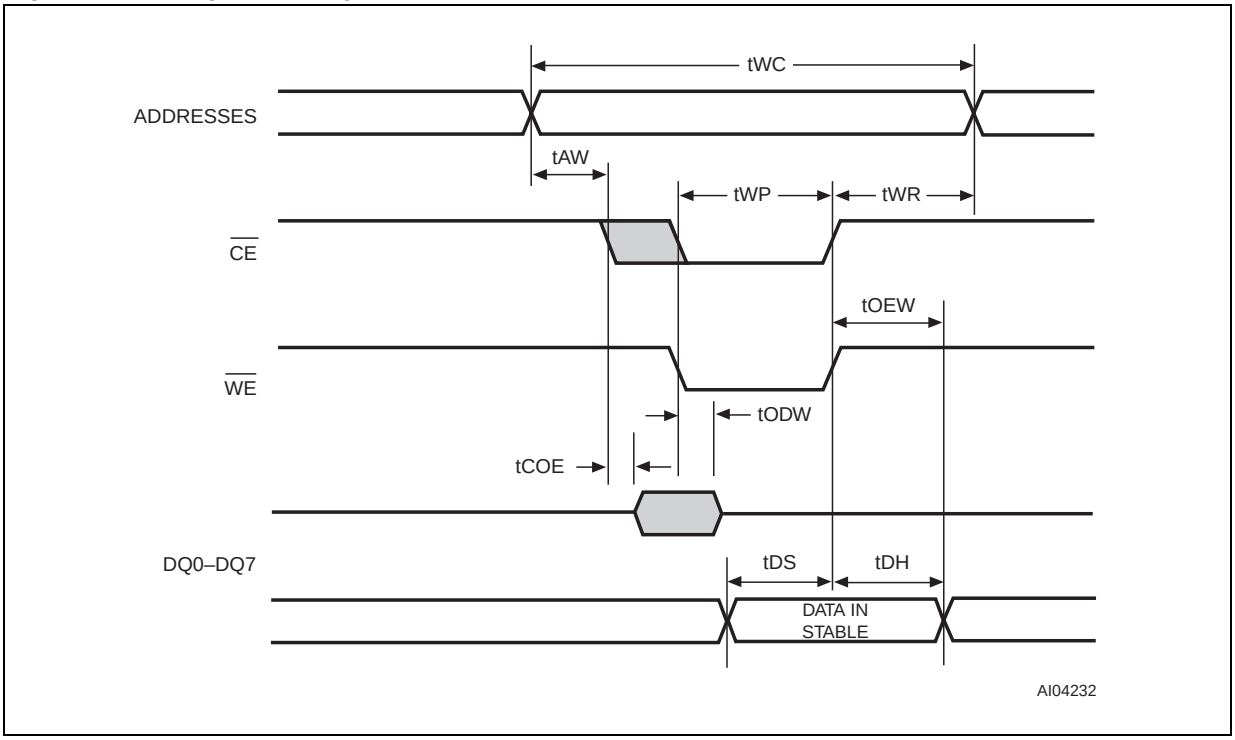

Note: $\overline{WE}$ is high for a READ cycle.

**Figure 7. Memory WRITE Cycle 1**




Note: 1. $\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during a WRITE cycle, the output buffers remain in a high impedance state.
2. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in WRITE Cycle 1, the output buffers remain in a high impedance state during this period.
3. If the $\overline{CE}$ high transition occurs simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.

**Figure 8. Memory WRITE Cycle 2**




Note: 1. $\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during a WRITE cycle, the output buffers remain in a high impedance state.
2. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

**Table 7. Memory AC Characteristics, M48T248Y**

| Symbol | | Parameter[1] | M48T248Y–70 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | READ Cycle Time | 70 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Access Time | | 70 | ns |
| $t_{ELQV}$ | $t_{CO}$ | Chip Enable Low to Output Valid | | 70 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | 35 | ns |
| $t_{ELQX}$ $t_{GLQX}$ | $t_{COE}$ | Chip Enable or Output Enable Low to Output Transition | 5 | | ns |
| $t_{AXQX}$ | tOH | Output Hold from Address Change | 5 | | ns |
| $t_{EHQZ}$ $t_{GHQZ}$ | $t_{OD}$[2] | Chip Enable or Output Enable High to Output Hi-Z | | 25 | ns |
| $t_{WLQZ}$ | $t_{ODW}$[2] | Output Hi-Z from $\overline{WE}$ | | 25 | ns |
| $t_{AVAV}$ | $t_{WC}$ | WRITE Cycle Time | 70 | | ns |
| $t_{WLWH}$ $t_{ELEH}$ | $t_{WP}$[3] | $\overline{WE}$, $\overline{CE}$ Pulse Width | 50 | | ns |
| $t_{AVEL}$ $t_{AVWL}$ | $t_{AW}$ | Address Setup Time | 0 | | ns |
| $t_{EHAX}$ | $t_{WR1}$ | WRITE Recovery Time | 15 | | ns |
| $t_{WHAX}$ | $t_{WR2}$ | Address Hold Time from $\overline{WE}$ | 0 | | ns |
| $t_{WHQX}$ | $t_{OEW}$ | Output Active from $\overline{WE}$ | 5 | | ns |
| $t_{DVEH}$ $t_{DVWH}$ | $t_{DS}$[4] | Data Setup Time | 30 | | ns |
| $t_{WHDX}$ | $t_{DH1}$[4] | Data Hold Time from $\overline{WE}$ | 0 | | ns |
| $t_{EHDX}$ | $t_{DH2}$[4] | Data Hold Time from $\overline{CE}$ | 10 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. These parameters are sampled with a 5 pF load are not 100% tested.
3. $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$ and $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

**Table 8. Memory AC Characteristics, M48T248V**

| Symbol | | Parameter[1] | M48T248V–85 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | READ Cycle Time | 85 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Access Time | | 85 | ns |
| $t_{ELQV}$ | $t_{CO}$ | Chip Enable Low to Output Valid | | 85 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | 45 | ns |
| $t_{ELQX}$ $t_{GLQX}$ | $t_{COE}$ | Chip Enable or Output Enable Low to Output Transition | 5 | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold from Address Change | 5 | | ns |
| $t_{EHQZ}$ $t_{GHQZ}$ | $t_{OD}$[2] | Chip Enable or Output Enable High to Output Hi-Z | | 35 | ns |
| $t_{WLQZ}$ | $t_{ODW}$[2] | Output Hi-Z from $\overline{WE}$ | | 30 | ns |
| $t_{AVAV}$ | $t_{WC}$ | WRITE Cycle Time | 85 | | ns |
| $t_{WLWH}$ | $t_{WP1}$[3] | WRITE Enable Pulse Width | 65 | | ns |
| $t_{ELEH}$ | $t_{WP2}$ | Chip Enable Pulse Width | 75 | | ns |
| $t_{AVEL}$ $t_{AVWL}$ | $t_{AW}$ | Address Setup Time | 0 | | ns |
| $t_{EHAX}$ | $t_{WR1}$[4] | WRITE Recovery Time | 15 | | ns |
| $t_{WHAX}$ | $t_{WR2}$[4] | Address Hold Time from $\overline{WE}$ | 5 | | ns |
| $t_{WHQX}$ | $t_{OEW}$ | Output Active from $\overline{WE}$ | 5 | | ns |
| $t_{DVEH}$ $t_{DVWH}$ | $t_{DS}$[5] | Data Setup Time | 35 | | ns |
| $t_{WHDX}$ | $t_{DH1}$[5] | Data Hold Time from $\overline{WE}$ | 0 | | ns |
| $t_{EHDX}$ | $t_{DH2}$[5] | Data Hold Time from $\overline{CE}$ | 15 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. These parameters are sampled with a 5 pF load are not 100% tested.
3. $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
5. $t_{DH}$ and $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

### Data Retention Mode

Data can be read or written only when $V_{CC}$ is greater than $V_{PFD}$. When $V_{CC}$ is below $V_{PFD}$ (the point at which write protection occurs), the clock registers and the SRAM are blocked from any access. When $V_{CC}$ falls below the Battery Switch Over threshold ($V_{SO}$), the device is switched from $V_{CC}$ to battery backup ($V_{BAT}$). RTC operation and SRAM data are maintained via battery backup until power is stable. All control, data, and address signals must be powered down when $V_{CC}$ is powered down.

The lithium power source is designed to provide power for RTC activity as well as RTC and RAM data retention when $V_{CC}$ is absent or unstable. The capability of this source is sufficient to power the device continuously for the life of the equipment into which it has been installed. For specification purposes, life expectancy is ten (10) years at 25°C with the internal oscillator running without $V_{CC}$. Each unit is shipped with its energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than $V_{PFD}$, the energy source is enabled for battery backup operation. The actual life expectancy will be much longer if no battery energy is used (e.g., when $V_{CC}$ is present).

**Figure 9. Power Down/Up Mode AC Waveforms**

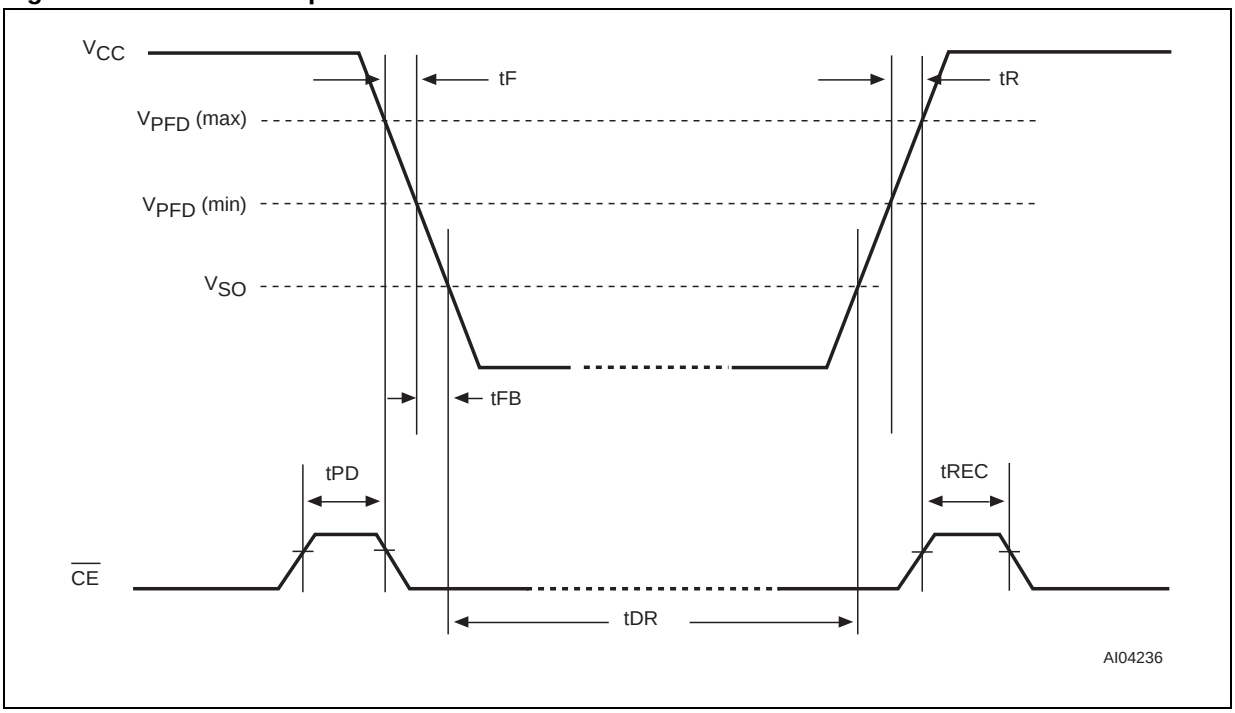



**Table 9. Power Down/Up Trip Points DC Characteristics**

| Symbol | Parameter[1] | Min | Max | Unit |
|---|---|---|---|---|
| $t_{REC}$ | $V_{PFD}$ (max) to $\overline{CE}$ low | 1.5 | 2.5 | ms |
| $t_F$ | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | 300 | | µs |
| $t_{FB}$ | $V_{PFD}$ (min) to $V_{SO}$ $V_{CC}$ Fall Time | 10 | | µs |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | 0 | | µs |
| $t_{PD}$ | $\overline{CE}$ High to Power-Fail | 0 | | µs |
| $t_{DR}$[2] | Expected Data Retention Time | 10 | | Years |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. At 25°C, $V_{CC}$ = 0V; the expected $t_{DR}$ is defined as cumulative time in the absence of $V_{CC}$ with the clock oscillator running.

## PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition of a serial bit-stream of 64 bits which must be matched by executing 64 consecutive WRITE cycles containing the proper data on DQ0.

All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 READ or WRITE cycles either extract or update data in the clock while disabling the memory.

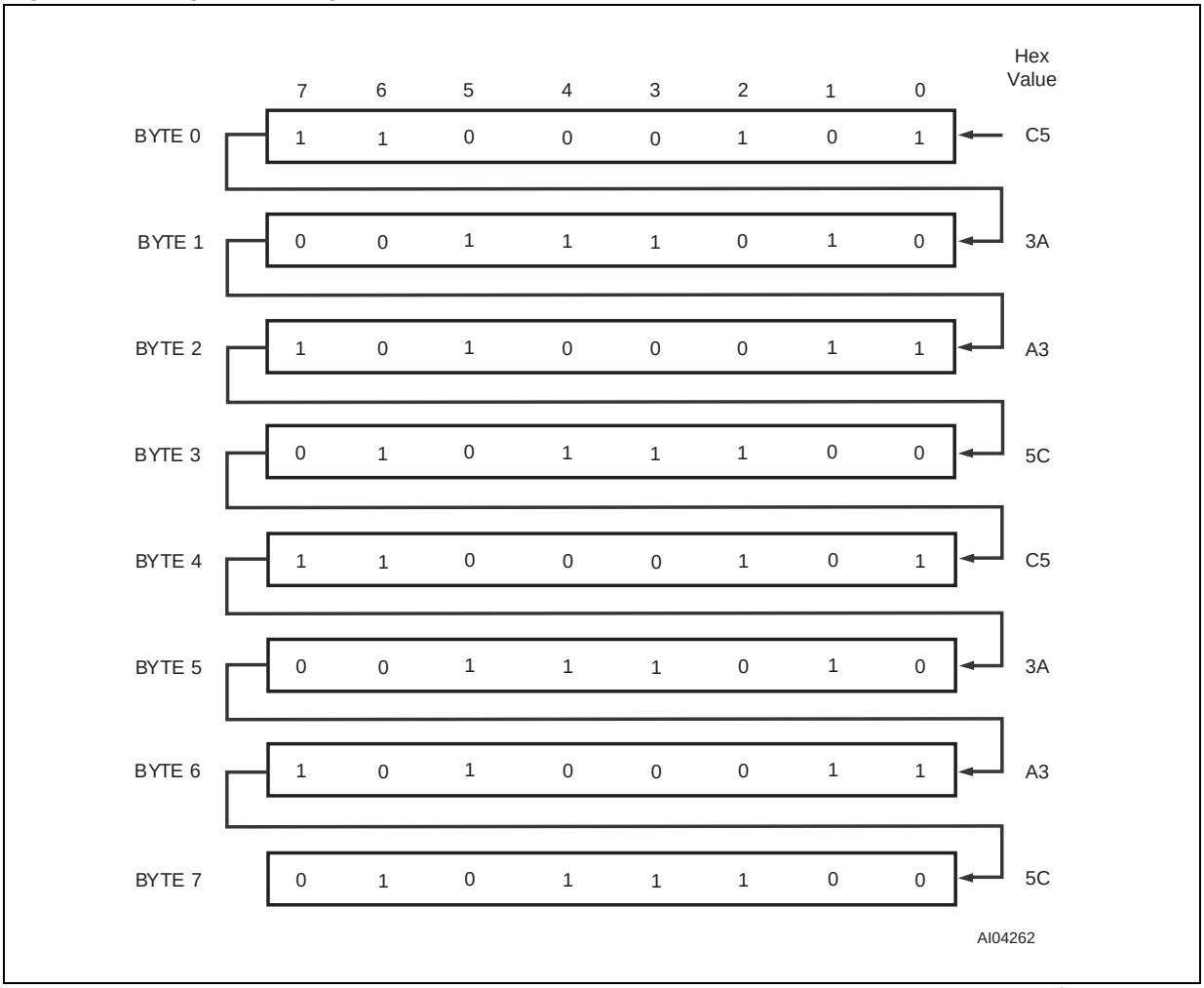
Data transfer to and from the timekeeping function is accomplished with a serial bit-stream under control of Chip Enable (CE), Output Enable (OE), and WRITE Enable (WE). Initially, a READ cycle using the CE and OE control of the clock starts the pattern recognition sequence by moving the pointer to the first bit of the 64-bit comparison register (see Figure 10, page 16).

Next, 64 consecutive WRITE cycles are executed using the CE and WE control of the device. These 64 WRITE cycles are used only to gain access to the clock. Therefore, any address to the memory is acceptable. However, the WRITE cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad.

When the first WRITE cycle is executed, it is compared to Bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next WRITE cycle.

If a match is not found, the pointer does not advance and all subsequent WRITE cycles are ignored. If a READ cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 WRITE cycles as described above until all of the bits in the comparison register have been matched. With a correct match for 64-bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the OE pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with CE cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

**Figure 10. Comparison Register Definition**




Note: The odds of this pattern being accidentally duplicated and sending aberrant entries to the RTC is less than 1 in $10^{19}$. This pattern is sent to the clock LSB to MSB.

### Clock Register Information

Clock information is contained in eight registers of 8 bits, each of which is sequentially accessed one (1) bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the clock registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These READ/WRITE registers are defined in the clock register map (see Table 10).

Data contained in the clock registers is in Binary Coded Decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with Bit 0 of Register 0 and ending with Bit 7 of Register 7.

### Clock Accuracy

The RTC is guaranteed to keep time accuracy to with ±1 minute per month at 25°C. The clock is factory-tuned with special calibration elements, and does not require additional calibration. Moderate temperature deviation will have a negligible effect in most applications.

### AM-PM/12/24 Mode

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When it is high, the 12-hour mode is selected. In the 12-hour mode, Bit 5 is the AM/PM bit with the logic high being “PM.” In the 24-hour mode, Bit 5 is the second 10-hour bit (20-23 hours).

### Oscillator and Reset Bits

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin input. When the reset bit is set to logic '1,' the Reset Input pin is ignored. When the reset bit logic is set to '0,' a low input on the reset pin will cause the device to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic '0,' the oscillator turns on and the RTC/calendar begins to increment.

### Zero Bits

Registers 1, 2, 3, 4, 5, and 6 contain one (1) or more bits that will always read logic '0.' When writing to these locations, either a logic '1' or '0' is acceptable.

**Table 10. Phantom Clock Register Map**

| | | | | | | | | | Function/Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Register** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | | |
| 0 | 0.1 Seconds | | | | 0.01 Seconds | | | | Seconds | 00-99 |
| 1 | 0 | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 2 | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 3 | 12/24 | 0 | 10 / A/P | Hrs | Hours (24 Hour Format) | | | | Hours | 01-12/ 00-23 |
| 4 | 0 | 0 | $\overline{OSC}$ | $\overline{RST}$ | 0 | Day of the Week | | | Day | 01-7 |
| 5 | 0 | 0 | 10 date | | Date: Day of the Month | | | | Date | 01-31 |
| 6 | 0 | 0 | 0 | 10M | Month | | | | Month | 01-12 |
| 7 | 10 Years | | | | Year | | | | Year | 00-99 |

Keys: A/P = AM/PM Bit
12/24 = 12 or 24-hour mode Bit
$\overline{OSC}$ = Oscillator Bit
$\overline{RST}$ = Reset Bit
0 = Must be set to '0'

**Figure 11. Phantom Clock READ Cycle**

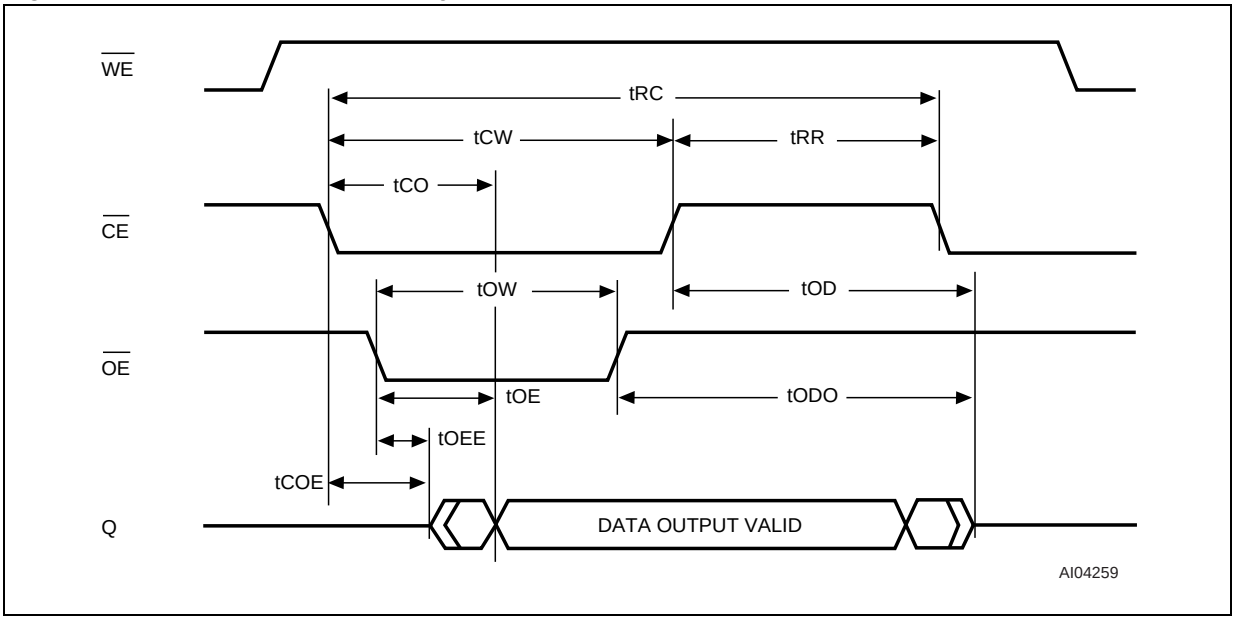



**Figure 12. Phantom Clock WRITE Cycle**

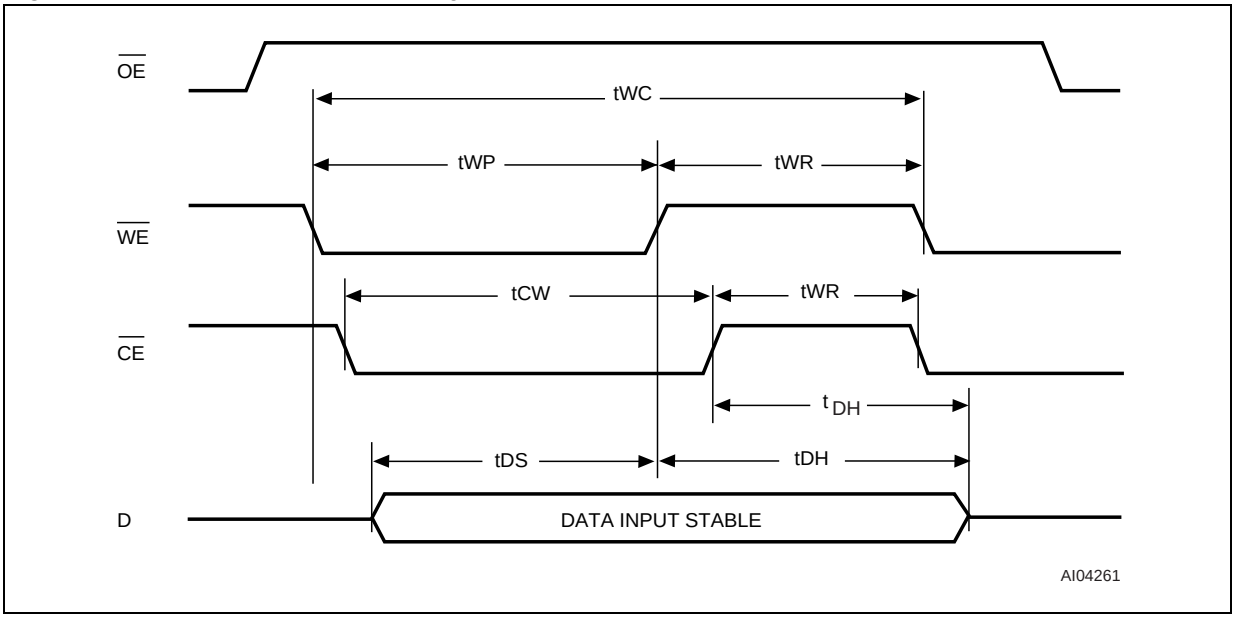



**Figure 13. Phantom Clock Reset**

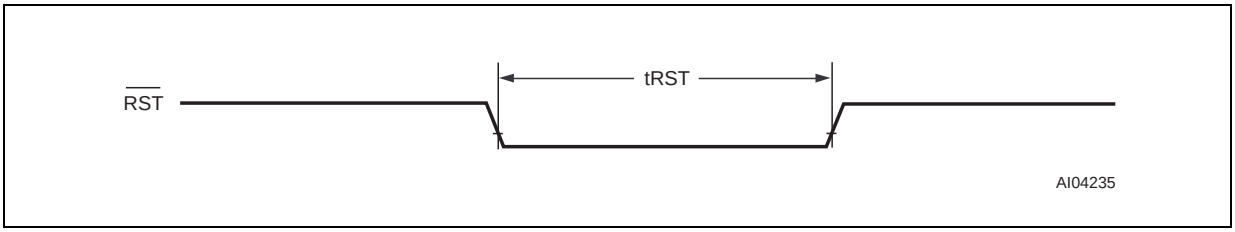


**Table 11. Phantom Clock AC Characteristics (M48T248Y)**

| Symbol | | Parameter[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{RC}$ | READ Cycle Time | 65 | | | ns |
| $t_{ELQV}$ | $t_{CO}$ | $\overline{CE}$ Access Time | | | 55 | ns |
| $t_{GLQV}$ | $t_{OE}$ | $\overline{OE}$ Access Time | | | 55 | ns |
| $t_{ELQX}$ | $t_{COE}$ | $\overline{CE}$ to Output Low Z | 5 | | | ns |
| $t_{GLQX}$ | $t_{OEE}$ | $\overline{OE}$ to Output Low Z | 5 | | | ns |
| $t_{EHQZ}$ | $t_{OD}$[2] | $\overline{CE}$ to Output High Z | | | 25 | ns |
| $t_{GHQZ}$ | $t_{ODO}$[2] | $\overline{OE}$ to Output High Z | | | 25 | ns |
| | $t_{RR}$ | READ Recovery | 10 | | | ns |
| $t_{AVAV}$ | $t_{WC}$ | WRITE Cycle Time | 65 | | | ns |
| $t_{WLWH}$ | $t_{WP}$[3] | WRITE Pulse Width | 55 | | | ns |
| $t_{EHAX}$ | $t_{WR}$[4] | WRITE Recovery | 10 | | | ns |
| $t_{DVEH}$ | $t_{DS}$[5] | Data Setup Time | 30 | | | ns |
| $t_{WHDX}$ | $t_{DH1}$[5] | Data Hold Time from $\overline{WE}$ | 0 | | | ns |
| $t_{EHDX}$ | $t_{DH2}$[5] | Data Hold Time from $\overline{CE}$ | 0 | | | ns |
| $t_{ELEH}$ | $t_{CW}$ | $\overline{CE}$ Pulse Width | 55 | | | ns |
| | $t_{RST}$ | $\overline{RST}$ Pulse Width | 65 | | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. These parameters are sampled with a 5 pF load and are not 100% tested.
3. $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
5. $t_{DH}$ and $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

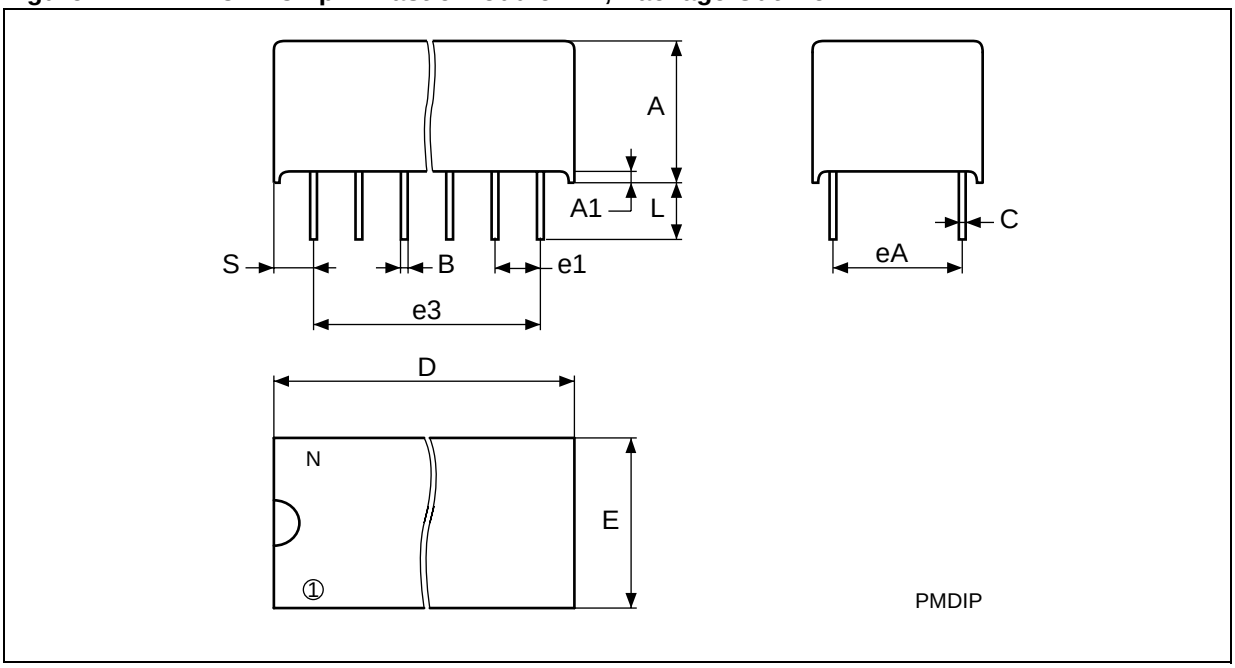
**Table 12. Phantom Clock AC Characteristics (M48T248V)**

| Symbol | | Parameter[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{RC}$ | READ Cycle Time | 85 | | | ns |
| $t_{ELQV}$ | $t_{CO}$ | $\overline{CE}$ Access Time | | | 85 | ns |
| $t_{GLQV}$ | $t_{OE}$ | $\overline{OE}$ Access Time | | | 85 | ns |
| $t_{ELQX}$ | $t_{COE}$ | $\overline{CE}$ to Output Low Z | 5 | | | ns |
| $t_{GLQX}$ | $t_{OEE}$ | $\overline{OE}$ to Output Low Z | 5 | | | ns |
| $t_{EHQZ}$ | $t_{OD}$[2] | $\overline{CE}$ to Output High Z | | | 30 | ns |
| $t_{GHQZ}$ | $t_{ODO}$[2] | $\overline{OE}$ to Output High Z | | | 30 | ns |
| | $t_{RR}$ | READ Recovery | 20 | | | ns |
| $t_{AVAV}$ | $t_{WC}$ | WRITE Cycle Time | 85 | | | ns |
| $t_{WLWH}$ | $t_{WP}$[3] | WRITE Pulse Width | 60 | | | ns |
| $t_{EHAX}$ | $t_{WR}$[4] | WRITE Recovery | 20 | | | ns |
| $t_{DVEH}$ | $t_{DS}$[5] | Data Setup Time | 35 | | | ns |
| $t_{WHDX}$ | $t_{DH1}$[5] | Data Hold Time from $\overline{WE}$ | 0 | | | ns |
| $t_{EHDX}$ | $t_{DH2}$[5] | Data Hold Time from $\overline{CE}$ | 0 | | | ns |
| $t_{ELEH}$ | $t_{CW}$ | $\overline{CE}$ Pulse Width | 65 | | | ns |
| | $t_{RST}$ | $\overline{RST}$ Pulse Width | 85 | | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. These parameters are sampled with a 5 pF load and are not 100% tested.
3. $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
5. $t_{DH}$ and $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

## PACKAGE MECHANICAL INFORMATION

**Figure 14. PMDIP32 – 32-pin Plastic Module DIP, Package Outline**




Note: Drawing is not to scale.

**Table 13. PMDIP32 – 32-pin Plastic Module DIP, Package Mechanical Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 9.27 | 9.52 | | 0.365 | 0.375 |
| A1 | | 0.38 | – | | 0.015 | – |
| B | | 0.43 | 0.59 | | 0.017 | 0.023 |
| C | | 0.20 | 0.33 | | 0.008 | 0.013 |
| D | | 42.42 | 43.18 | | 1.670 | 1.700 |
| E | | 18.03 | 18.80 | | 0.710 | 0.740 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | | 34.29 | 41.91 | | 1.350 | 1.650 |
| eA | | 14.99 | 16.00 | | 0.590 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| S | | 1.91 | 2.79 | | 0.075 | 0.110 |
| N | 32 | | | 32 | | |

## PART NUMBERING

**Table 14. Ordering Information Example**

Example: M48T 248Y –70 PM 1 TR

**Device Type**

M48T

**Supply Voltage and Write Protect Voltage**

248Y = $V_{CC}$ = 4.5 to 5.5V; $V_{PFD}$ = 4.25 to 4.50V

248V = $V_{CC}$ = 3.0 to 3.6V; $V_{PFD}$ = 2.80 to 2.97V

**Speed**

–70 = 70ns (M48T248Y)

–85 = 85ns (M48T248V)

**Package**

PM = PMDIP32

**Temperature Range**

1 = 0 to 70°C

**Shipping Method for SOIC**

blank = Tubes

TR = Tape & Reel

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

## REVISION HISTORY

**Table 15. Document Revision History**

| Date | Rev. # | Revision Details |
|---|---|---|
| June 2001 | 1.0 | First Issue |
| 28-Mar-03 | 2.0 | v2.2 template applied; test condition updated (Table 9) |