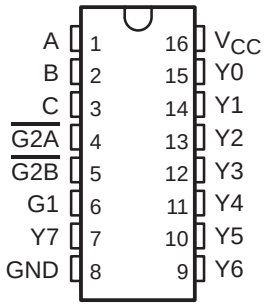
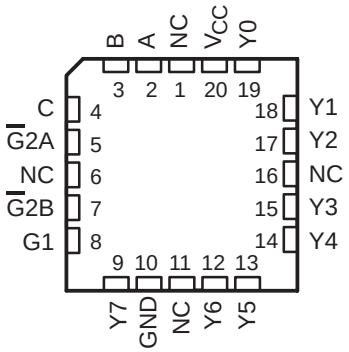
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Package, and DIPs (J)**

**SN54LVC138A . . . J OR W PACKAGE**
**SN74LVC138A . . . D, DB, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LVC138A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The SN54LVC138A 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V $V_{CC}$ operation and the SN74LVC138A 3-line to 8-line decoder/demultiplexer is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The ’LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

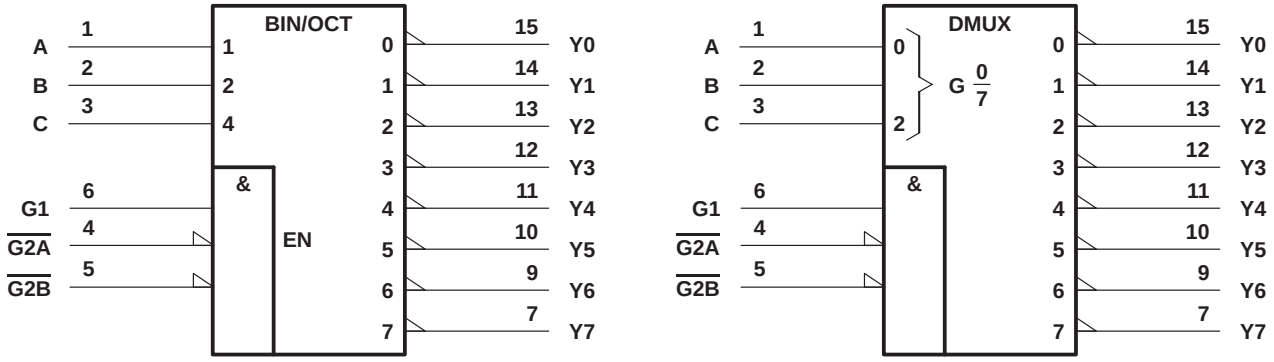
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC138A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVC138A is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

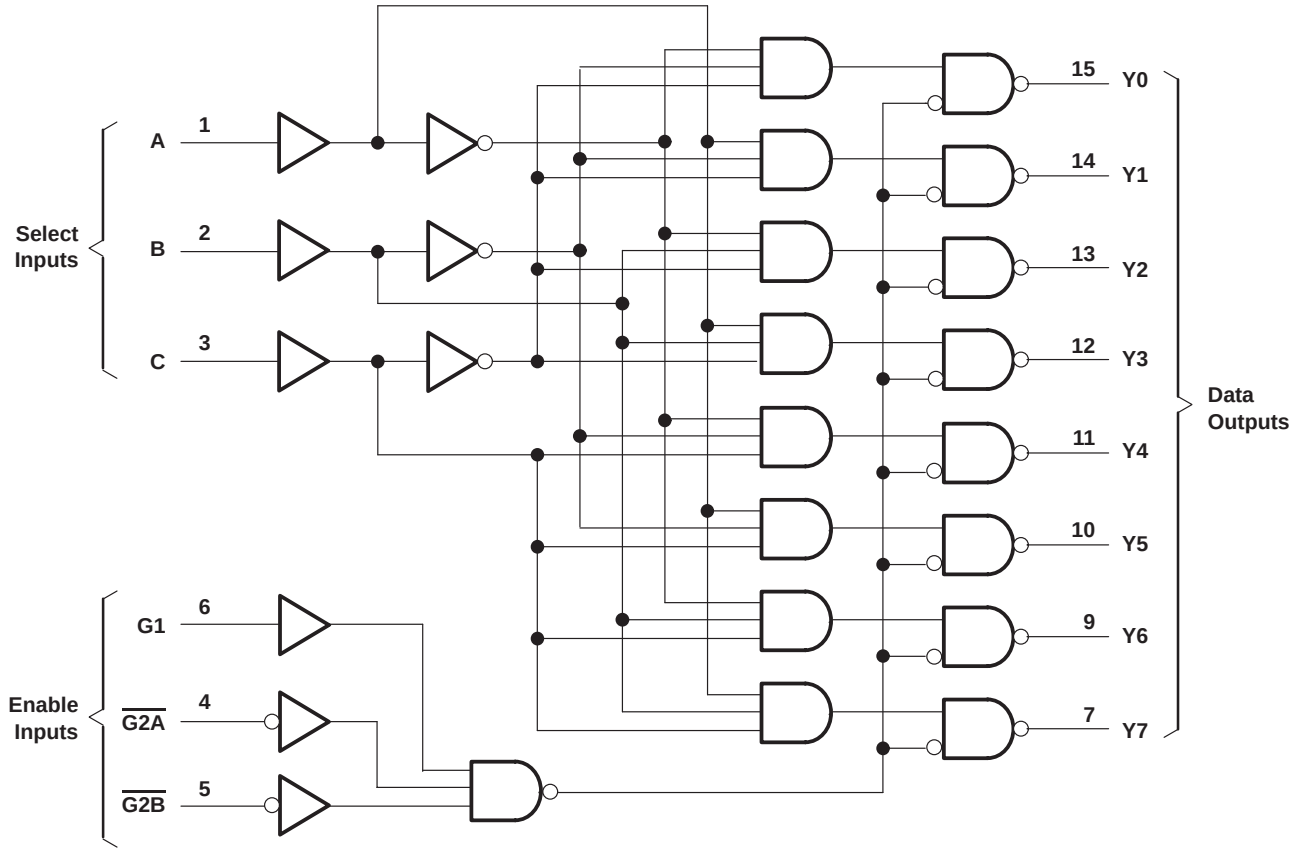
| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, DB, J, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
PW package . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

| | | | SN54LVC138A | | SN74LVC138A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 10 | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LVC138A | | | SN74LVC138A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 μA | 1.65 V to 3.6 V | | | | $V_{CC}$–0.2 | | | V |
| | | 2.7 V to 3.6 V | $V_{CC}$–0.2 | | | | | | |
| | $I_{OH}$ = –4 mA | 1.65 V | | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | 2.3 V | | | | 1.7 | | | |
| | $I_{OH}$ = –12 mA | 2.7 V | 2.2 | | | 2.2 | | | |
| | | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | 3 V | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | 1.65 V to 3.6 V | | | | | | 0.2 | V |
| | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | $I_{OL}$ = 4 mA | 1.65 V | | | | | | 0.45 | |
| | $I_{OL}$ = 8 mA | 2.3 V | | | | | | 0.7 | |
| | $I_{OL}$ = 12 mA | 2.7 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 3.6 V | | | ±5 | | | ±5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 10 | | | 10 | μA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V | | | 500 | | | 500 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 5 | | | 5 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC138A | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B or C | Y | | 7.9 | 1 | 6.7 | ns |
| | $\overline{G2A}$ or $\overline{G2B}$ | | | 7.4 | 1 | 6.5 | |
| | G1 | | | 6.4 | 1 | 5.8 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

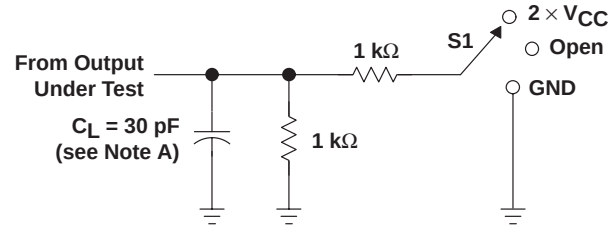
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC138A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | |
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B or C | Y | 15.9 | 1 | 9.9 | | 7.9 | 1 | 6.7 | ns |
| | $\overline{G2A}$ or $\overline{G2B}$ | | 15.4 | 1 | 9.4 | | 7.4 | 1 | 6.5 | |
| | G1 | | 14.4 | 1 | 8.4 | | 6.4 | 1 | 5.8 | |
| $t_{sk(o)}$‡ | | | | | | | | | 1 | ns |

‡ Skew between any two outputs of the same package switching in the same direction

## operating characteristics, $T_A$ = 25°C

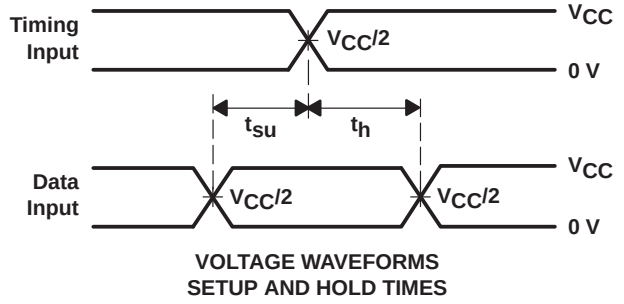
| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 25 | 26 | 27 | pF |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V

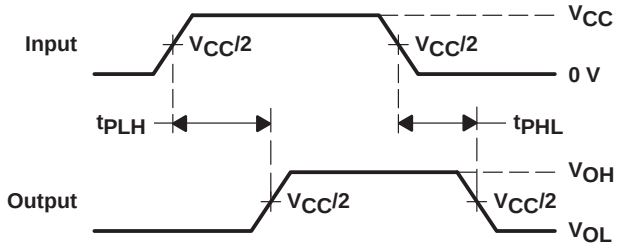



LOAD CIRCUIT

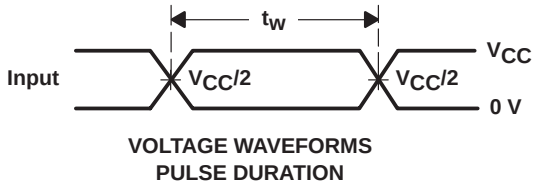
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |



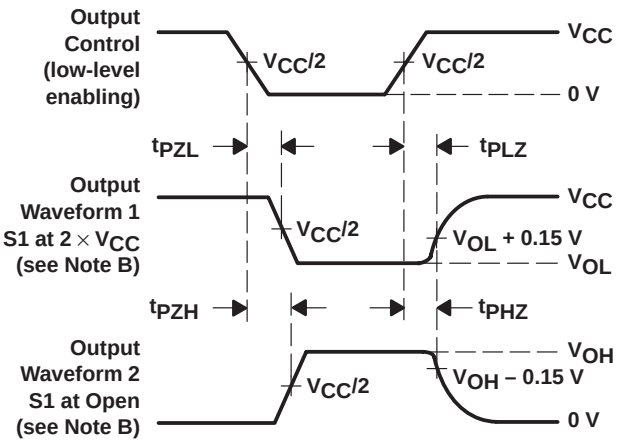

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

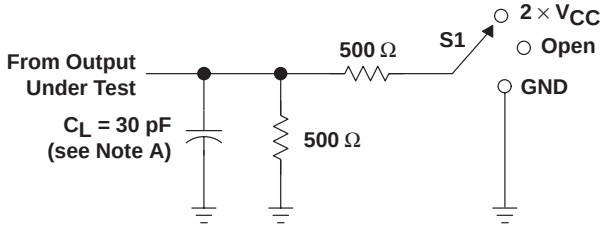



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

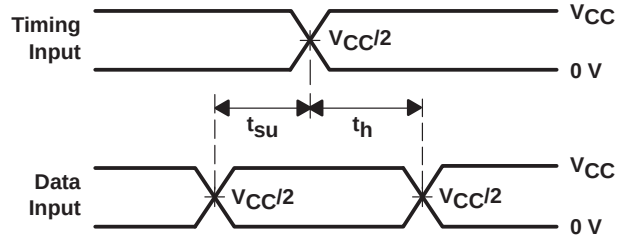
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

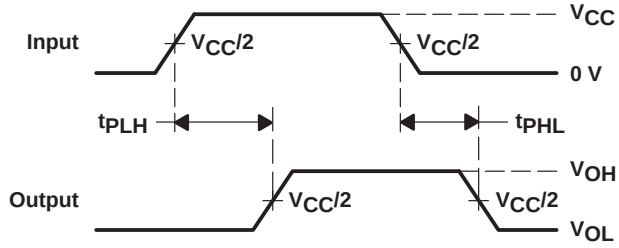



| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |

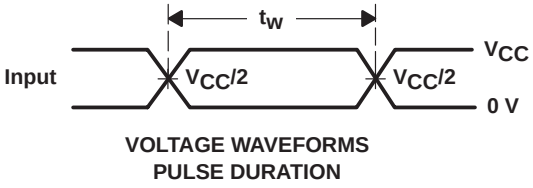
LOAD CIRCUIT



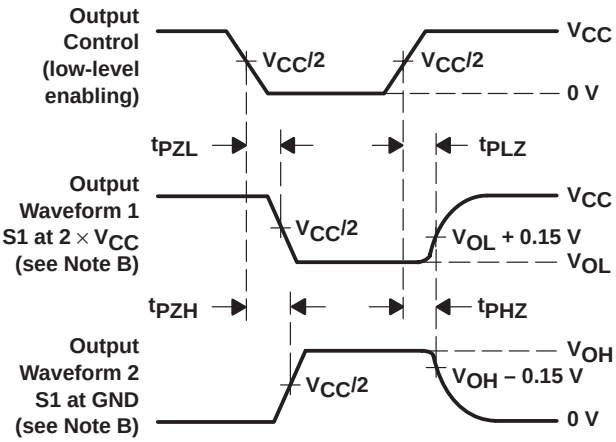

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

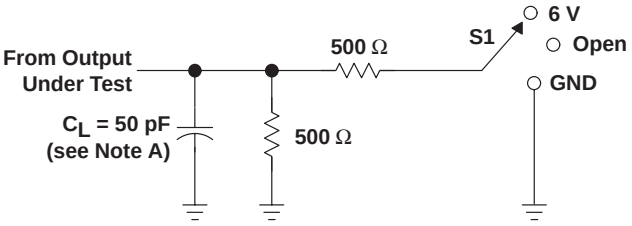



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

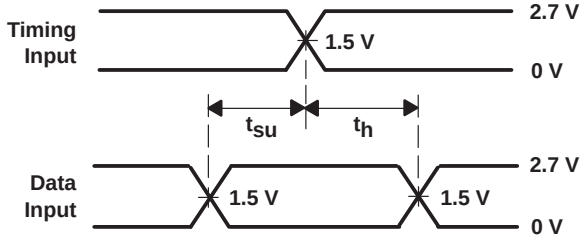
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

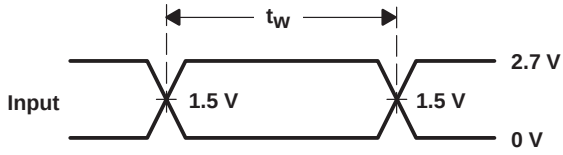



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

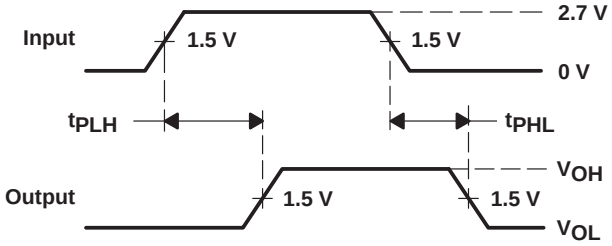
LOAD CIRCUIT



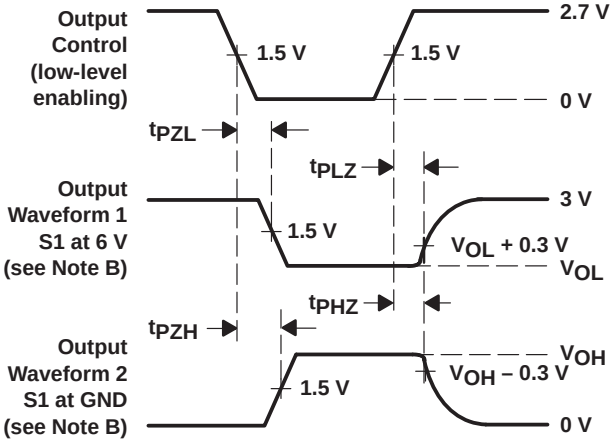

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

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