SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS362D – SEPTEMBER 1999 – REVISED MAY 2001

- **Four ('391), Eight ('389) or Sixteen ('387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates† up to 630 Mbps With Very Low Radiation (EMI)**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Times Less Than 2.9 ns**
- **Output Skew Is Less Than 150 ps**
- **Part-to-Part Skew Is Less Than 1.5 ns**
- **35-mW Total Power Dissipation in Each Driver Operating at 200 MHz**
- **Driver Is High Impedance When Disabled or With $V_{CC} < 1.5$ V**
- **SN65' Version Bus-Pin ESD Protection Exceeds 15 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**
- **Low-Voltage TTL (LVTTL) Logic Inputs Are 5-V Tolerant**

'LVDS389
DBT PACKAGE
(TOP VIEW)

GND	1		38	A1Y
V_{CC}	2		37	A1Z
GND	3		36	A2Y
ENA	4		35	A2Z
A1A	5		34	A3Y
A2A	6		33	A3Z
A3A	7		32	A4Y
A4A	8		31	A4Z
GND	9		30	NC
V_{CC}	10		29	NC
GND	11		28	NC
B1A	12		27	B1Y
B2A	13		26	B1Z
B3A	14		25	B2Y
B4A	15		24	B2Z
ENB	16		23	B3Y
GND	17		22	B3Z
V_{CC}	18		21	B4Y
GND	19		20	B4Z

'LVDS387
DGG PACKAGE
(TOP VIEW)

GND	1		64	A1Y
V_{CC}	2		63	A1Z
V_{CC}	3		62	A2Y
GND	4		61	A2Z
ENA	5		60	A3Y
A1A	6		59	A3Z
A2A	7		58	A4Y
A3A	8		57	A4Z
A4A	9		56	B1Y
ENB	10		55	B1Z
B1A	11		54	B2Y
B2A	12		53	B2Z
B3A	13		52	B3Y
B4A	14		51	B3Z
GND	15		50	B4Y
V_{CC}	16		49	B4Z
V_{CC}	17		48	C1Y
GND	18		47	C1Z
C1A	19		46	C2Y
C2A	20		45	C2Z
C3A	21		44	C3Y
C4A	22		43	C3Z
ENC	23		42	C4Y
D1A	24		41	C4Z
D2A	25		40	D1Y
D3A	26		39	D1Z
D4A	27		38	D2Y
END	28		37	D2Z
GND	29		36	D3Y
V_{CC}	30		35	D3Z
V_{CC}	31		34	D4Y
GND	32		33	D4Z

'LVDS391
D OR PW PACKAGE
(TOP VIEW)

EN1,2	1		16	1Y
1A	2		15	1Z
2A	3		14	2Y
V_{CC}	4		13	2Z
GND	5		12	3Y
3A	6		11	3Z
4A	7		10	4Y
EN3,4	8		9	4Z

description

This family of four, eight, and sixteen differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the sixteen current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

TEXAS INSTRUMENTS

description (continued)

When disabled, the driver outputs are high impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 are characterized for operation from –40°C to 85°C. The SN75LVDS387, SN75LVDS389, and SN75LVDS391 are characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

(1/4 of 'LVDS387 or 1/2 of 'LVDS389 shown)   **('LVDS391 shown)**
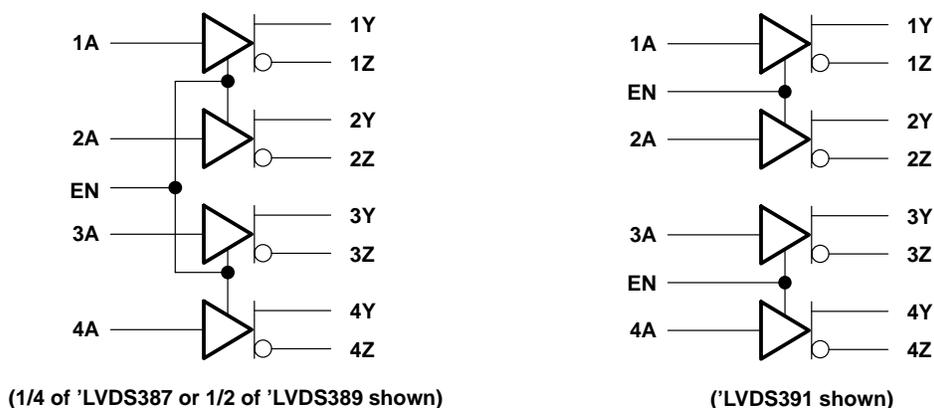
AVAILABLE OPTIONS

| PART NUMBER†	TEMPERATURE RANGE	NO. OF DRIVERS	BUS-PIN ESD
SN65LVDS387DGG	–40°C to 85°C	16	15 kV
SN75LVDS387DGG	0°C to 70°C	16	4 kV
SN65LVDS389DBT	–40°C to 85°C	8	15 kV
SN75LVDS389DBT	0°C to 70°C	8	4 kV
SN65LVDS391D	–40°C to 85°C	4	15 kV
SN75LVDS391D	0°C to 70°C	4	4 kV
SN65LVDS391PW	–40°C to 85°C	4	15 kV
SN75LVDS391PW	0°C to 70°C	4	4 kV

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., SN65LVDS387DGGR).

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

H = high-level, L = low-level, X = irrelevant,
Z = high-impedance (off)

equivalent input and output schematic diagrams

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4 V
Input voltage range: Inputs	−0.5 V to 6 V
Y or Z	−0.5 V to 4 V
Electrostatic discharge: SN65' (Y, Z, and GND)	Class 3, A:15 kV, B: 500 V
SN75' (Y, Z, and GND)	Class 3, A:4 kV, B: 400 V
Continuous power dissipation	(see Dissipation Rating Table)
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN75'	0		70	°C
	SN65'	−40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$|V_{OD}|$	Differential output voltage magnitude	R_L = 100 Ω, , See Figure 1 and Figure 2		247	340	454	mV
$\Delta|V_{OD}|$	Change in differential output voltage magnitude between logic states			−50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage			1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3		−50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{CC}	Supply current	'LVDS387	Enabled, R_L = 100 Ω, V_{IN} = 0.8 V or 2 V		85	95	mA
		'LVDS389			50	70	
		'LVDS391			20	26	
		'LVDS387	Disabled, V_{IN} = 0 V or V_{CC}		0.5	1.5	
		'LVDS389			0.5	1.5	
		'LVDS391			0.5	1.3	
I_{IH}	High-level input current	V_{IH} = 2 V			3	20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			2	10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V				±24	mA
		V_{OD} = 0 V				±12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}				±1	μA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, $\quad$ V_O = 2.4 V				±1	μA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V			5		pF
C_O	Output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled			9.4		pF

† All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 4	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	ns
t_r	Differential output signal rise time		0.4	0.8	1	ns
t_f	Differential output signal fall time		0.4	0.8	1	ns
$t_{sk(p)}$	Pulse skew ($|t_{PHL} - t_{PLH}|$)			150	500	ps
$t_{sk(o)}$	Output skew‡			80	150	ps
$t_{sk(pp)}$	Part-to-part skew§				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		6.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			5.9	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.5	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.5	15	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

PARAMETER MEASUREMENT INFORMATION
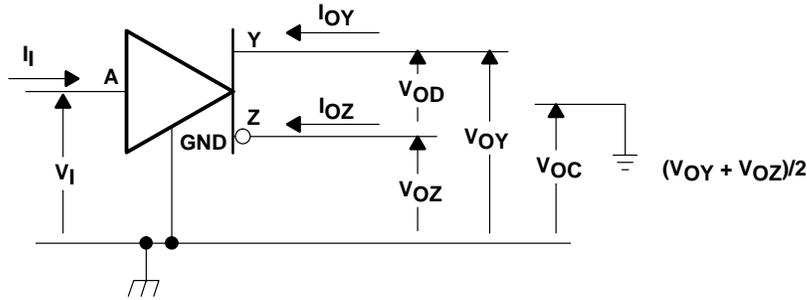
**Figure 1. Voltage and Current Definitions**
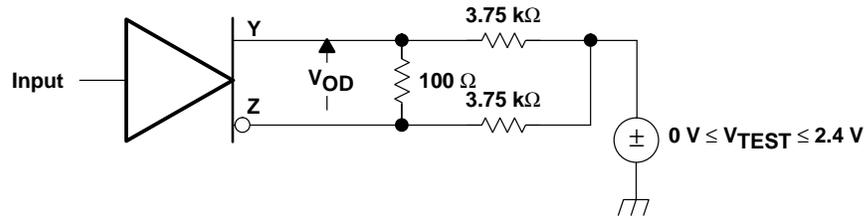
Figure 2. VOD Test Circuit
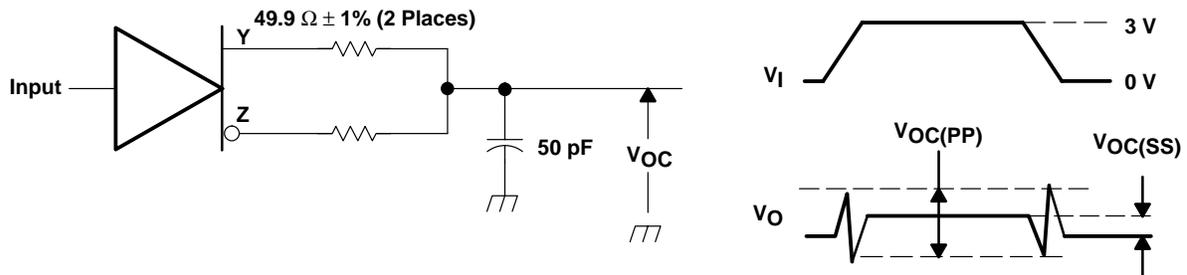
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage
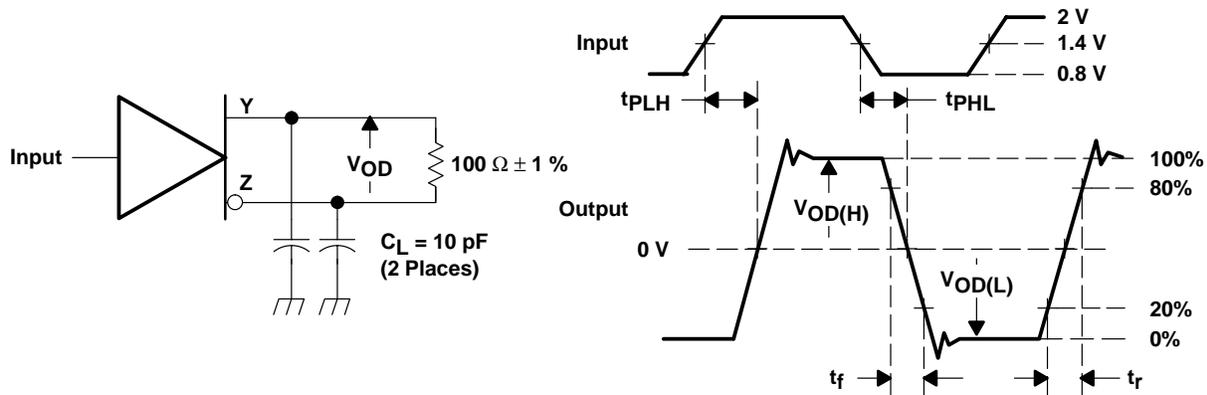
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION
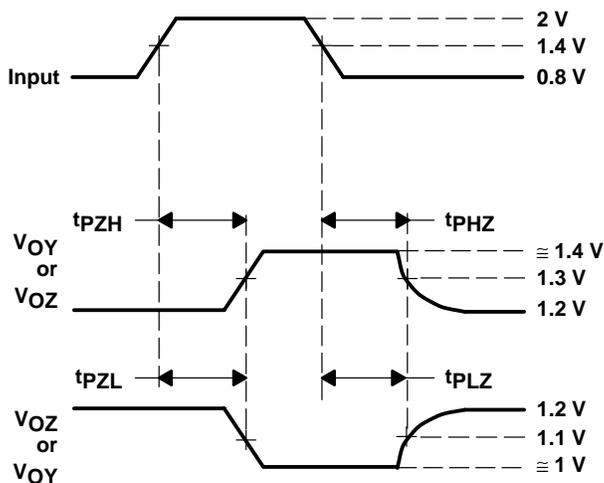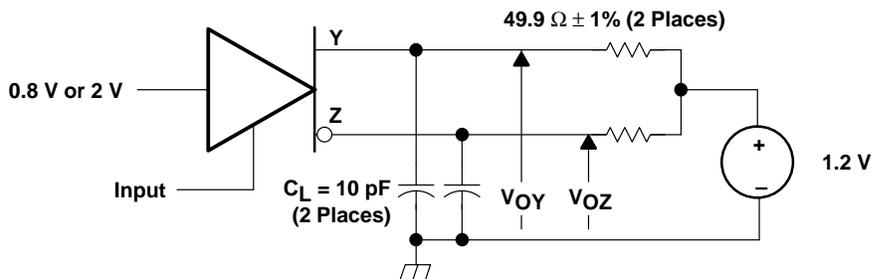
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 5. Enable and Disable Time Circuit and Definitions**

TEXAS
INSTRUMENTS

TYPICAL CHARACTERISTICS

'LVDS391
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY

Figure 6

'LVDS387
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY

Figure 7

'LVDS389
SUPPLY CURRENT (RMS)
vs
SWITCHING FREQUENCY

Figure 8

TEXAS
INSTRUMENTS
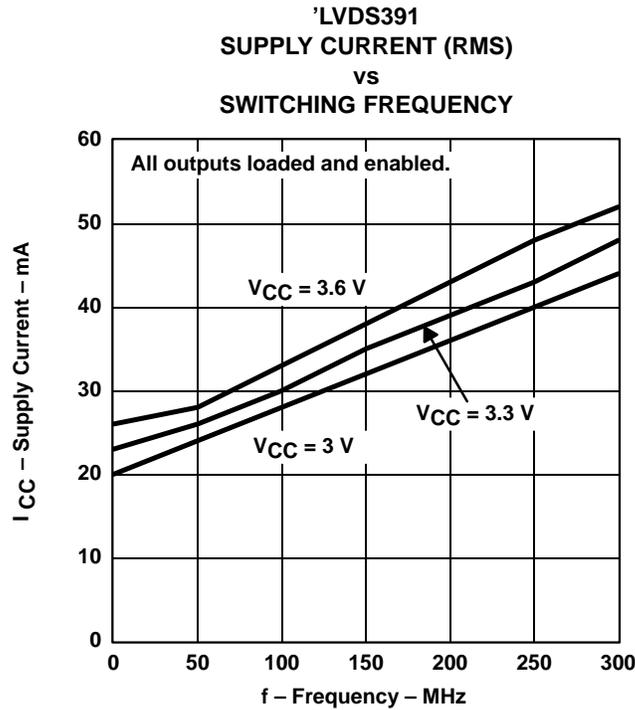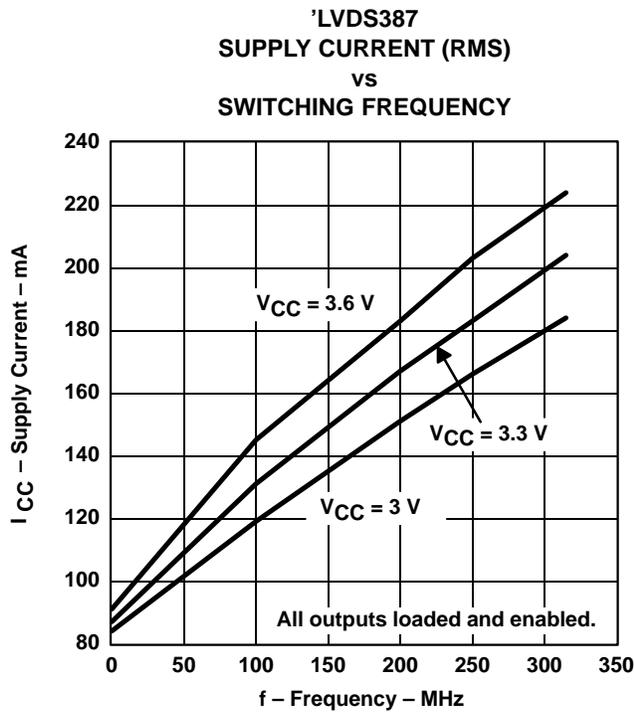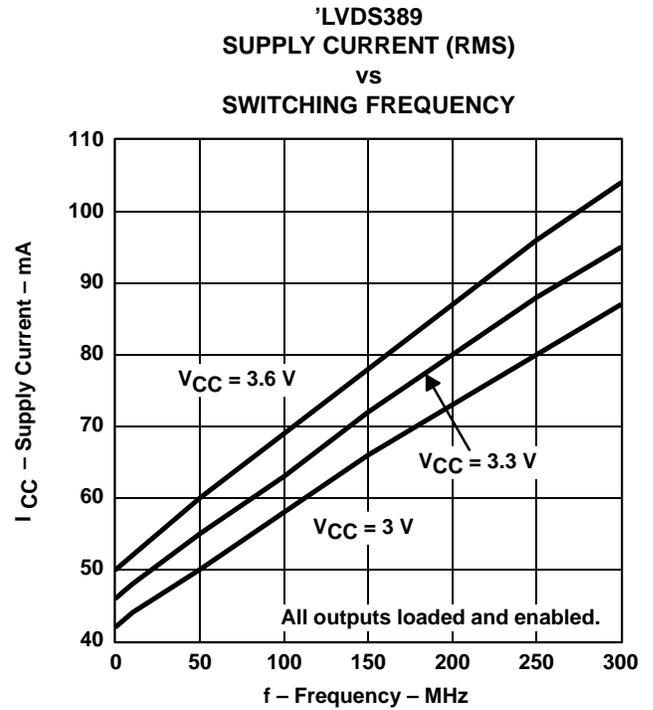
TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE
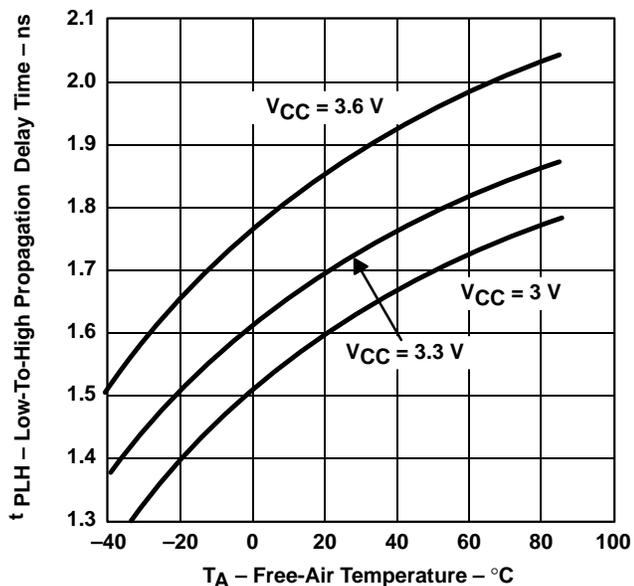
Figure 9

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE
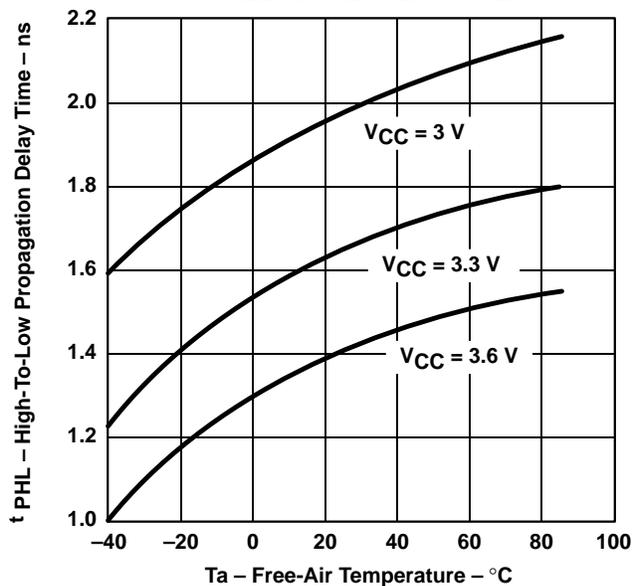
Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT
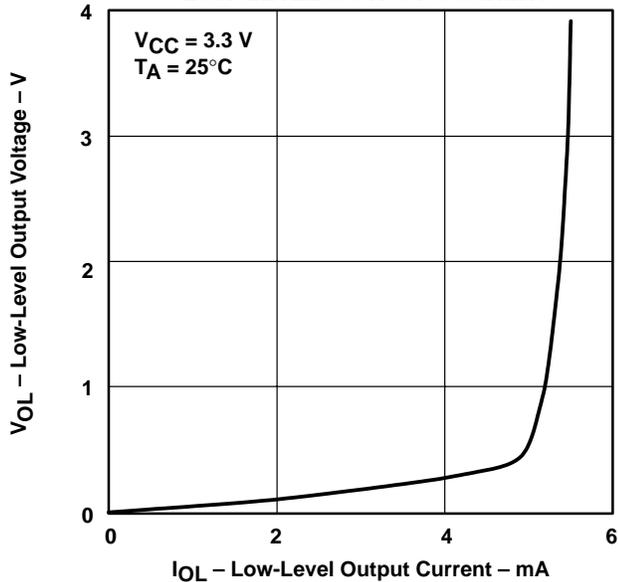
Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT
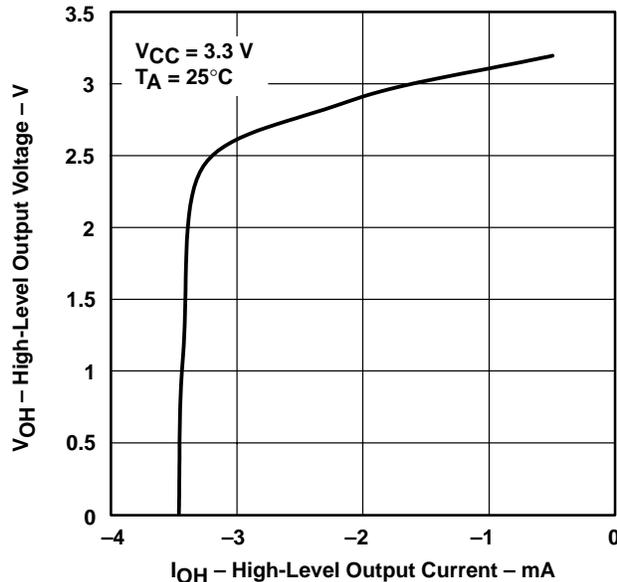
Figure 12
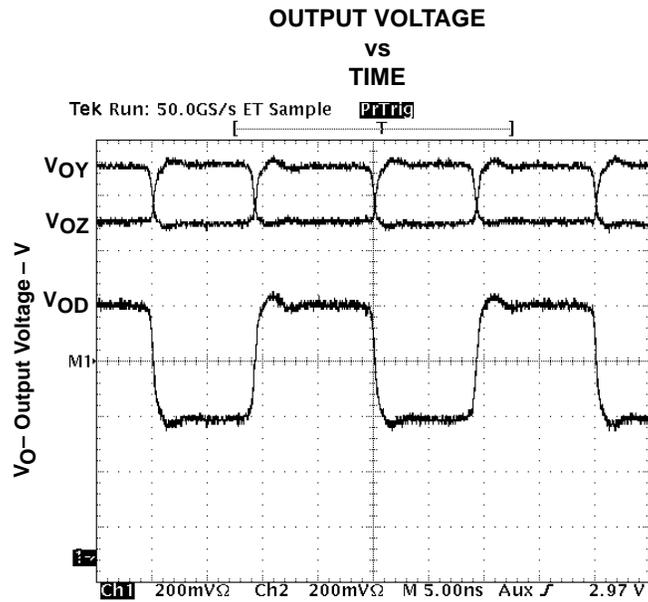
SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
**vs**
TIME

Figure 13

APPLICATION INFORMATION
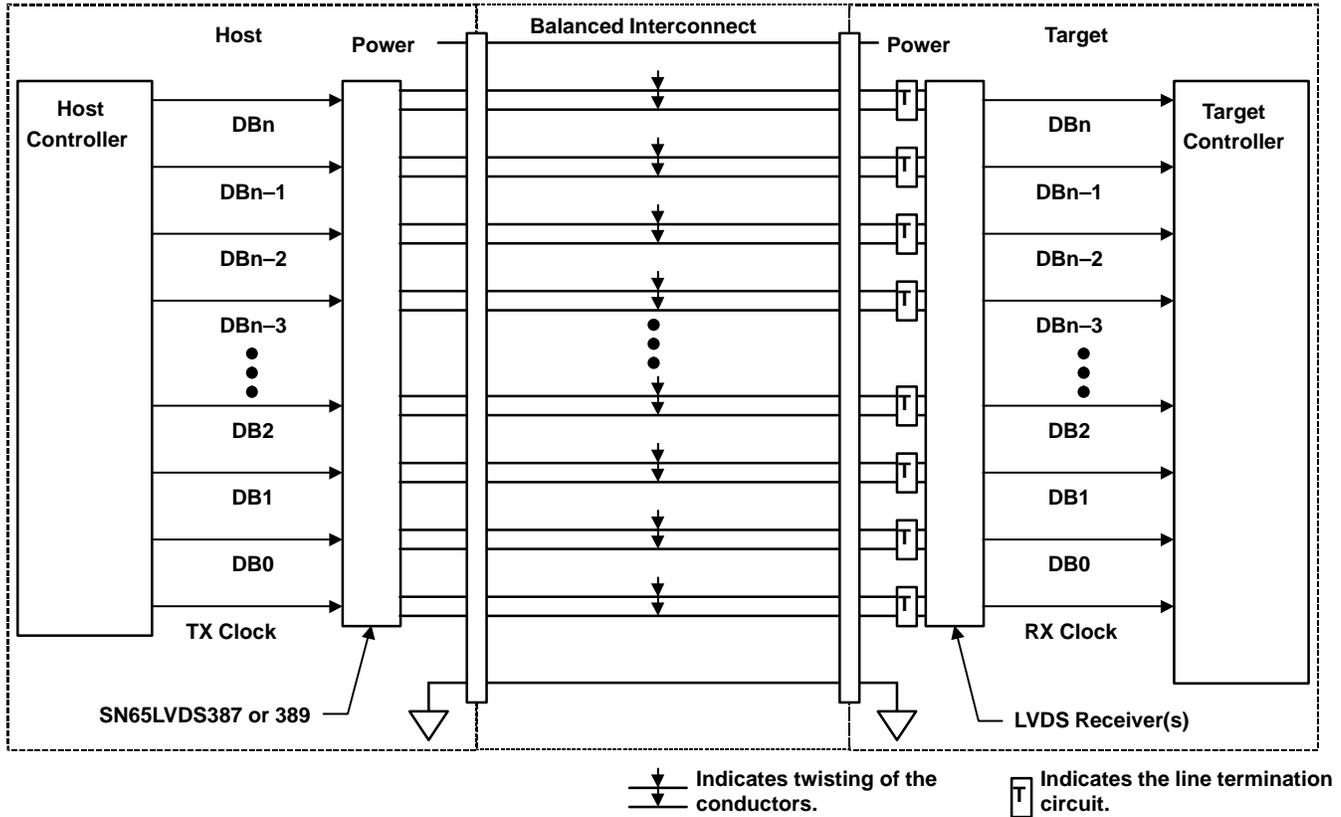
Figure 14. Typical Application Schematic

Signaling Rate vs Distance

The ultimate data transfer rate over a given cable or trace length involves many variables. Starting with the capabilities of this LVDS driver to reproduce a data pulse as short as 1.6 ns (a 630 Mbps signaling rate) with less than 500 ps of pulse distortion, any degradation of this pulse by the transmission media will necessarily reduce the timing margin at the receiving end of the data link.

The timing uncertainty induced by the transmission media is commonly referred to as jitter and comes from numerous sources. The characteristics of a particular transmission media can be quantified by using an eyepattern measurement such as shown in Figure 12, which shows about 340 ps of jitter or 20% of the data pulse width.

![Texas Instruments logo]
TEXAS INSTRUMENTS

APPLICATION INFORMATION
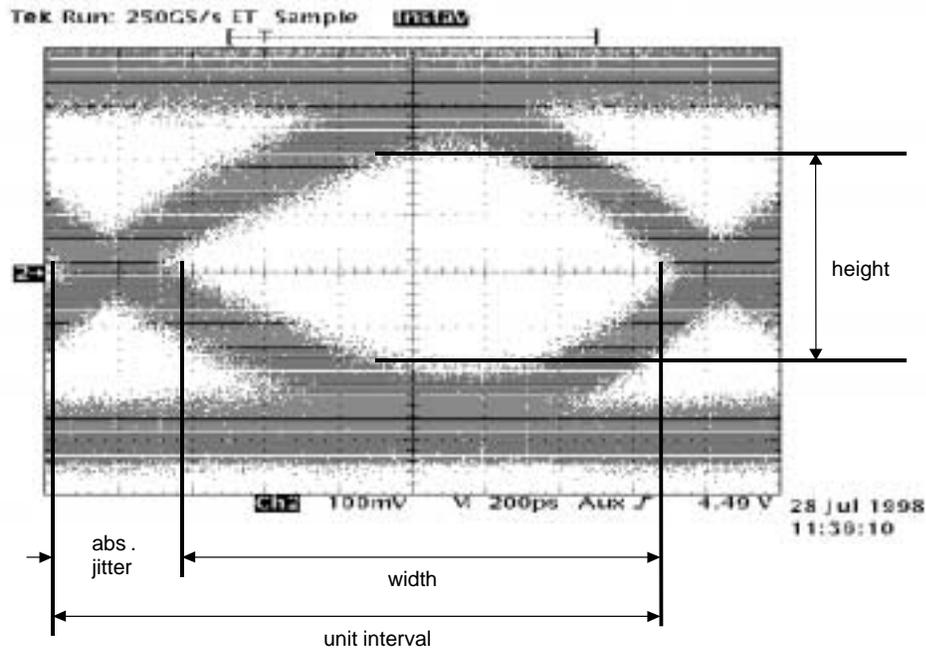
Figure 15. Typical LVDS Eyepattern

A generally accepted range of jitter at the receiver inputs that allows data recovery is 5% to 20% of the unit interval (data pulse width). Table 1 shows the signaling rate achieved on various cables and lengths at a 5% eyepattern jitter with a typical LVDS driver.

Table 1. Signaling Rates for Various Cables for 5% Eyepattern Jitter

LENGTH (m)	CABLE†					
	A (Mbps)	B (Mbps)	C (Mbps)	D (Mbps)	E (Mbps)	F (Mbps)
1	240	200	240	270	180	230
5	205	210	230	250	215	230
10	180	150	195	200	145	180

† Cable A: CAT 3, specified up to 16 MHz, no shield, outside conductor diameter (∅) 0.52 mm
  Cable B: CAT 5, specified up to 100 MHz, no shield, ∅ 0.52 mm
  Cable C: CAT 5, specified up to 100 MHz, taped over all shield, ∅ 0.52 mm
  Cable D: CAT 5 (exceeding CAT 5), specified up to 300 MHz, braided over all shield plus taped individual shield for any
          pair, ∅ 0.64 mm (AWG22)
  Cable E: CAT 5 (exceeding CAT 5), specified up to 350 MHz, ∅ 0.64 mm (AWG22), no shield
  Cable F: CAT 5 (exceeding CAT 5), specified up to 350 MHz, "self-shielded", ∅ 0.64 mm (AWG22)

During synchronous parallel transfers, skew between the data and clock lines will also reduce the timing margin. This must be accounted for in the system timing budget. Fortunately, the low output skew of this LVDS driver will generally be a small portion of this budget.

other LVDS products

For other products and applications notes in the LVDS and LVDM product families visit our Web site at **http://www.ti.com/sc/datatran**.

SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

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MECHANICAL DATA

D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.014\ (0,35)}$ ⊕ 0.010 (0,25) Ⓜ

14   8

$\dfrac{0.244\ (6,20)}{0.228\ (5,80)}$

$\dfrac{0.157\ (4,00)}{0.150\ (3,81)}$

1   7

A

0.008 (0,20) NOM

Gage Plane

0°–8°

0.010 (0,25)

$\dfrac{0.044\ (1,12)}{0.016\ (0,40)}$

0.069 (1,75) MAX

$\dfrac{0.010\ (0,25)}{0.004\ (0,10)}$

Seating Plane

△ 0.004 (0,10)

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96
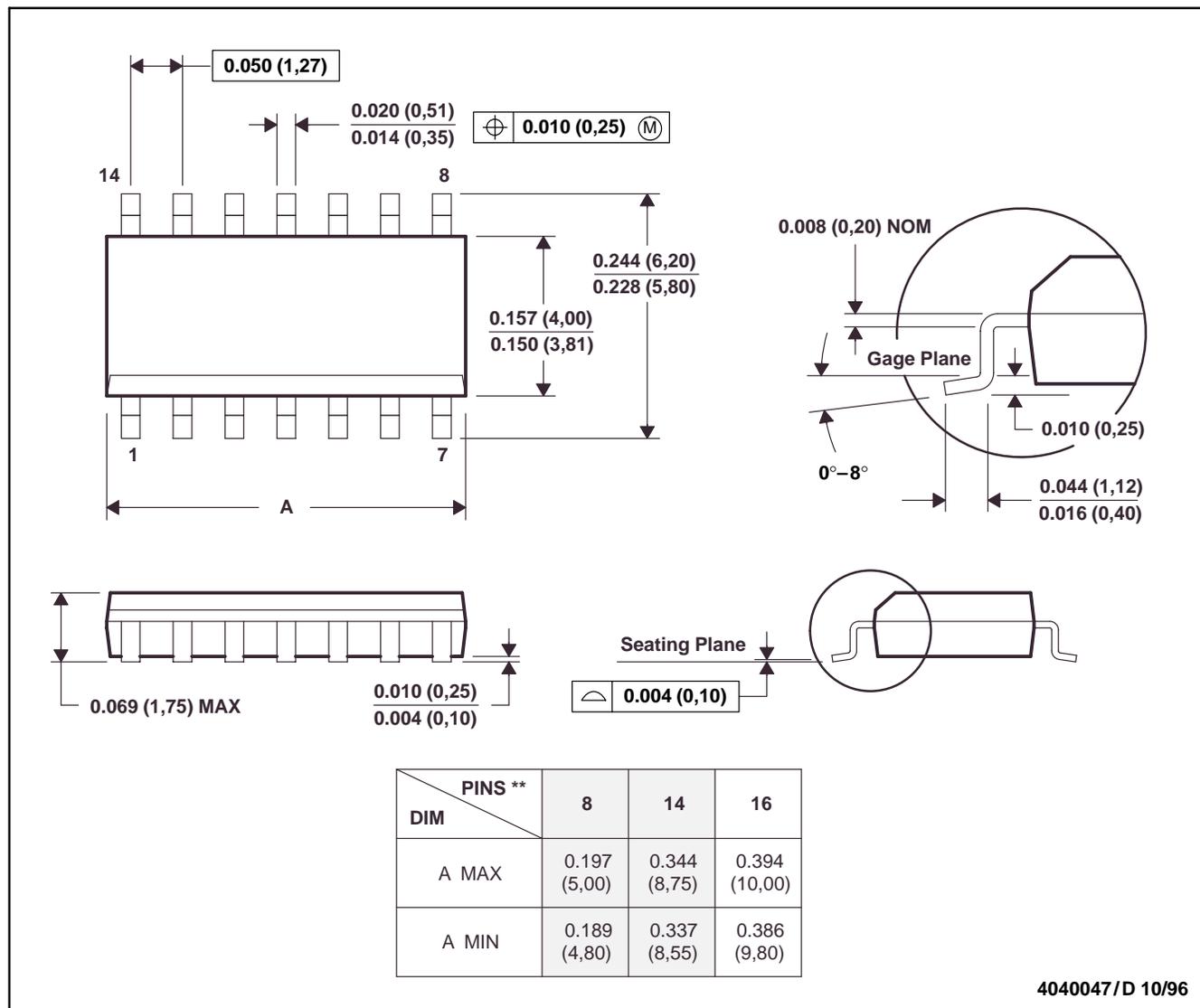
NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
           D. Falls within JEDEC MS-012

MECHANICAL DATA

DBT (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN
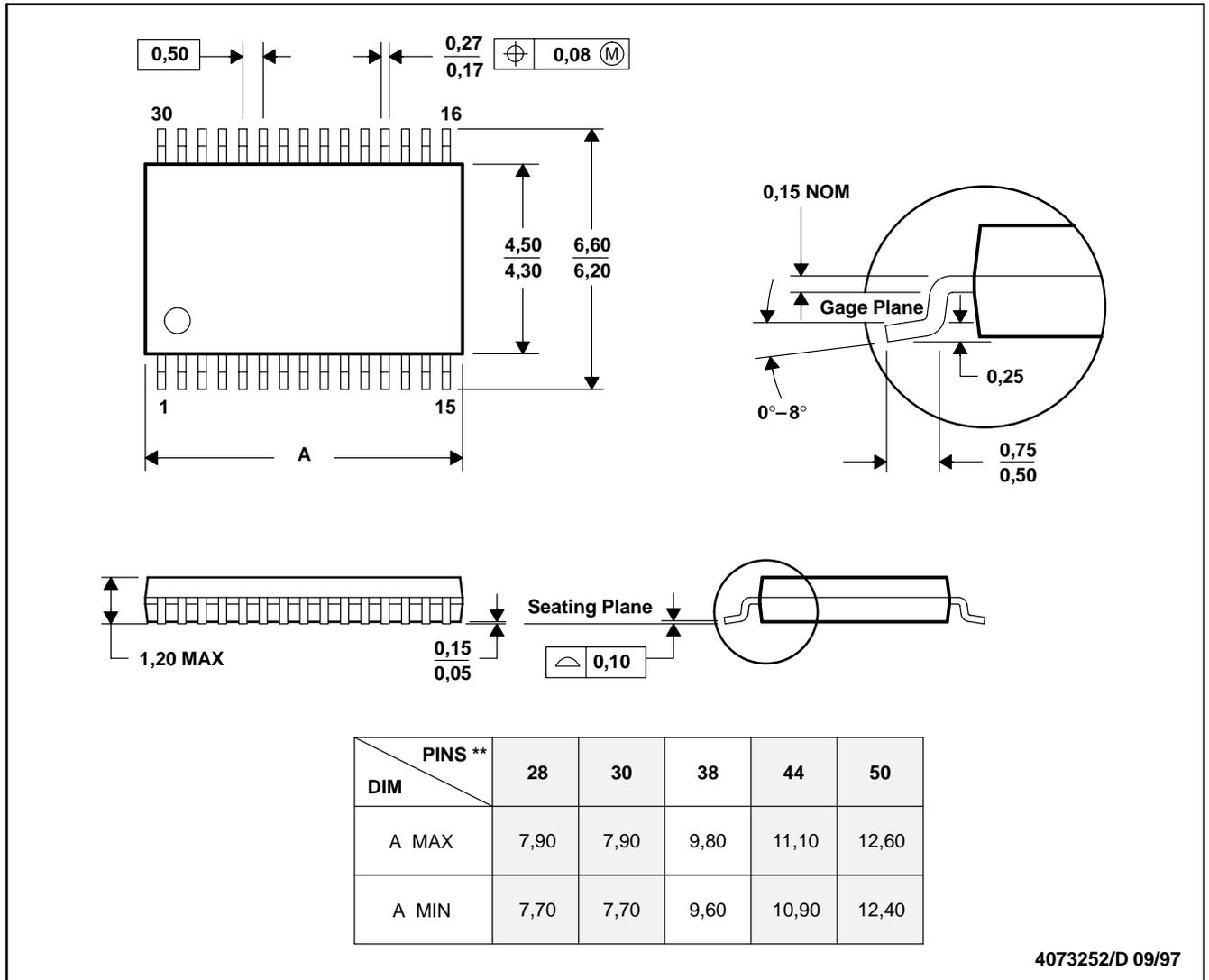
PINS ** DIM	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion.
        D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391
HIGH-SPEED DIFFERENTIAL LINE DRIVERS

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MECHANICAL DATA

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN
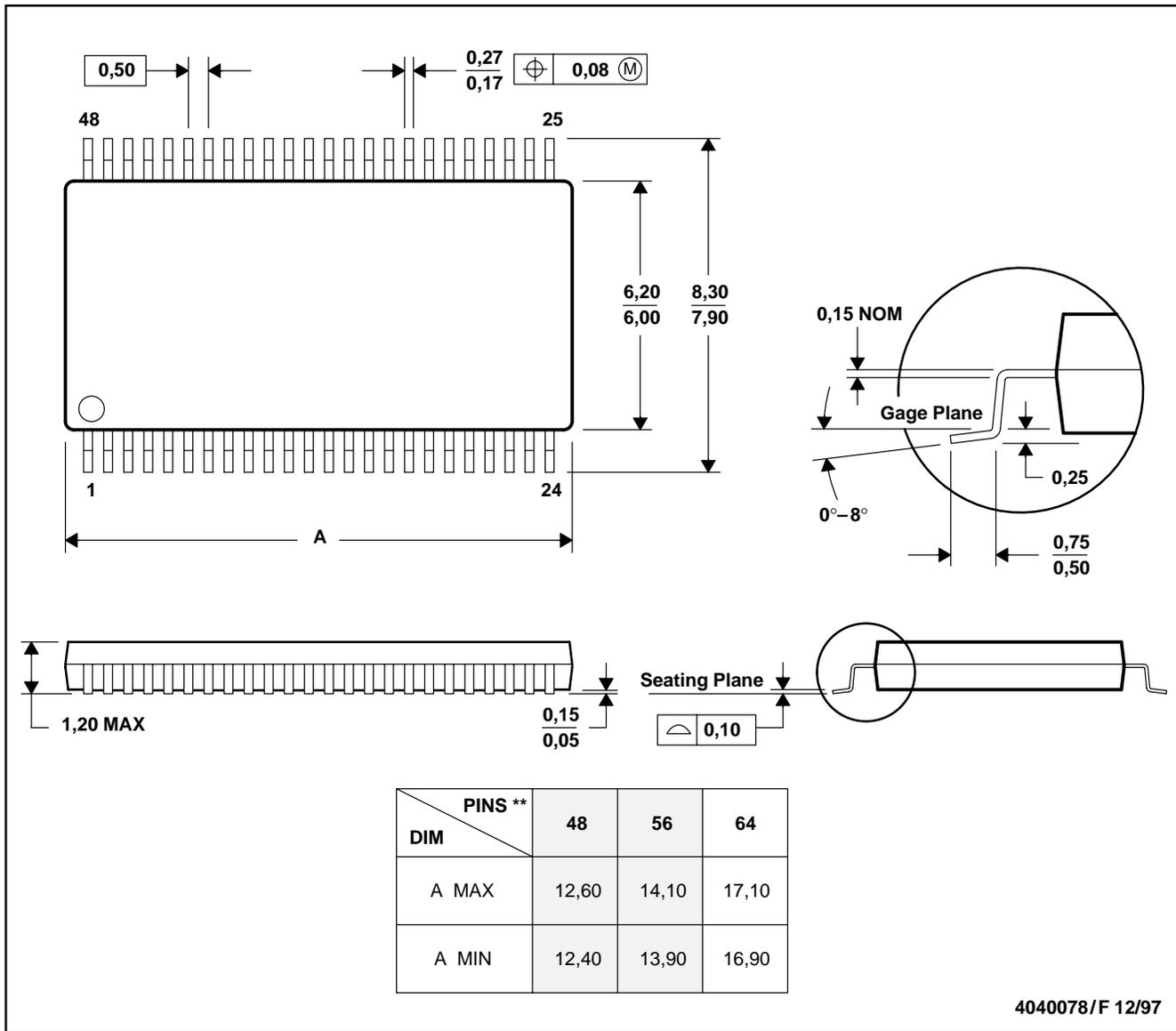
PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

MECHANICAL DATA

PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**
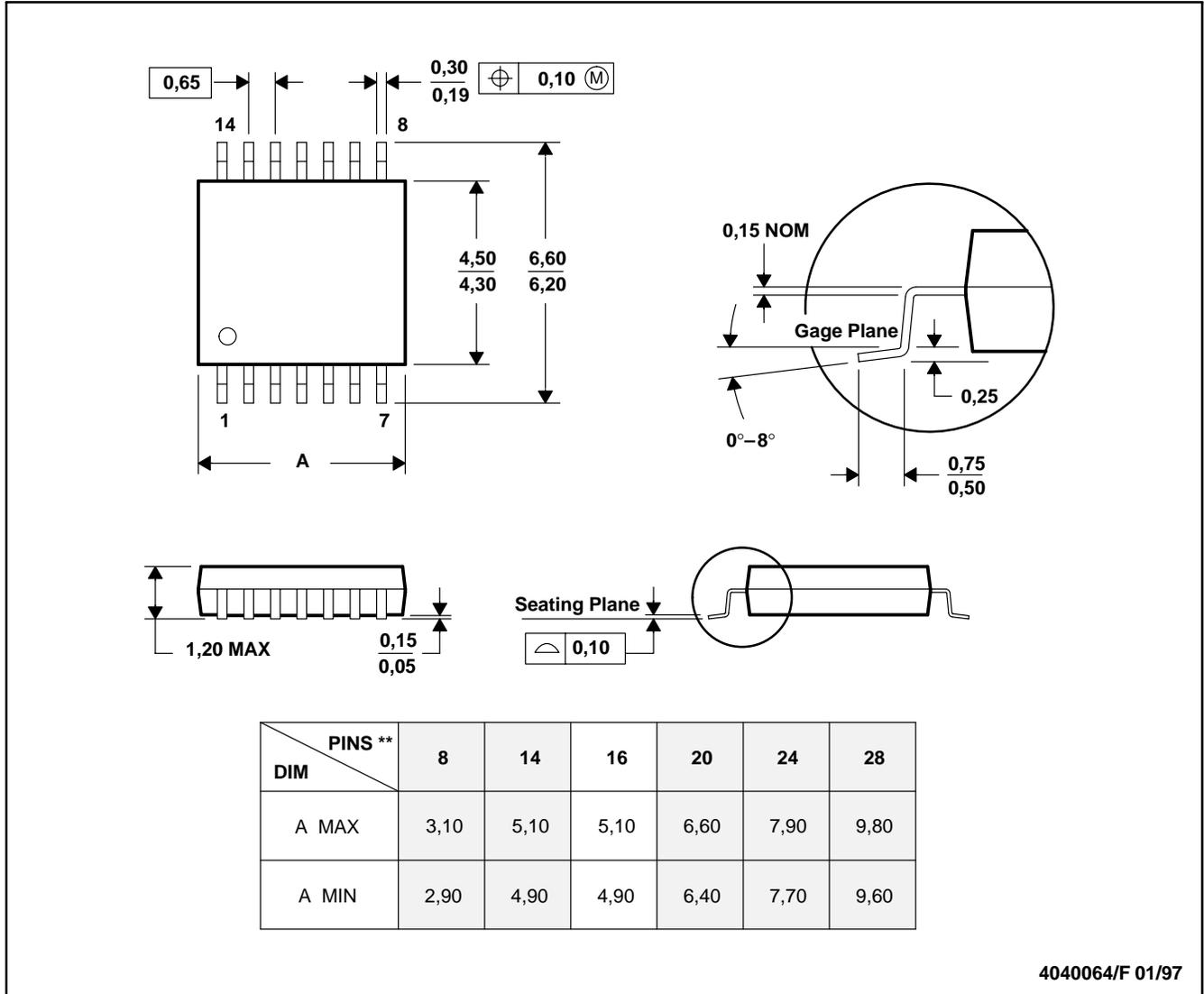
14 PINS SHOWN

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS389DBT	ACTIVE	SM8	DBT	38	50	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS389DBTG4	PREVIEW	SM8	DBT	38	50	None	Call TI	Call TI
SN65LVDS389DBTR	ACTIVE	SM8	DBT	38	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS389DBTRG4	PREVIEW	SM8	DBT	38	2000	None	Call TI	Call TI
SN65LVDS391D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS391DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS391PW	ACTIVE	TSSOP	PW	16	90	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS389DBT	ACTIVE	SM8	DBT	38	50	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS389DBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS389DBTR	ACTIVE	SM8	DBT	38	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS389DBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS391D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS391DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS391PW	ACTIVE	TSSOP	PW	16	90	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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