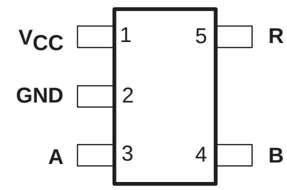
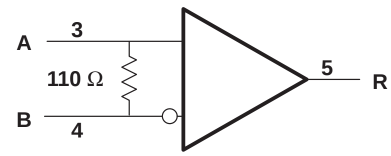
SLLS374B – JULY 1999 – REVISED JANUARY 2000

- **Meets or Exceeds ANSI TIA/EIA-644-1995 Standard**
- **Integrated Line Termination Resistor**
- **Designed for Signaling Rates up to 400 Mbps**
- **Operates From a 2.4-V to 3.6-V Supply**
- **Available in the SOT23-5 Package**
- **Differential Input Voltage Threshold Less Than 100 mV**
- **Propagation Delay Times, 2.5 ns Typical**
- **Power Dissipation at 200 MHz is Typically 60 mW**
- **Bus-Pin ESD Protection Exceeds 15 kV**
- **Open-Circuit Fail Safe**
- **Outputs High Impedance With V_{CC} < 1.5 V**

SN65LVDT2
DBV PACKAGE
(TOP VIEW)



logic diagram



Function Table

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV < V_{ID} < 100 mV	?
$V_{ID} \leq -100$ mV	L
Open	H

H = high level, L = low level , ? = indeterminate

description

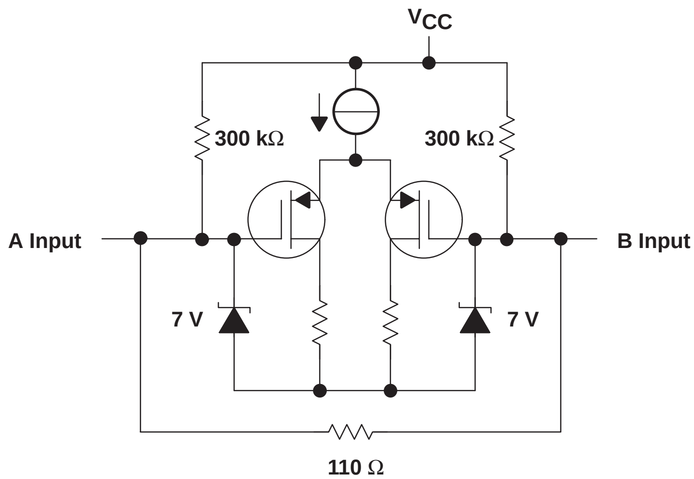
The SN65LVDT2 is a single low-voltage differential line receiver in a small-outline transistor package. The inputs comply with the TIA/EIA-644 standard and provide a maximum differential input threshold of 100 mV over an input common-mode voltage range of 0 V to 2.5 V.

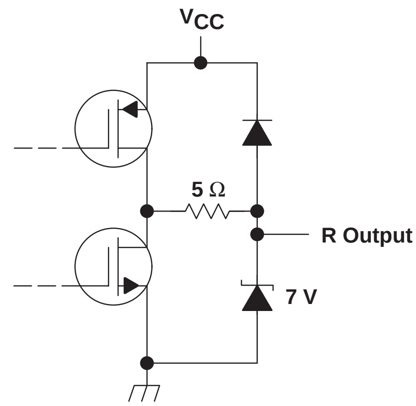
When used with a low-voltage differential signaling (LVDS) driver (such as the SN65LVDS1) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit board traces or cables at very high rates with very low electromagnetic emissions and power consumption.

The high-speed switching of LVDS signals requires the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. TI offers both the SN65LVDT2, which integrates the terminating resistor for point-to-point applications, and its companion the SN65LVDS2, which requires an external resistor. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make these devices ideal for battery-powered applications.

The SN65LVDT2 is characterized for operation from –40°C to 85°C.

equivalent input and output schematic diagrams





absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 4 V
Voltage range (A, B, or R)	–0.5 V to V_{CC}+ 0.5 V
Electrostatic discharge: A, B , and GND (see Note 2)	CLass 3, A:15 kV, B:600 V
Continuous total power dissipation	See dissipation rating table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$†	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	200 mW

† This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.4	3.3	3.6	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		0.6	V
Common–mode input voltage, V_{IC} (see Figure 6)	0		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			V_{CC}–0.8	
Operating free–air temperature, T_A	–40		85	°C

COMMON-MODE INPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

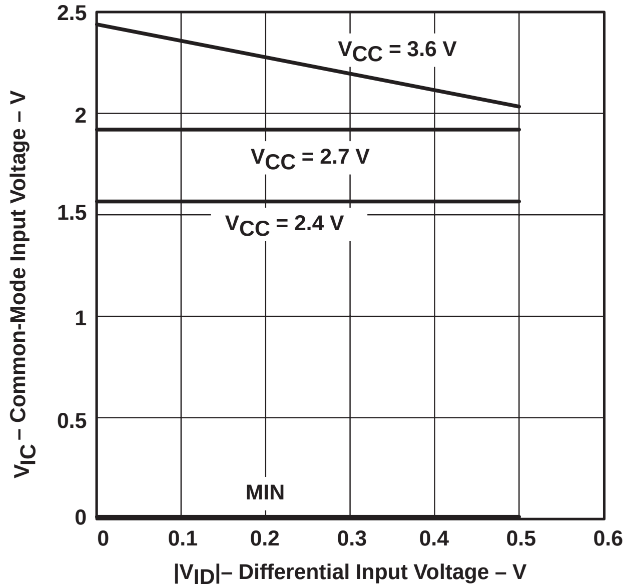


Figure 1. V_{IC} vs V_{ID} and V_{CC}

electrical characteristics over recommended operating conditions, V_{CC} = 2.4 V to 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	I_{OH} = –8 mA	1.9	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.25	0.4	V
I_{CC}	Supply current	No load, Steady state		4	7	mA
I_I	Input current (A or B inputs)	V_I = 0 V			±40	µA
		V_I = 2.4 V or V_{CC} – 0.8	–2.4			
I_{ID}	Differential input current (I_{IA} – I_{IB})	V_{IA} = 0.4 V, V_{IB} = 0 V V_{IA} = 2.4 V, V_{IB} = 2 V	3	3.6	4.4	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V, V_I = 2.4 V, Other input open			40	µA

† All typical values are at 25°C and with a 2.7-V supply.

receiver switching characteristics over recommended operating conditions, V_{CC} = 2.4 V to 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	1.4	2.6	3.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.5	3.6	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)‡			0.1	0.6	ns
t_r	Output signal rise time			0.8	1.4	ns
t_f	Output signal fall time			0.8	1.4	ns

† All typical values are at 25°C and with a 2.7-V.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

electrical characteristics over recommended operating conditions, V_{CC} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold	See Figure 2 and Table 1	–100			mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4	3		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.25	0.4	V
I_{CC}	Supply current	No load, Steady state		5	8	mA
I_I	Input current (A or B inputs)	V_I = 0 V, Other input open			±40	µA
		V_I = 2.4 V, Other input open	–2.4			µA
I_{ID}	Differential input current (I_{IA} – I_{IB})	V_{IA} = 0.4 V, V_{IB} = 0 V V_{IA} = 2.4 V, V_{IB} = 2 V	3	3.6	4.4	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V, V_I = 2.4 V, Other input open			40	µA

† All typical values are at 25°C and with a 3.3-V supply.

receiver switching characteristics over recommended operating conditions, V_{CC} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	1.4	2.6	3.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.5	3.1	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} – t_{pLH}\rvert$)‡			0.1	0.5	ns
t_r	Output signal rise time			0.7	1.1	ns
t_f	Output signal fall time			0.7	1.1	ns

† All typical values are at 25°C and with a 3.3-V.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

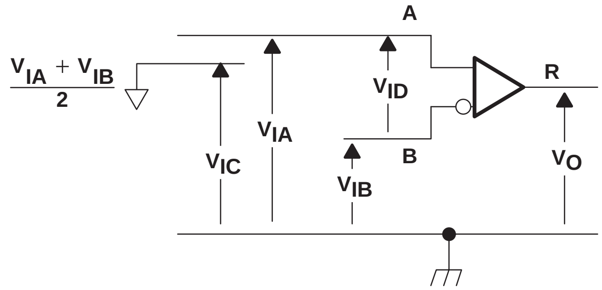
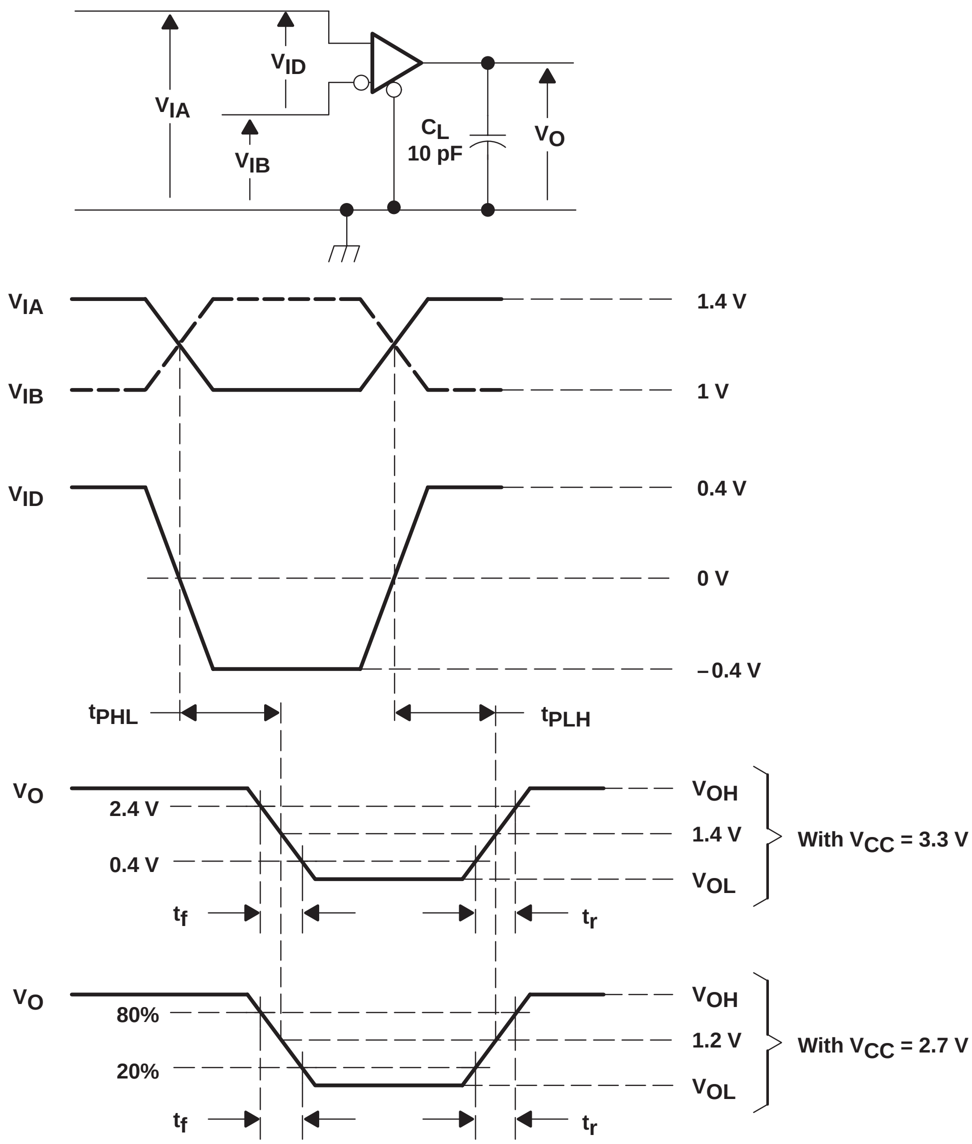


Figure 2. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

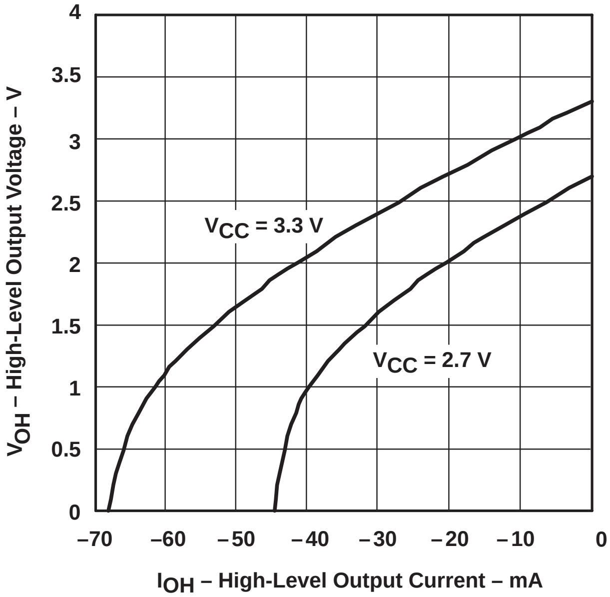


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

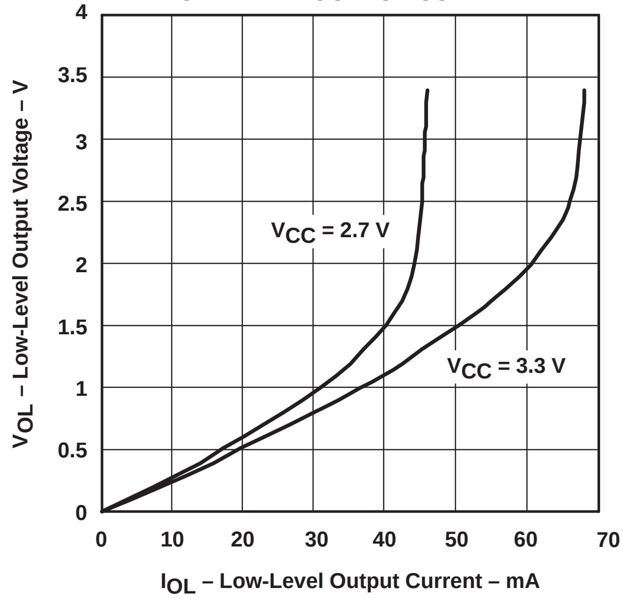


Figure 5

HIGH-TO-LOW LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

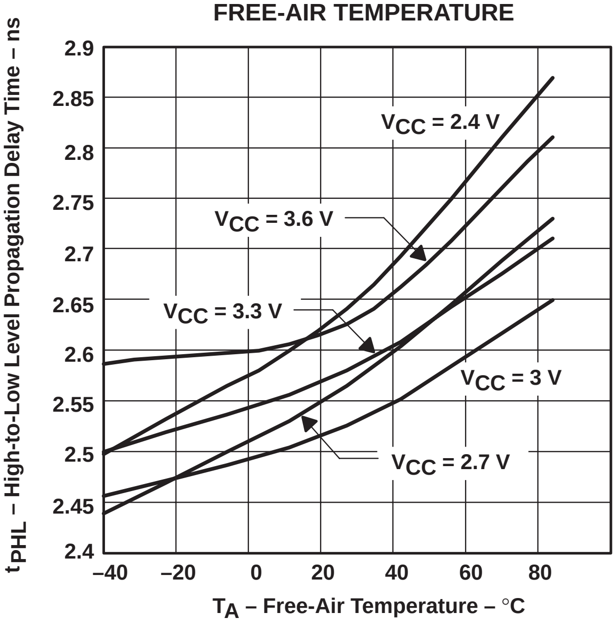


Figure 6

LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

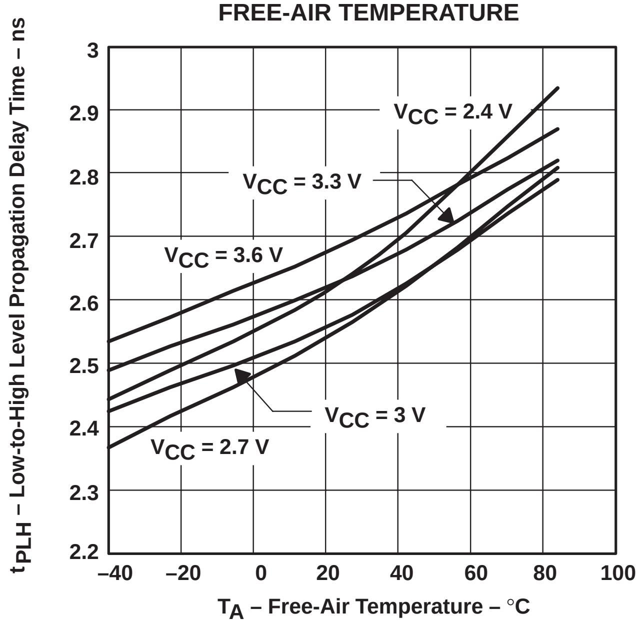


Figure 7

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

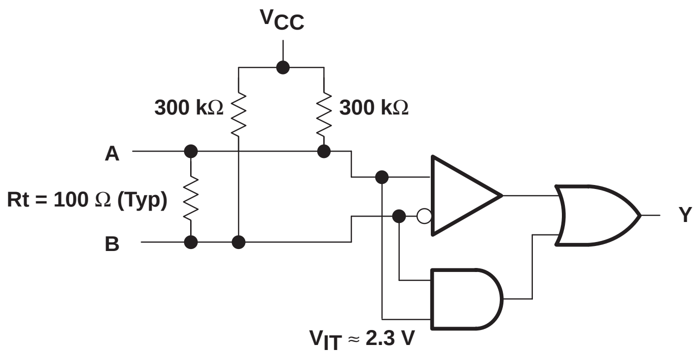
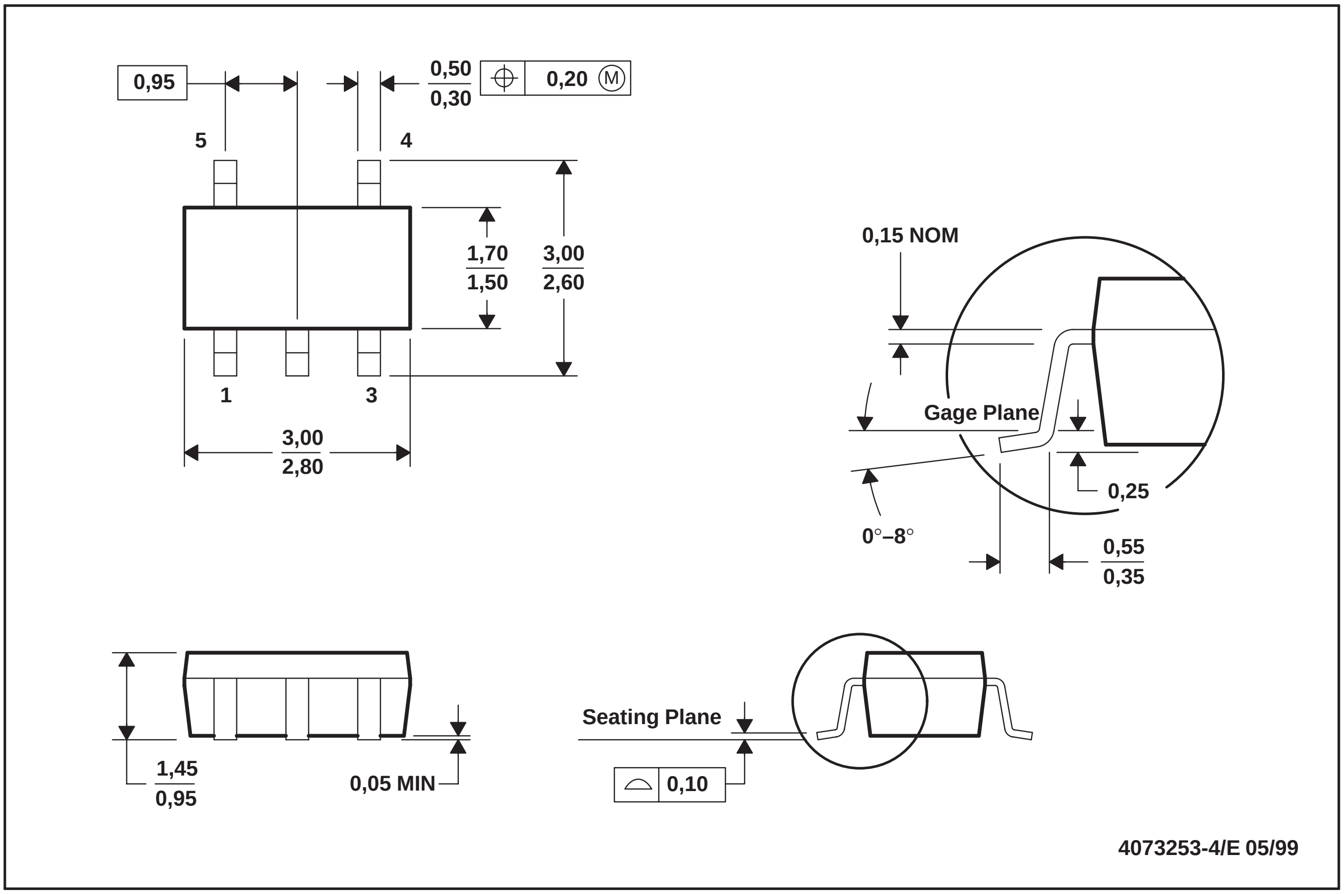


Figure 8. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

MECHANICAL INFORMATION

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178