

**FAIRCHILD**  
SEMICONDUCTOR®

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## 74VHC125 Quad Buffer with 3-STATE Outputs

### General Description

The VHC125 contains four independent non-inverting buffers with 3-STATE outputs. It is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology and achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High Speed:  $t_{PD} = 3.8$  ns (typ) at  $V_{CC} = 5$  V
- Lower power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_A = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8$ V (max)
- Pin and function compatible with 74HC125

### Ordering Code:

Order Number	Package Number	Package Description
74VHC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC125MX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC125SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC125MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC125N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

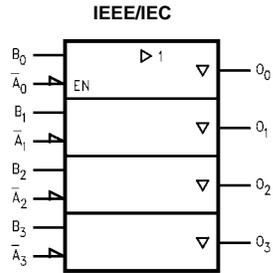
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** ".NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

74VHC125 Quad Buffer with 3-STATE Outputs



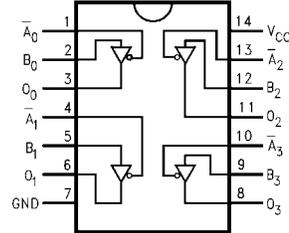
**Logic Symbol**



**Pin Descriptions**

Pin Names	Description
$\bar{A}_n, B_n$	Inputs
$O_n$	Outputs

**Connection Diagram**



**Function Table**

Inputs		Output
$\bar{A}_n$	$B_n$	$O_n$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = HIGH Impedance  
 X = Immaterial

**Absolute Maximum Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 3)

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	$V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$
	0 ~ 100 ns/V 0 ~ 20 ns/V

**Note 2:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 3:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$		V		
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 $V_{CC}$		0.50 0.3 $V_{CC}$	V		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
		3.0	2.58			2.48				
4.5	3.94			3.80						
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
		3.0			0.36		0.44			
4.5			0.36		0.44					
$I_{OZ}$	3-STATE Output Off-State Current	5.5			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	
$I_{IN}$	Input Leakage Current	0 – 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 4)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.5	0.8	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 4)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.5	-0.8	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 4)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 4)	Maximum HIGH Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

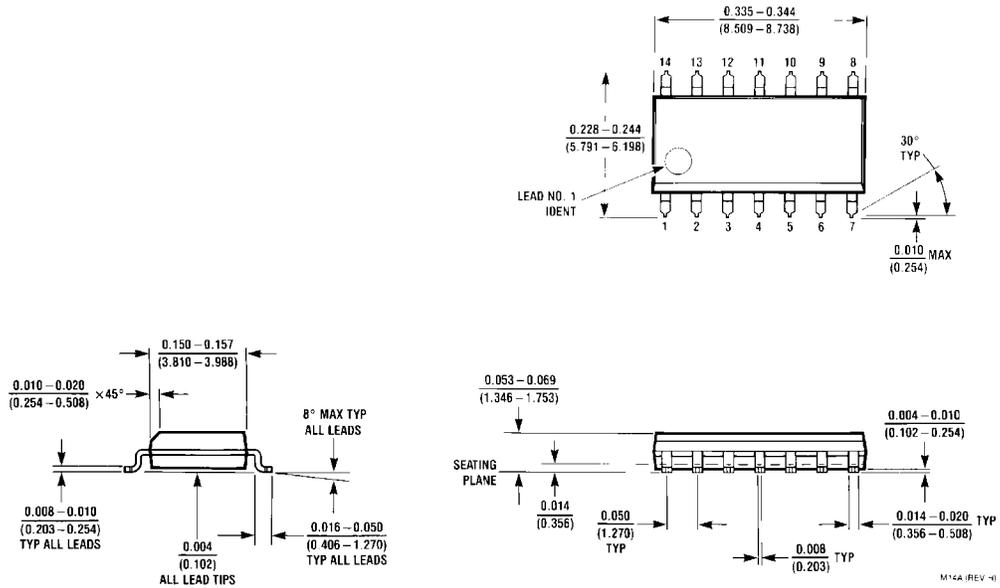
**Note 4:** Parameter guaranteed by design.

AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time	3.3 ± 0.3	5.6	8.0	1.0	9.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PHL</sub>			8.1	11.5	1.0	13.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	3.8	5.5	1.0	6.5	ns	C <sub>L</sub> = 15 pF	
			5.3	7.5	1.0	8.5		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub>	3-STATE Output Enable Time	3.3 ± 0.3	5.4	8.0	1.0	9.5	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF	
t <sub>PZH</sub>			7.9	11.5	1.0	13.0			C <sub>L</sub> = 50 pF
		5.0 ± 0.5	3.6	5.1	1.0	6.0	ns	C <sub>L</sub> = 15 pF	
			5.1	7.1	1.0	8.0		C <sub>L</sub> = 50 pF	
t <sub>PLZ</sub>	3-STATE Output Disable Time	3.3 ± 0.3	9.5	13.2	1.0	15.0	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF	
t <sub>PHZ</sub>			6.1	8.8	1.0	10.0			C <sub>L</sub> = 50 pF
t <sub>OSLH</sub>	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 5) C <sub>L</sub> = 50 pF	
t <sub>OSHL</sub>			5.0 ± 0.5		1.0				1.0
C <sub>IN</sub>	Input Capacitance		4	10		10	pF	V <sub>CC</sub> = Open	
C <sub>OUT</sub>	Output Capacitance		6				pF	V <sub>CC</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation Capacitance		14				pF	(Note 6)	

**Note 5:** Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$ ;  $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$ .

**Note 6:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC} (OPR.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$  (per bit).

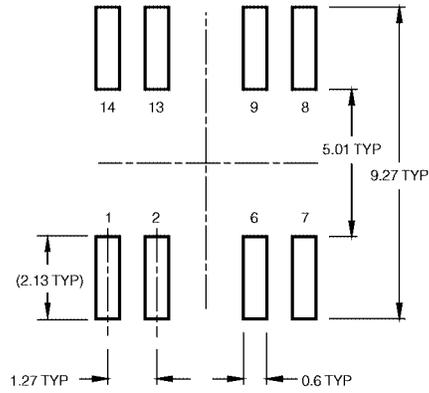
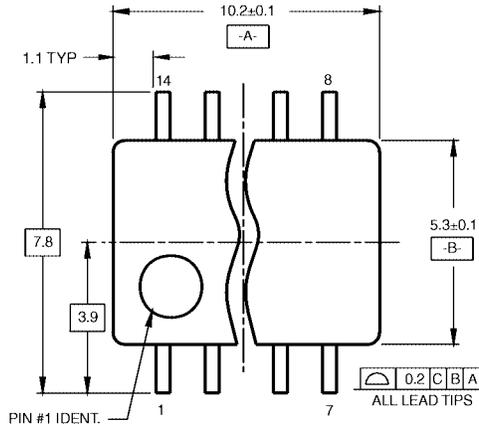
**Physical Dimensions** inches (millimeters) unless otherwise noted



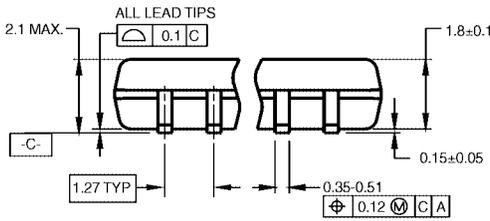
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

M14A (REV. H)

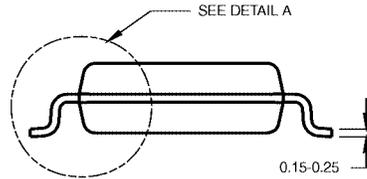
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

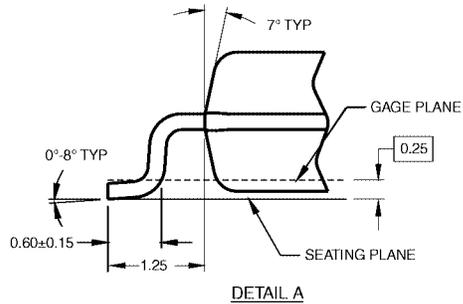


DIMENSIONS ARE IN MILLIMETERS



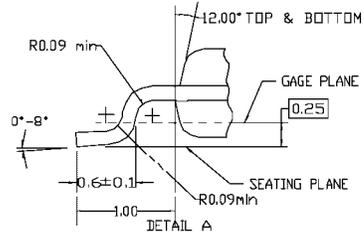
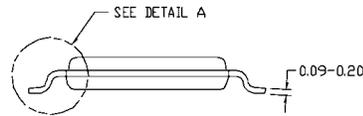
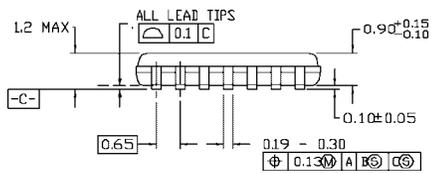
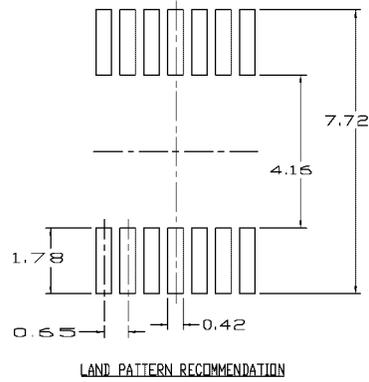
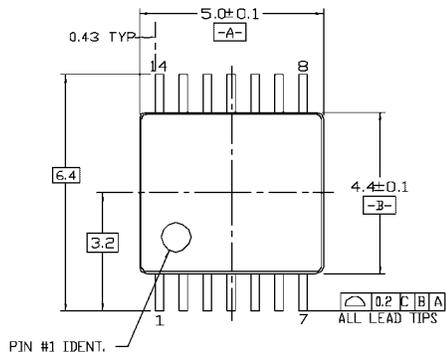
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



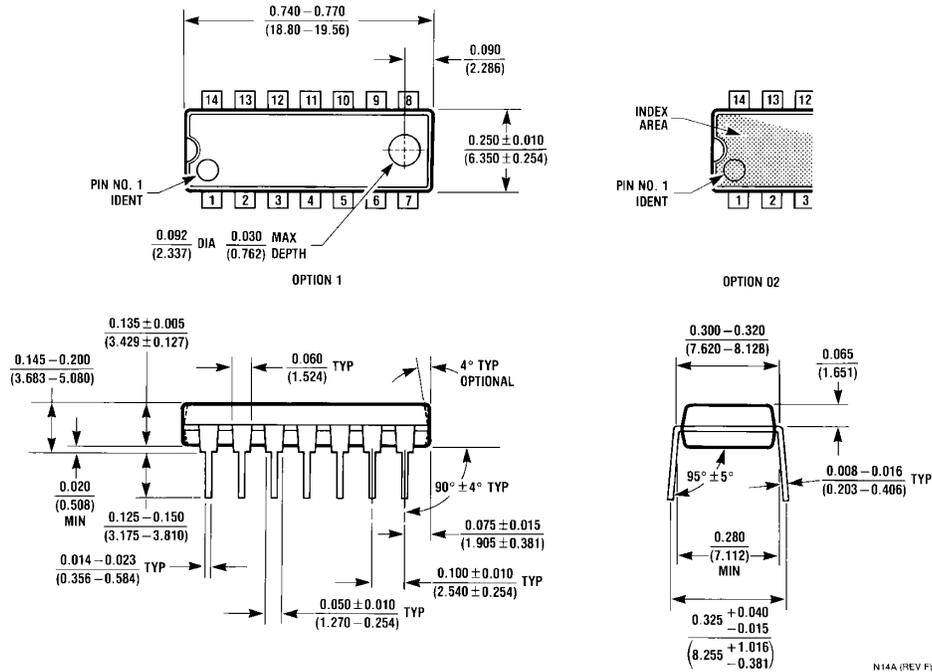
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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