

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC174F, TC74VHC174FN, TC74VHC174FT

HEX D-TYPE FLIP-FLOP WITH CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

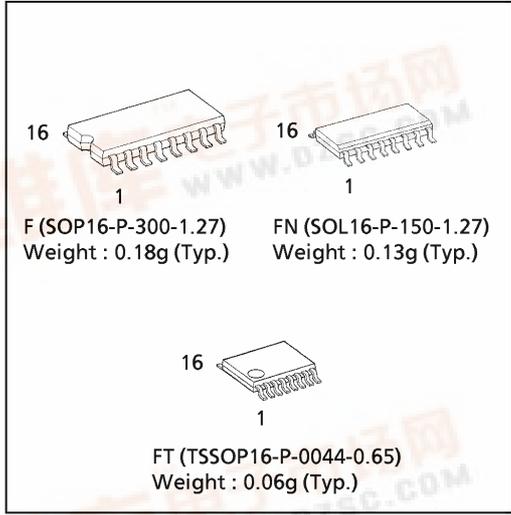
Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the CLR input is held low, the Q output are in the low logic level independent of the other inputs.

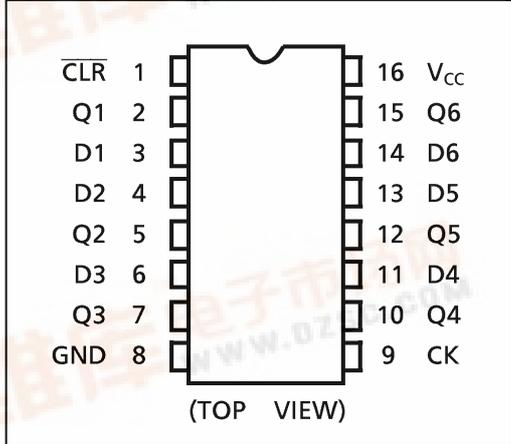
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

- High Speed..... $f_{MAX} = 150\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 0.8\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS174



PIN ASSIGNMENT

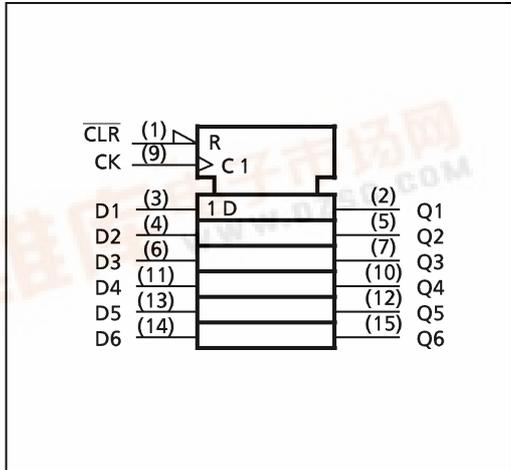


TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
CLR	D	CK	Q	
L	X	X	L	CLEAR
H	L		L	—
H	H		H	—
H	X		Q _n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL

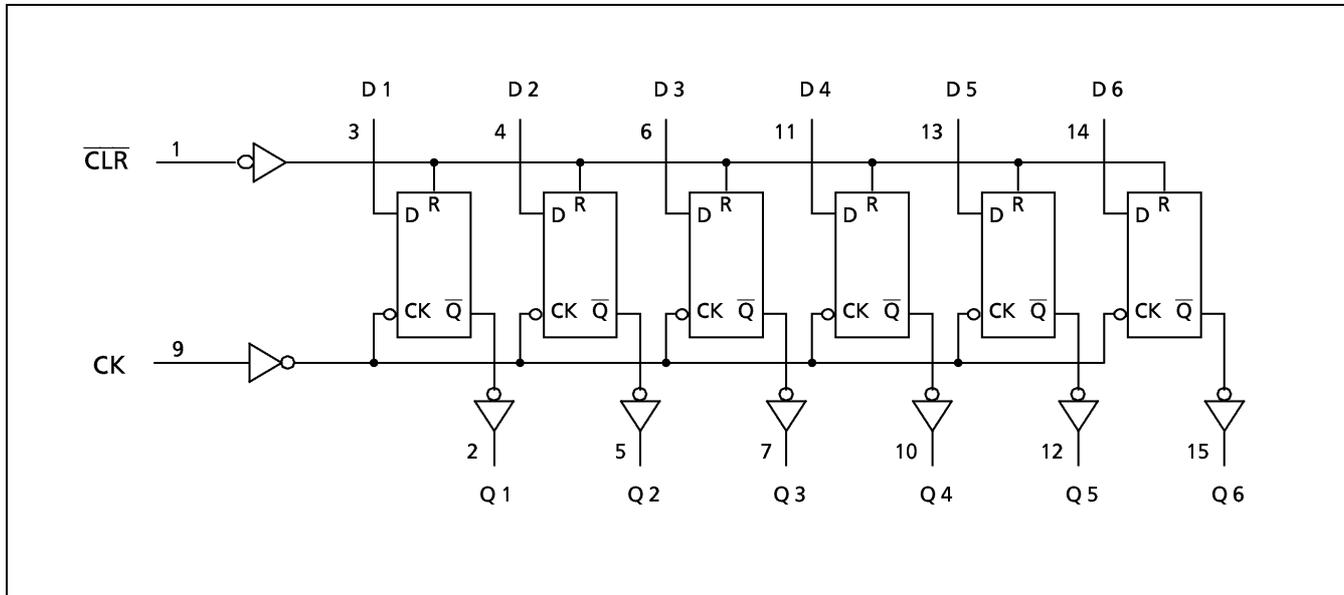


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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0~ 5.5	1.50 V _{CC} ×0.7	— —	— —	1.50 V _{CC} ×0.7	—	V
Low - Level Input Voltage	V _{IL}			2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} ×0.3	— —	0.50 V _{CC} ×0.3	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C		LIMIT	UNIT
					TYP .	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(L)} t _{W(H)}			3.3 ± 0.3	—	5.0	5.0	ns
				5.0 ± 0.5	—	5.0	5.0	
Minimum Pulse Width (CLR)	t _{W(L)}			3.3 ± 0.3	—	5.0	5.0	
				5.0 ± 0.5	—	5.0	5.0	
Minimum Set - up Time	t _s			3.3 ± 0.3	—	5.0	6.0	
				5.0 ± 0.5	—	4.5	4.5	
Minimum Hold Time	t _h			3.3 ± 0.3	—	0.0	0.0	
				5.0 ± 0.5	—	0.5	0.5	
Minimum Removal Time (CLR)	t _{rem}			3.3 ± 0.3	—	3.0	3.0	
				5.0 ± 0.5	—	2.5	2.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	7.2	11.0	1.0	13.0	ns
				50	—	9.7	14.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.9	7.2	1.0	8.5	
				50	—	6.4	9.2	1.0	10.5	
Propagation Delay Time (CLR-Q)	t _{pHL}		3.3 ± 0.3	15	—	7.4	11.4	1.0	13.5	
				50	—	9.9	14.9	1.0	17.0	
			5.0 ± 0.5	15	—	5.1	7.6	1.0	9.0	
				50	—	6.6	9.6	1.0	11.0	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	15	95	150	—	80	—	MHZ
				50	55	85	—	50	—	
			5.0 ± 0.5	15	130	175	—	110	—	
				50	90	120	—	80	—	
Output to Output Skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.5 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	29	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per F/F)}$$

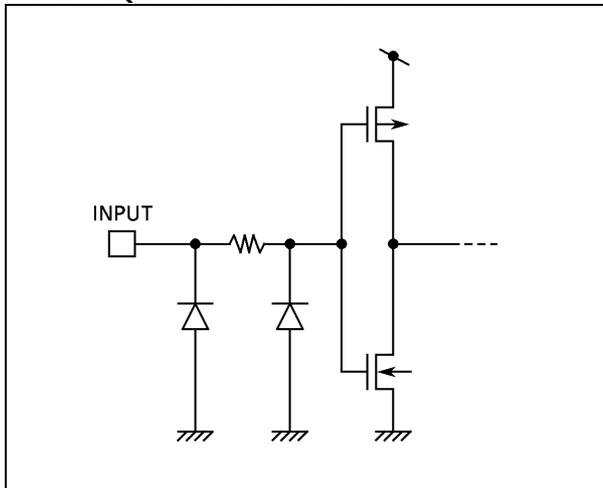
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 19 + 10 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

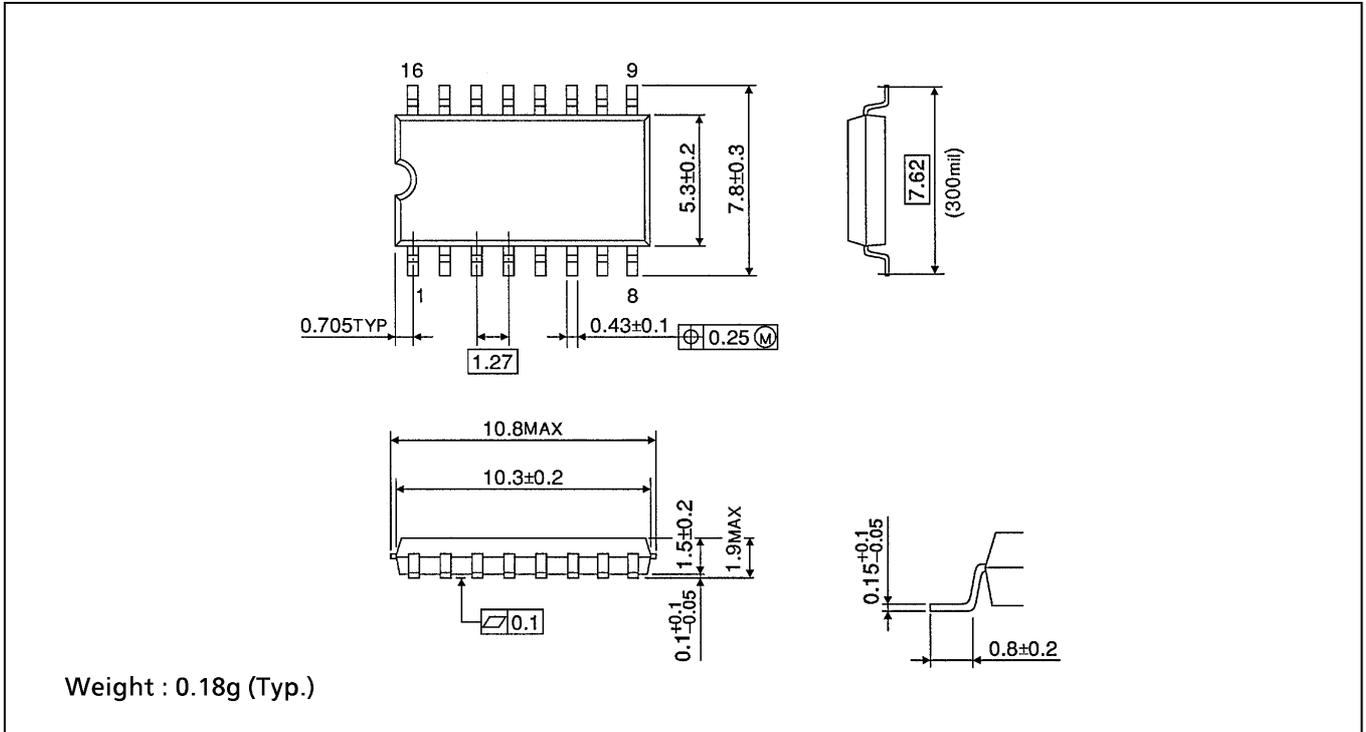
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

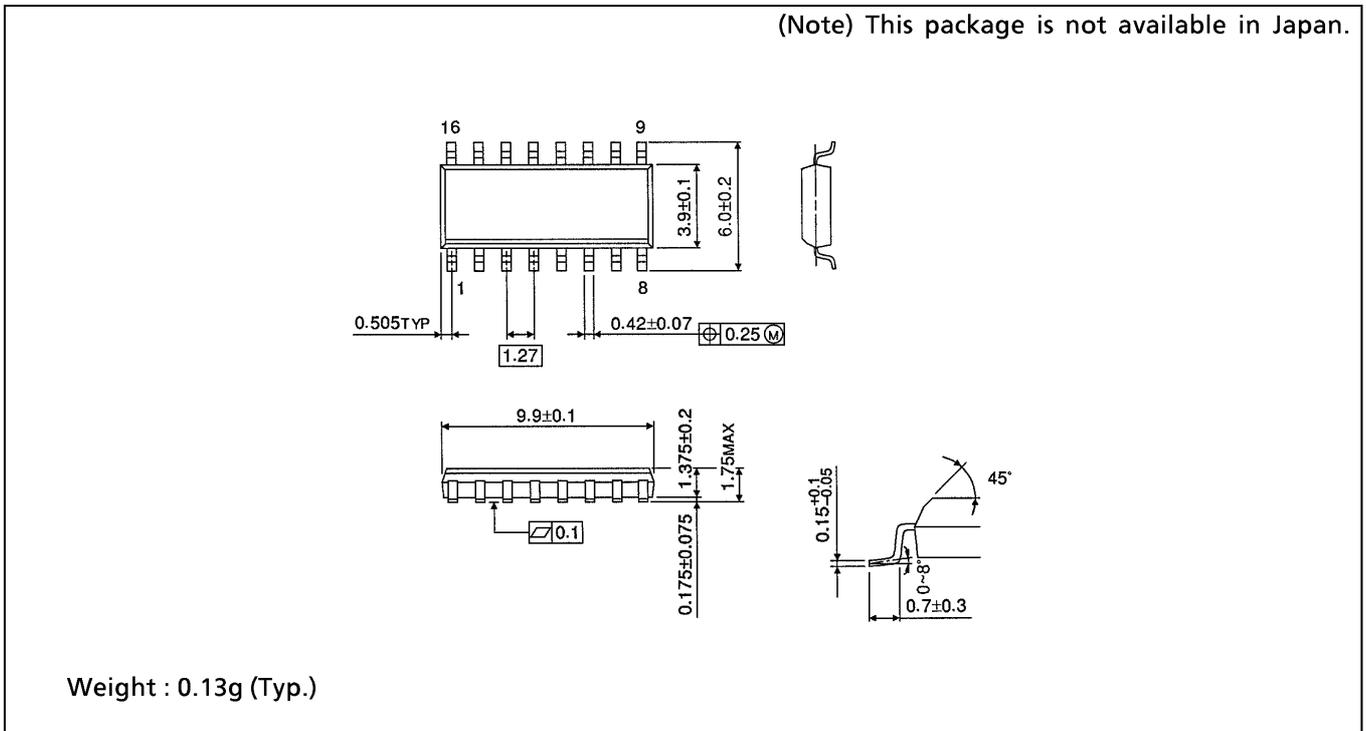
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOP16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm

