

**TOSHIBA**

**TC74VHC367,368F/FN/FT**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VHC367F, TC74VHC367FN, TC74VHC367FT**  
**TC74VHC368F, TC74VHC368FN, TC74VHC368FT**

HEX BUS BUFFER

TC74VHC367 F/FN/FT NON - INVERTED, 3 - STATE OUTPUTS  
 TC74VHC368 F/FN/FT INVERTED, 3 - STATE OUTPUTS

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC367 and 368 are advanced high speed CMOS HEX BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. They contain six buffers ; four buffers are controlled by an enable input ( $\overline{G1}$ ), and the other two buffers are controlled by another enable input ( $\overline{G2}$ ). The outputs of each buffer group are enabled when  $\overline{G1}$  and/or  $\overline{G2}$  inputs are held low ; if held high, these outputs are in a high impedance state. The TC74VHC367 is a non - inverting output type, while the TC74VHC368 is an inverting output type. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

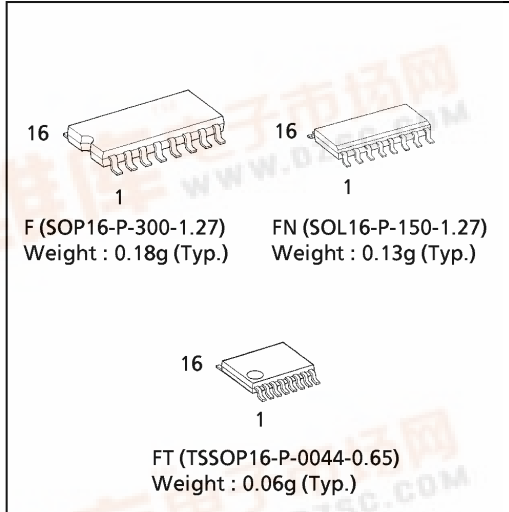
**FEATURES :**

- High Speed.....  $t_{pd} = 3.8ns(typ.)$  at  $V_{CC} = 5V$
- Low Power Dissipation.....  $I_{CC} = 4\mu A(Max.)$  at  $T_a = 25^\circ C$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.....  $V_{CC} (opr) = 2V \sim 5.5V$
- Low Noise .....  $V_{OLP} = 0.8V (Max.)$
- Pin and Function Compatible with 74ALS367/368

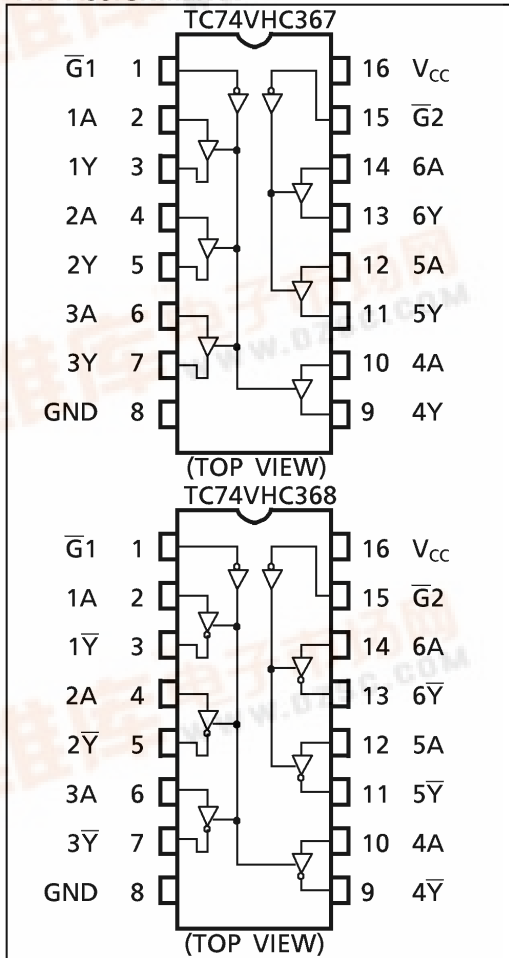
**TRUTH TABLE**

INPUTS		OUTPUTS	
$\overline{G}$	A	Y(367)	$\overline{Y}$ (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care  
 Z : High Impedance



**PIN ASSIGNMENT**

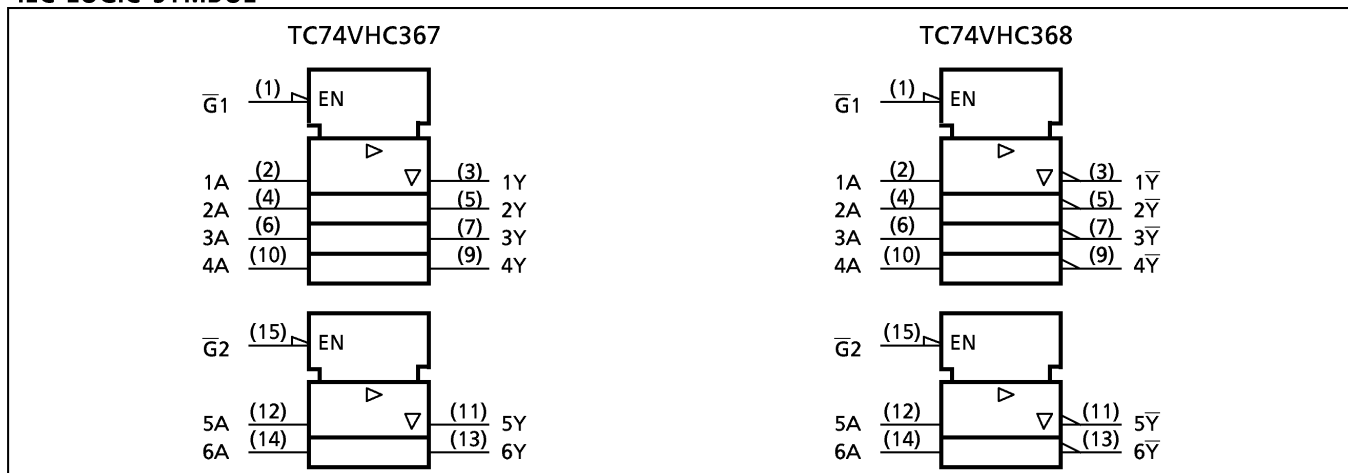


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**IEC LOGIC SYMBOL**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 ( $V_{CC} = 3.3 \pm 0.3V$ ) 0~20 ( $V_{CC} = 5 \pm 0.5V$ )	ns / V

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**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V <sub>IH</sub>		2.0 3.0~ 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	—	V	
Low - Level Input Voltage	V <sub>IL</sub>		2.0 3.0~ 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I <sub>OH</sub> = -4mA I <sub>OH</sub> = -8mA	4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4mA I <sub>OL</sub> = 8mA	4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	± 0.25	—	± 2.50	μA	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND	0~5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0		

**AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 3ns$  )**

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (TC74VHC367)	t <sub>pLH</sub>	3.3 ± 0.3	15	—	5.9	8.3	1.0	10.0	ns
			50	—	8.4	11.8	1.0	13.5	
	t <sub>pHL</sub>	5.0 ± 0.5	15	—	4.1	5.9	1.0	7.0	
			50	—	5.6	7.9	1.0	9.0	
Propagation Delay Time (TC74VHC368)	t <sub>pLH</sub>	3.3 ± 0.3	15	—	5.3	7.5	1.0	9.0	
			50	—	7.8	11.0	1.0	12.5	
	t <sub>pHL</sub>	5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	
			50	—	5.3	7.5	1.0	8.5	
3-State Output Enable Time	t <sub>pZL</sub>	RL = 1kΩ	3.3 ± 0.3	15	—	6.8	10.5	1.0	12.5
				50	—	9.3	14.0	1.0	16.0
	t <sub>pZH</sub>		5.0 ± 0.5	15	—	4.8	7.2	1.0	8.5
				50	—	6.3	9.2	1.0	10.5
3-State Output Disable Time	t <sub>pLZ</sub>	RL = 1kΩ	3.3 ± 0.3	50	—	9.9	13.6	1.0	15.5
				50	—	6.3	9.2	1.0	10.5
t <sub>pHZ</sub>	5.0 ± 0.5		50	—	6.3	9.2	1.0	10.5	
			50	—	6.3	9.2	1.0	10.5	
Output to Output Skew	t <sub>osLH</sub>	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5
				50	—	—	1.0	—	1.0
t <sub>osHL</sub>	5.0 ± 0.5		50	—	—	1.0	—	1.0	
			50	—	—	1.0	—	1.0	
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	pF
Output Capacitance	C <sub>OUT</sub>			—	6	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 2)		—	19	—	—	—	

Note (1) Parameter guaranteed by design.  $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

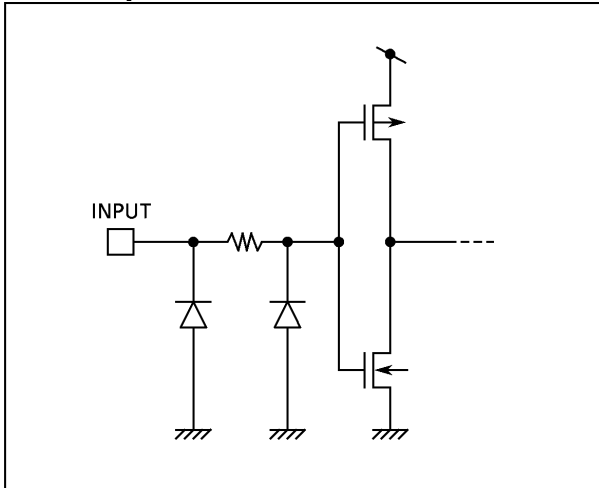
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per bit)}$$

**NOISE CHARACTERISTICS ( Input  $t_r = t_f = 3ns$  )**

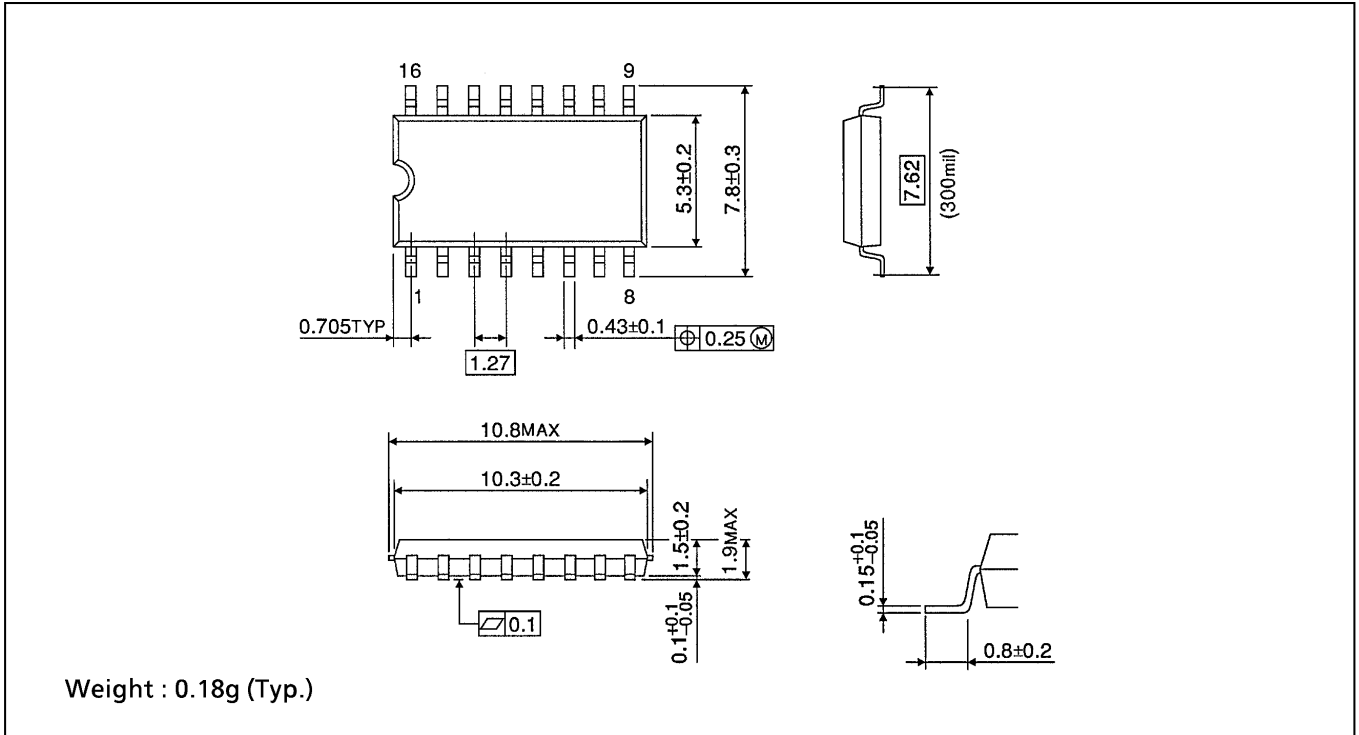
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
		V <sub>CC</sub> (V)		TYP.	MAX.	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50pF	5.0	—	1.5	V

**INPUT EQUIVALENT CIRCUIT**



**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

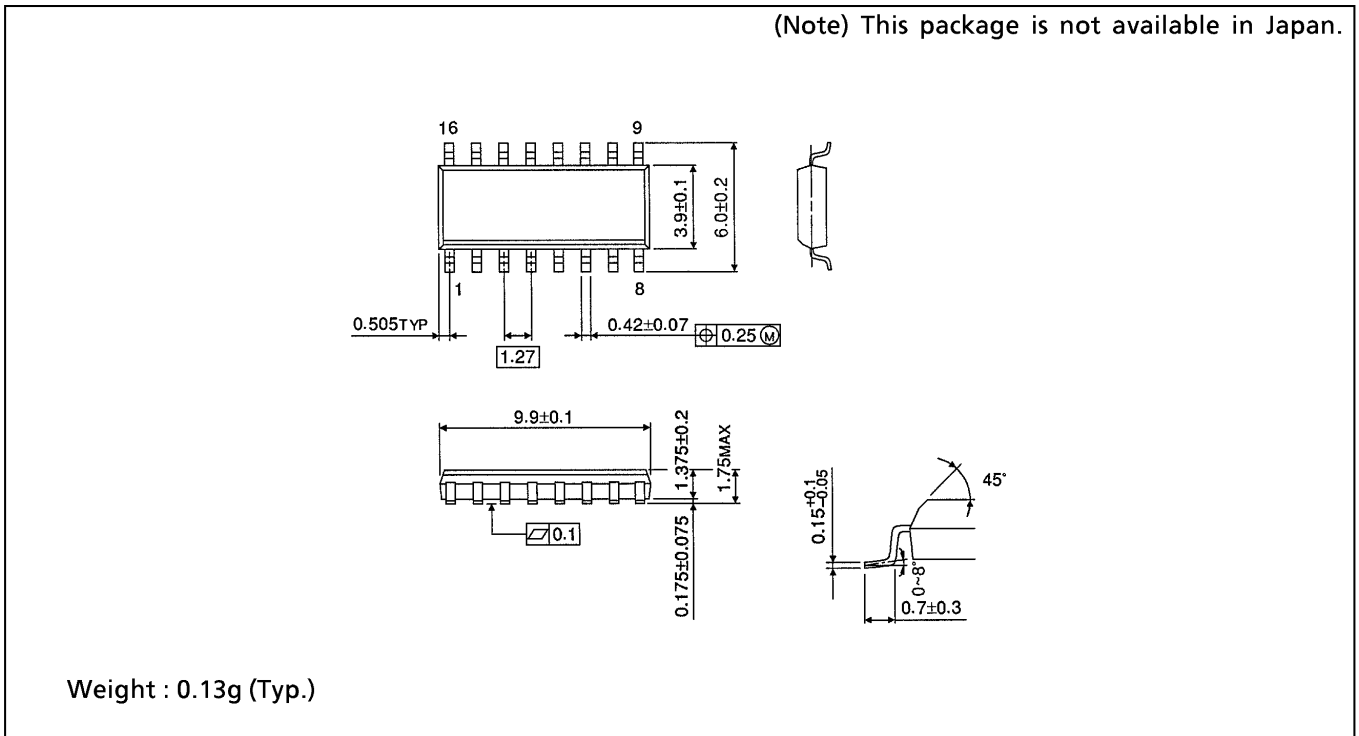
Unit in mm



**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOP16-P-150-1.27)**

Unit in mm

(Note) This package is not available in Japan.



TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm

