May 1998

FAIRCHILD SEMICONDUCTOR TM

74LVQ374
Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The LVQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

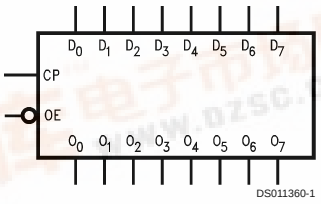
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- 3-STATE outputs drive bus lines or buffer memory address registers

Ordering Code:

Order Number	Package Number	Package Description
74LVQ374SC	M20B	20-Lead (0.300" Wide) Molded Small Outline Package, SOIC JEDEC
74LVQ374SJ	M20D	20-Lead Molded Shrink Small Outline Package, SOIC EIAJ
74LVQ374QSC	MQA20	20-Lead (0.150" Wide) Molded Shrink Small Outline Package, SOIC JEDEC

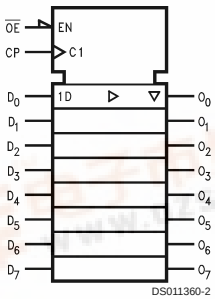
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



DS011360-1

IEEE/IEC



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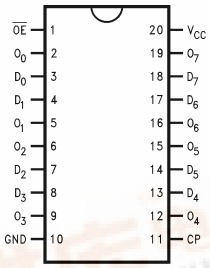
Connection Diagram

Pin Assignment for SOIC and QSOP



DS011360-3

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

Truth Table

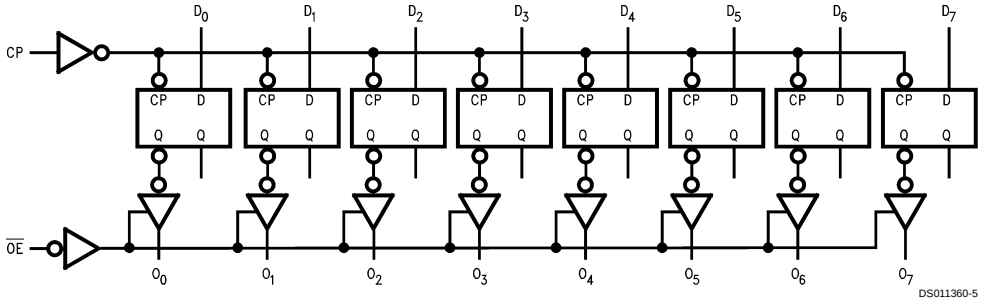
Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Functional Description

The LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40˚C to +85˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C		T_A = −40˚C to +85˚C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 µA
		3.0		2.58	2.48	V	V_{IN} = V_{IL} or V_{IH} (Note 3) I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		3.0		0.36	0.44	V	V_{IN} = V_{IL} or V_{IH} (Note 3) I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	µA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic	3.6			36	mA	V_{OLD} = 0.8V Max (Note 5)
I_{OHD}	Output Current (Note 4)	3.6			−25	mA	V_{OHD} = 2.0V Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	µA	V_{IN} = V_{CC} or GND
I_{OZ}	Maximum 3-STATE Leakage Current	3.6		±0.25	±2.5	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8		V	(Notes 6, 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8		V	(Notes 6, 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 6, 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 6, 8)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	2.7	55			50		MHz
		3.3 ±0.3	75			70		
t_{PLH}	Propagation Delay	2.7	3.0	11.4	18.3	3.0	19.0	ns
t_{PHL}	CP to O_n	3.3 ±0.3	3.0	9.5	13.0	3.0	13.5	
t_{PZL}	Output Enable Time	2.7	3.0	11.4	18.3	3.0	19.0	ns
t_{PZH}		3.3 ±0.3	3.0	9.5	13.0	3.0	13.5	
t_{PHZ}	Output Disable Time	2.7	1.0	11.4	20.4	1.0	21.0	ns
t_{PLZ}		3.3 ±0.3	1.0	9.5	14.5	1.0	15.0	
t_{OSHL}	Output to Output Skew (Note 9)	2.7		1.0	1.5		1.5	ns
t_{OSLH}	CP to O_n	3.3 ±0.3		1.0	1.5		1.5	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

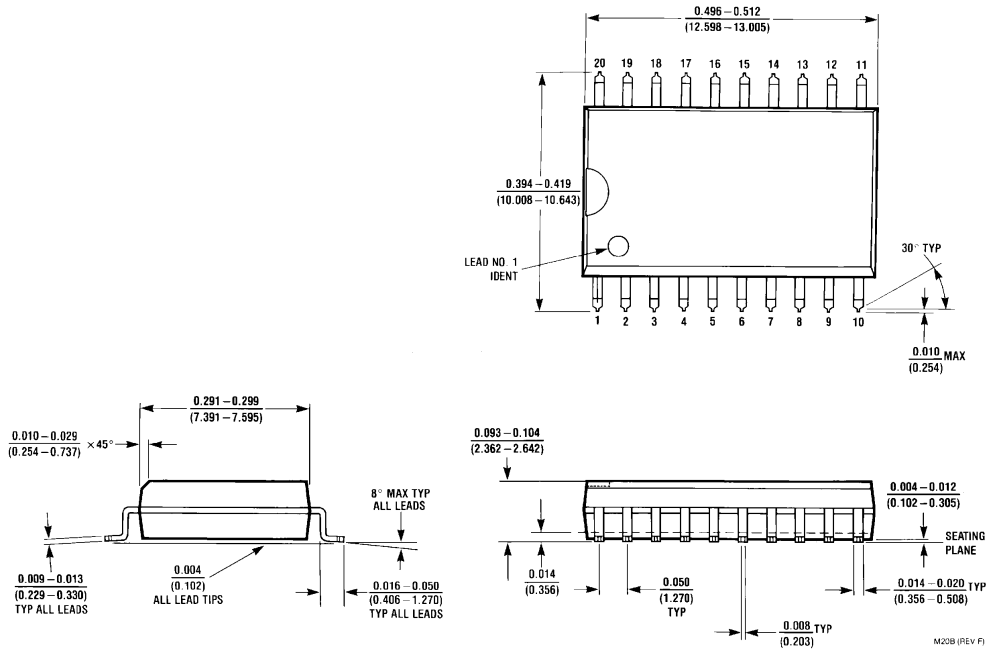
Symbol	Parameter	V_{CC} (V)	T_A = +25°C, C_L = 50 pF		T_A = 40°C− to +85°C, C_L = 50 pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW	2.7	0	4.0	4.5	ns
	D_n to CP	3.3 ±0.3	0	3.0	3.0	
t_H	Hold Time, HIGH or LOW	2.7	0	1.5	1.5	ns
	D_n to CP	3.3 ±0.3	0	1.5	1.5	
t_W	CP Pulse Width,	2.7	2.4	5.0	6.0	ns
	HIGH or LOW	3.3 ±0.3	2.0	4.0	4.0	

Capacitance

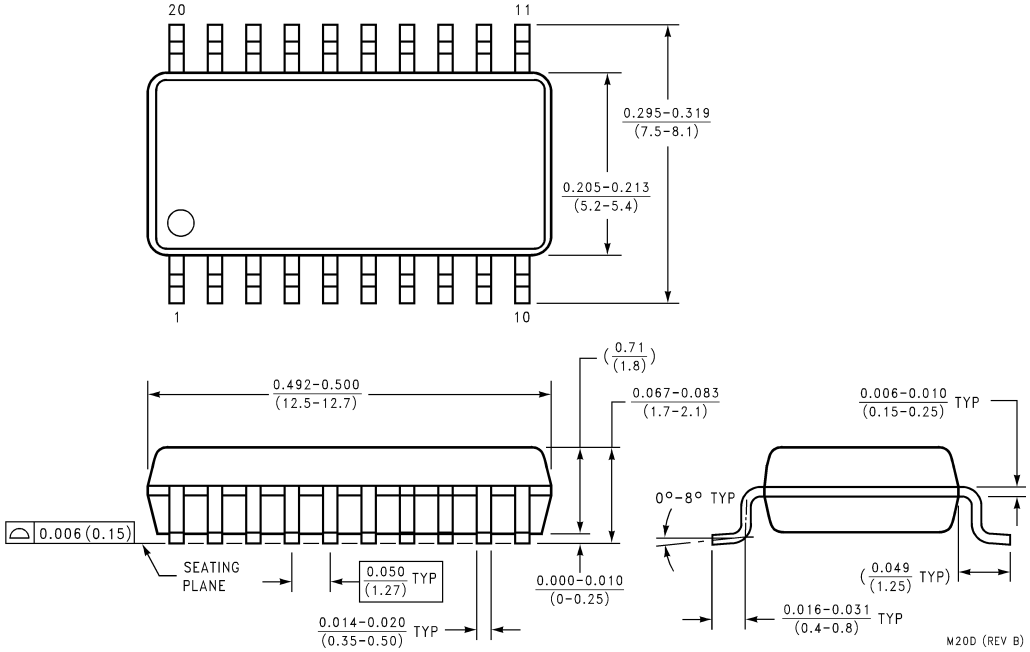
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 10)	Power Dissipation Capacitance	39	pF	V_{CC} = 3.3V

Note 10: C_{PD} is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted

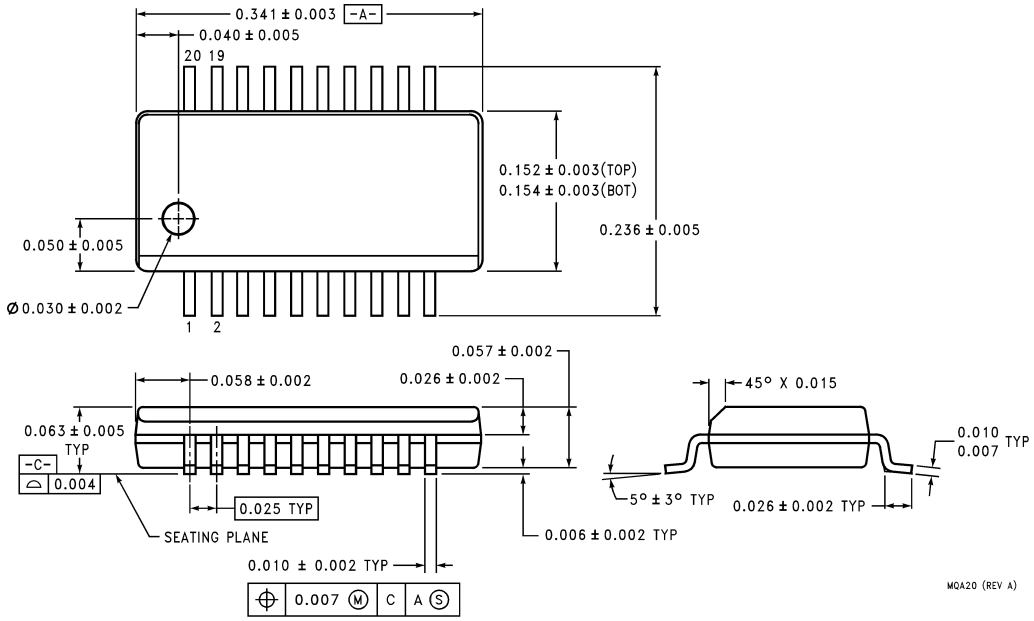


20-Lead (0.300" Wide) Molded Small Outline Package, SOIC JEDEC
Package Number M20B



20-Lead Molded Shrink Small Outline Package, SOIC EIAJ
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead (0.150" Wide) Molded Shrink Small Outline Package, SOIC JEDEC
(also known as QSOP)
Package Number MQA20

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