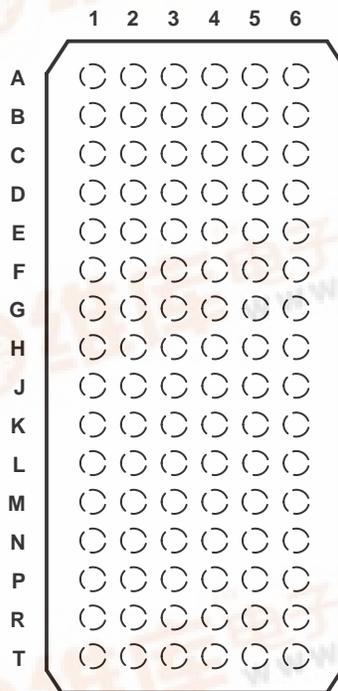


SN74LVTH32374 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS752B – SEPTEMBER 2000 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus+™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Unregulated Battery Operation Down to 2.7 V

GKE OR ZKE PACKAGE
(TOP VIEW)



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|-----|------------------|------------------|-----|-----|
| A | 1Q2 | 1Q1 | $\overline{1OE}$ | 1CLK | 1D1 | 1D2 |
| B | 1Q4 | 1Q3 | GND | GND | 1D3 | 1D4 |
| C | 1Q6 | 1Q5 | 1V _{CC} | 1V _{CC} | 1D5 | 1D6 |
| D | 1Q8 | 1Q7 | GND | GND | 1D7 | 1D8 |
| E | 2Q2 | 2Q1 | GND | GND | 2D1 | 2D2 |
| F | 2Q4 | 2Q3 | 1V _{CC} | 1V _{CC} | 2D3 | 2D4 |
| G | 2Q6 | 2Q5 | GND | GND | 2D5 | 2D6 |
| H | 2Q7 | 2Q8 | $\overline{2OE}$ | 2CLK | 2D8 | 2D7 |
| J | 3Q2 | 3Q1 | $\overline{3OE}$ | 3CLK | 3D1 | 3D2 |
| K | 3Q4 | 3Q3 | GND | GND | 3D3 | 3D4 |
| L | 3Q6 | 3Q5 | 2V _{CC} | 2V _{CC} | 3D5 | 3D6 |
| M | 3Q8 | 3Q7 | GND | GND | 3D7 | 3D8 |
| N | 4Q2 | 4Q1 | GND | GND | 4D1 | 4D2 |
| P | 4Q4 | 4Q3 | 2V _{CC} | 2V _{CC} | 4D3 | 4D4 |
| R | 4Q6 | 4Q5 | GND | GND | 4D5 | 4D6 |
| T | 4Q7 | 4Q8 | $\overline{4OE}$ | 4CLK | 4D8 | 4D7 |

description/ordering information

The SN74LVTH32374 is a 32-bit edge-triggered D-type flip-flop designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-----------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | LFBGA – GKE | Tape and reel | SN74LVTH32374GKER | HV374 |
| | LFBGA – ZKE (Pb-free) | | SN74LVTH32374ZKER | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description /ordering information (continued)

This device can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

FUNCTION TABLE
(each 8-bit flip-flop)

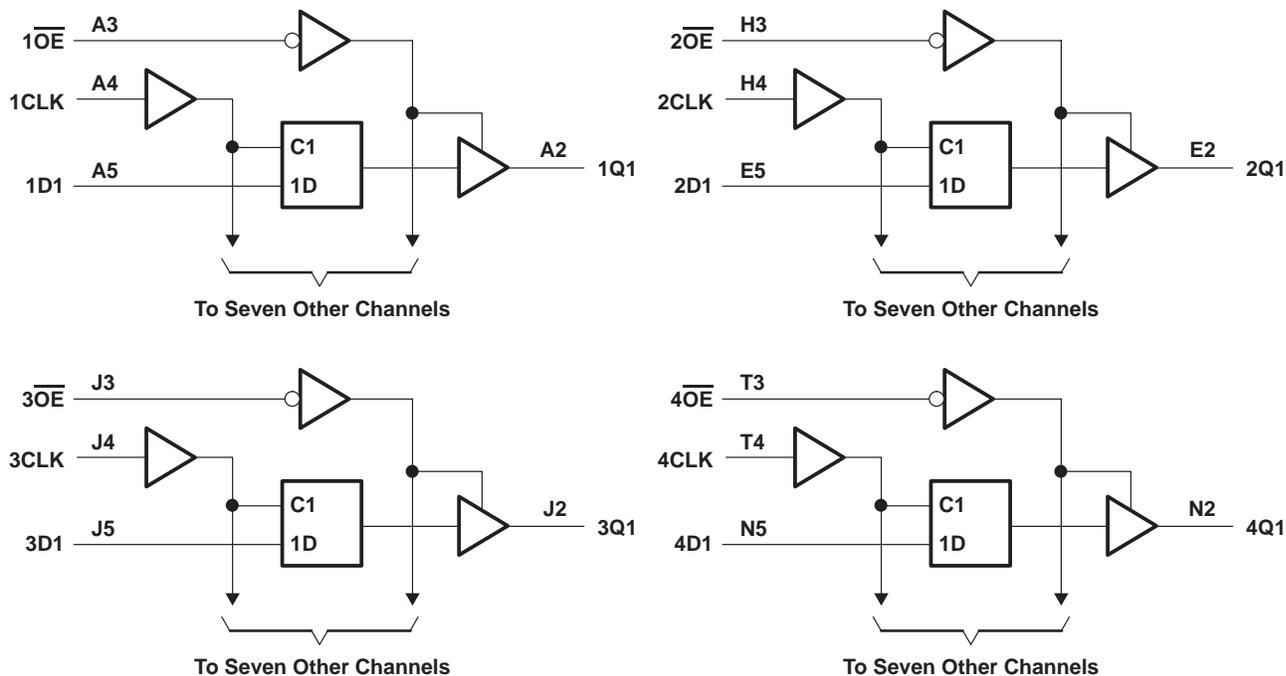
| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): GKE/ZKE package | 40°C/W |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----|-----|-----------------|
| V _{CC} | Supply voltage | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | V |
| V _I | Input voltage | | 5.5 | V |
| I _{OH} | High-level output current | | -32 | mA |
| I _{OL} | Low-level output current | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | ns/V |
| | | | | Outputs enabled |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | μs/V |
| T _A | Operating free-air temperature | -40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|--------------------|--|--|--|------------------------------|------|-----------|---------------|---------|
| V_{IK} | | $V_{CC} = 2.7\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V | |
| V_{OH} | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$, | $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{CC}-0.2$ | | | V | |
| | | $V_{CC} = 2.7\text{ V}$, | $I_{OH} = -8\text{ mA}$ | 2.4 | | | | |
| | | $V_{CC} = 3\text{ V}$, | $I_{OH} = -32\text{ mA}$ | 2 | | | | |
| V_{OL} | | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\text{ }\mu\text{A}$ | | | 0.2 | V | |
| | | | $I_{OL} = 24\text{ mA}$ | | | 0.5 | | |
| | | $V_{CC} = 3\text{ V}$ | $I_{OL} = 16\text{ mA}$ | | | 0.4 | | |
| | | | $I_{OL} = 32\text{ mA}$ | | | 0.5 | | |
| | | | $I_{OL} = 64\text{ mA}$ | | | 0.55 | | |
| I_I | | $V_{CC} = 0\text{ or }3.6\text{ V}$, | $V_I = 5.5\text{ V}$ | | | 10 | μA | |
| | | Control inputs | $V_{CC} = 3.6\text{ V}$, | $V_I = V_{CC}\text{ or GND}$ | | | | ± 1 |
| | | Data inputs | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}$ $V_I = 0$ | | | | 1 -5 |
| I_{off} | | $V_{CC} = 0$, | $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | ± 100 | μA | |
| $I_I(\text{hold})$ | | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | | | 75 | μA | |
| | | | $V_I = 2\text{ V}$ | | | -75 | | |
| | | $V_{CC} = 3.6\text{ V, }^\ddagger$ | $V_I = 0\text{ to }3.6\text{ V}$ | | | ± 500 | | |
| I_{OZH} | | $V_{CC} = 3.6\text{ V}$, | $V_O = 3\text{ V}$ | | | 5 | μA | |
| I_{OZL} | | $V_{CC} = 3.6\text{ V}$, | $V_O = 0.5\text{ V}$ | | | -5 | μA | |
| I_{OZPU} | | $V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA | |
| I_{OZPD} | | $V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μA | |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | | Outputs high | | 0.38 | mA | |
| | | | | Outputs low | | 10 | | |
| | | | | Outputs disabled | | 0.38 | | |
| ΔI_{CC}^\S | | $V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | | | | 0.2 | mA | |
| C_i | | $V_I = 3\text{ V or }0$ | | | | 3 | pF | |
| C_o | | $V_O = 3\text{ V or }0$ | | | | 9 | pF | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 3.3 \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|--------------------|---------------------------------|---------------------------------|-----|-------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 160 | | 160 | | MHz |
| t_w | Pulse duration, CLK high or low | 3 | | 3 | | ns |
| t_{su} | Setup time, data before CLK↑ | High or low | | 1.8 | 2 | ns |
| t_h | Hold time, data after CLK↑ | High or low | | 0.8 | 0.1 | ns |

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 3.3 V ± 0.3 V | | | V _{CC} = 2.7 V | | UNIT |
|--------------------|-----------------|----------------|------------------------------------|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| f _{max} | | | 160 | | | 160 | | MHz |
| t _{PLH} | CLK | Q | 1.9 | 3 | 4.5 | 5.2 | | ns |
| t _{PHL} | | | 2.1 | 2.9 | 4 | 4.2 | | |
| t _{PZH} | \overline{OE} | Q | 1.5 | 2.8 | 4.5 | 5.4 | | ns |
| t _{PZL} | | | 1.5 | 2.8 | 4.4 | 5 | | |
| t _{PHZ} | \overline{OE} | Q | 2.4 | 3.5 | 5 | 5.4 | | ns |
| t _{PLZ} | | | 2 | 3.2 | 4.6 | 4.8 | | |
| t _{sk(o)} | | | | | | 0.5 | | ns |

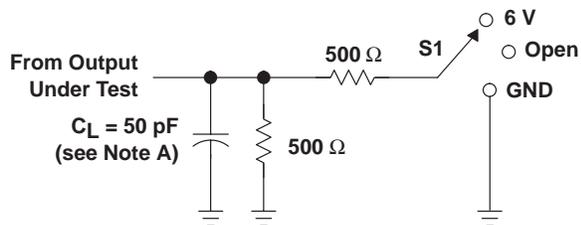
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

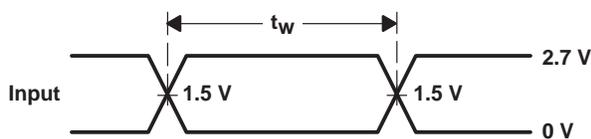
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PARAMETER MEASUREMENT INFORMATION

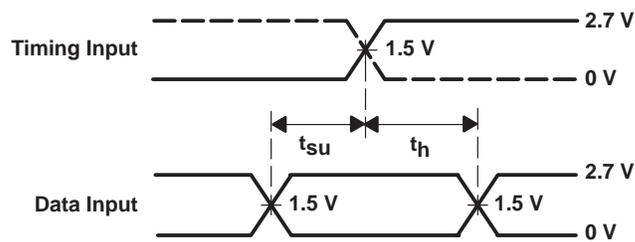


LOAD CIRCUIT

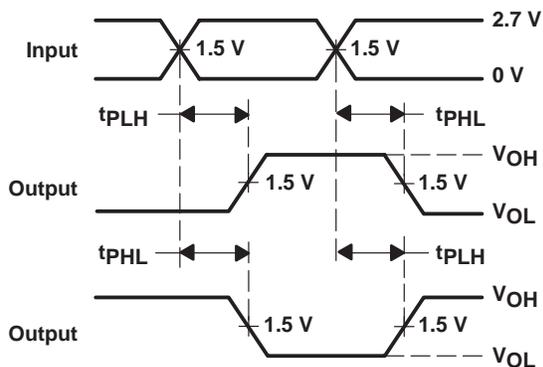
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



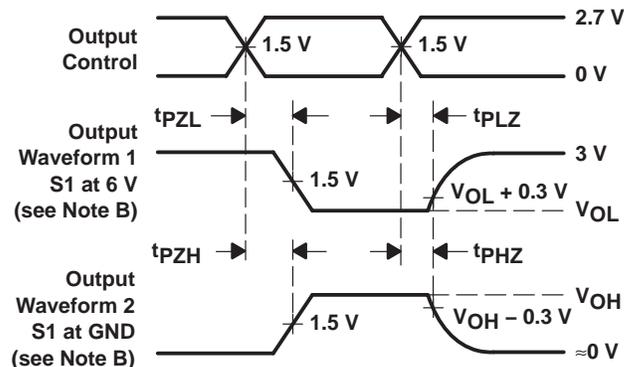
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

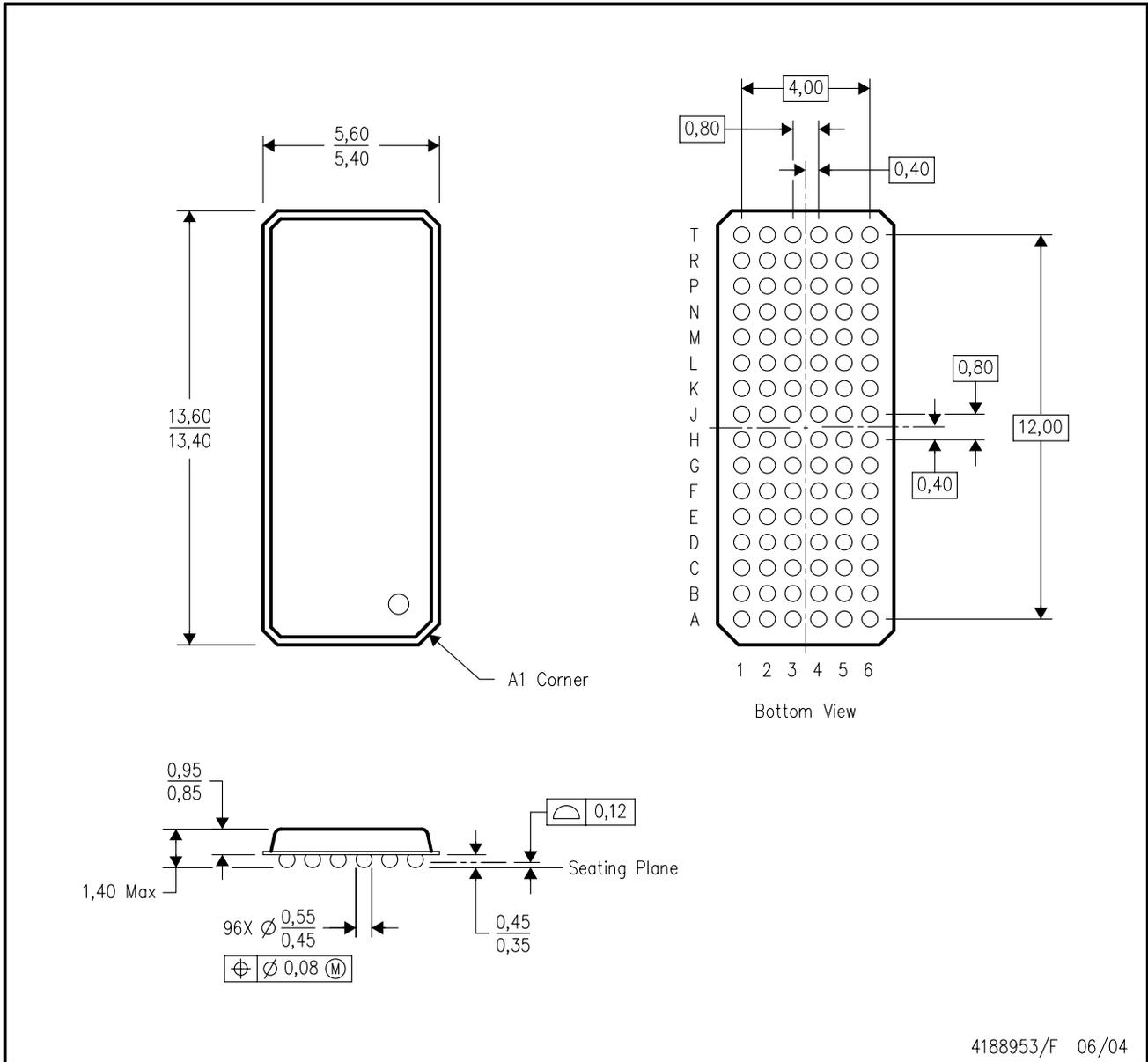
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

MECHANICAL DATA

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



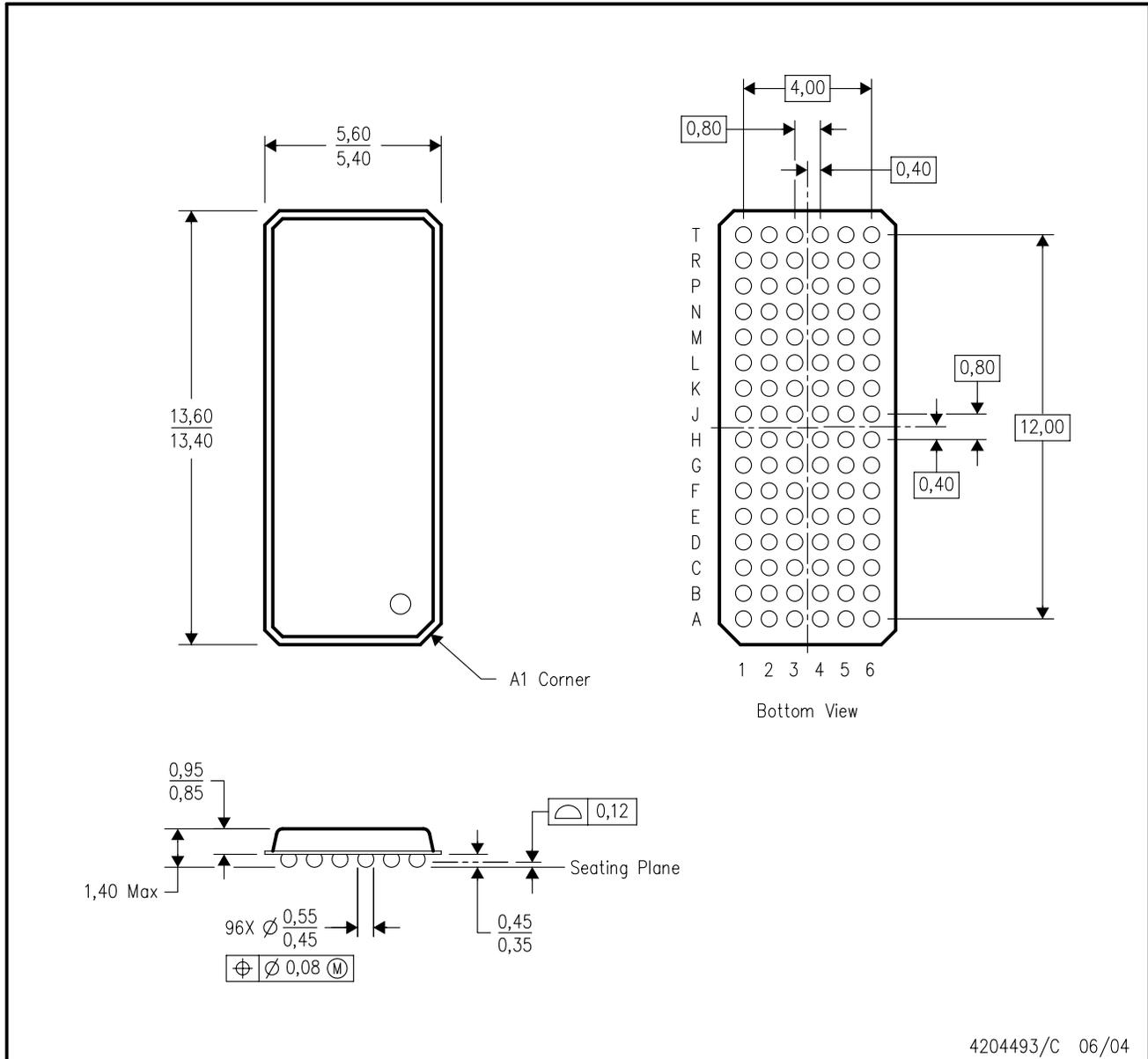
4188953/F 06/04

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-205 variation CC.
 - This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

MECHANICAL DATA

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-205 variation CC.
 - This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265