

DATA SHEET

74LVT273 3.3V Octal D flip-flop

Product specification
Supersedes data of 1994 May 11
IC23 Data Handbook

1998 Feb 19

3.3V Octal D flip-flop

74LVT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Output capability: +64mA/−32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latchup protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000V per Mil Std 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The LVT273 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

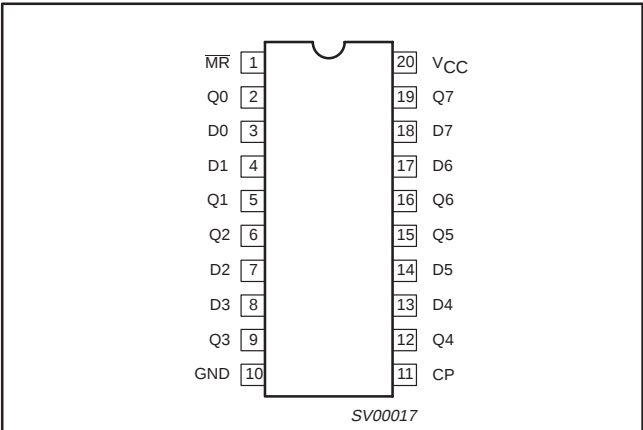
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	$C_L = 50\text{pF}; V_{CC} = 3.3\text{V}$	3.5 3.5	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or 3.0V	4	pF

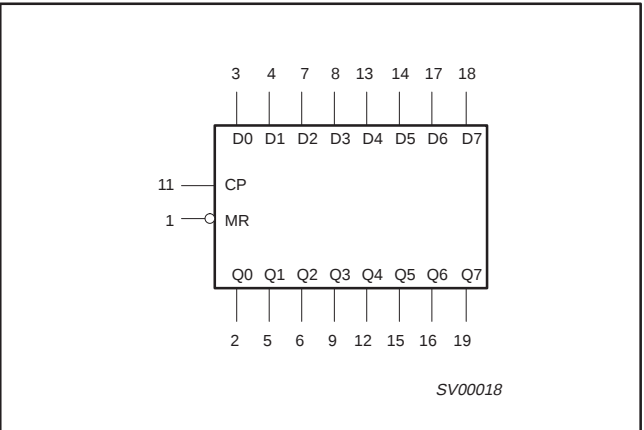
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	−40°C to +85°C	74LVT273 D	74LVT273 D	SOT163-1
20-Pin Plastic SSOP Type II	−40°C to +85°C	74LVT273 DB	74LVT273 DB	SOT339-1
20-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVT273 PW	74LVT273PW DH	SOT360-1

PIN CONFIGURATION



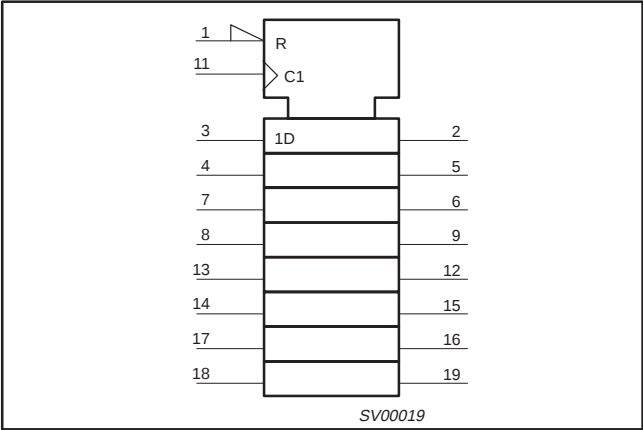
LOGIC SYMBOL



3.3V Octal D flip-flop

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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

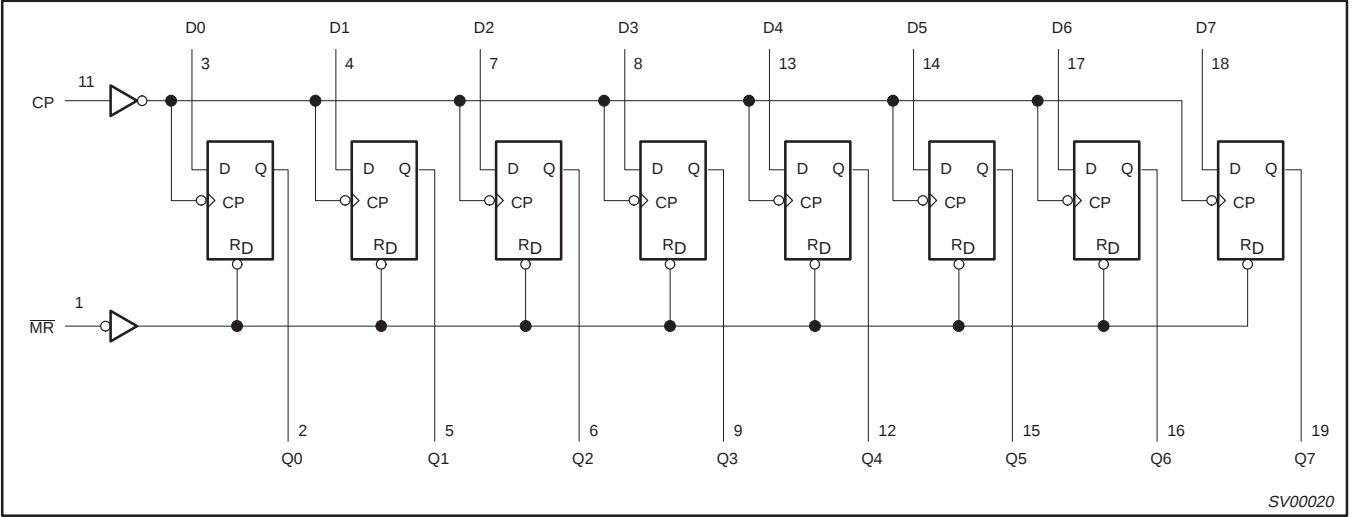
INPUTS			OUTPUTS	OPERATING MODE
MR	CP	D _n	Q0 – Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load “1”
H	↑	l	L	Load “0”
H	L	X	Q ₀	Retain state

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q₀ = Output as it was

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Data outputs
1	MR	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V _{CC}	Positive supply voltage

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage ³		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High State	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = −18mA			−0.9	−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = −100μA		V _{CC} -0.2	V _{CC} -0.1		V
		V _{CC} = 2.7V; I _{OH} = −8mA		2.4	2.5		
		V _{CC} = 3.0V; I _{OH} = −32mA		2.0	2.2		
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA			0.1	0.2	V
		V _{CC} = 2.7V; I _{OL} = 24mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 16mA			0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA			0.4	0.55	
V _{RST}	Power-up output low voltage ⁴	V _{CC} = 3.6V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55	V
I _I	Input leakage current	V _{CC} = 0 or 3.6V; V _I = 5.5V			1	10	μA
		V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		±0.1	±1	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ³		0.1	1	
		V _{CC} = 3.6V; V _I = 0			−1	−5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			1	±100	μA
I _{HOLD}	Bus Hold current A inputs ⁵	V _{CC} = 3V; V _I = 0.8V		75	150		μA
		V _{CC} = 3V; V _I = 2.0V		−75	−150		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			60	125	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.13	0.19	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			3	12	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. Unused pins at V_{CC} or GND.
4. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V	
			MIN	TYP ¹	MAX	MAX	
f _{MAX}	Maximum clock frequency	1	150				MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	1	1.7 1.9	3.5 3.5	5.5 5.5	6.3 5.9	ns
t _{PHL}	Propagation delay MR to Qn	2	1.3	3.2	6.2	6.2	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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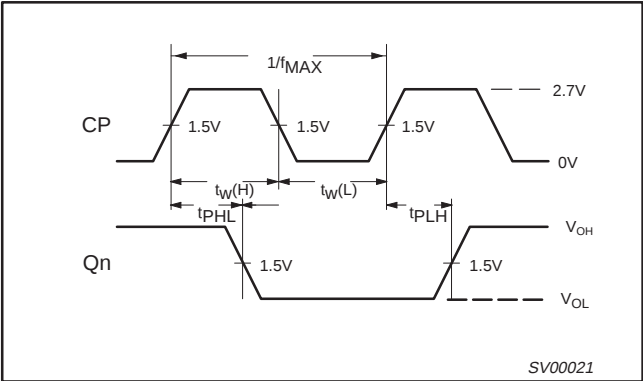
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$, $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

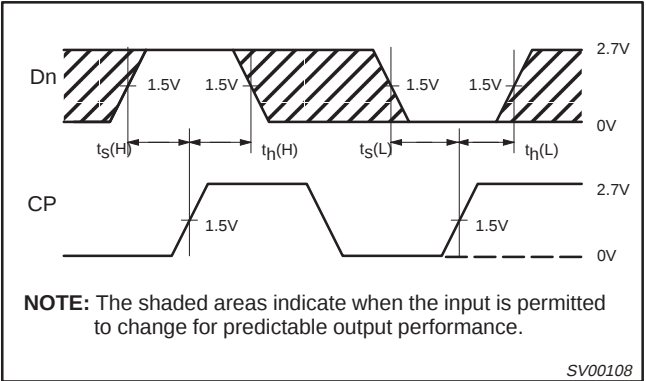
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = +3.3 \pm 0.3\text{V}$		$V_{CC} = 2.7\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to CP	3	2.3 2.3	1.0 1.0	2.7 2.7	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to CP	3	0 0	-0.6 -0.6	0 0	ns
$t_w(\text{H})$ $t_w(\text{L})$	Clock pulse width High or Low	1	3.3 3.3	1.5 1.5	3.3 3.3	ns
$t_w(\text{L})$	Master Reset pulse width, Low	2	3.3	1.5	3.3	ns
t_{REC}	Recovery time $\overline{\text{MR}}$ to CP	2	2.7	1.0	3.2	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 2.7\text{V}$

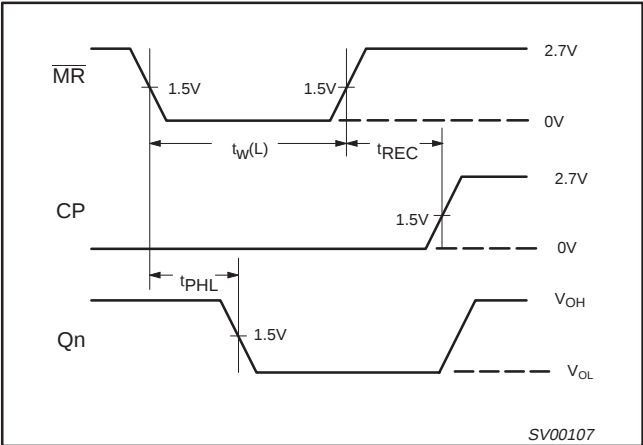


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Setup and Hold Times

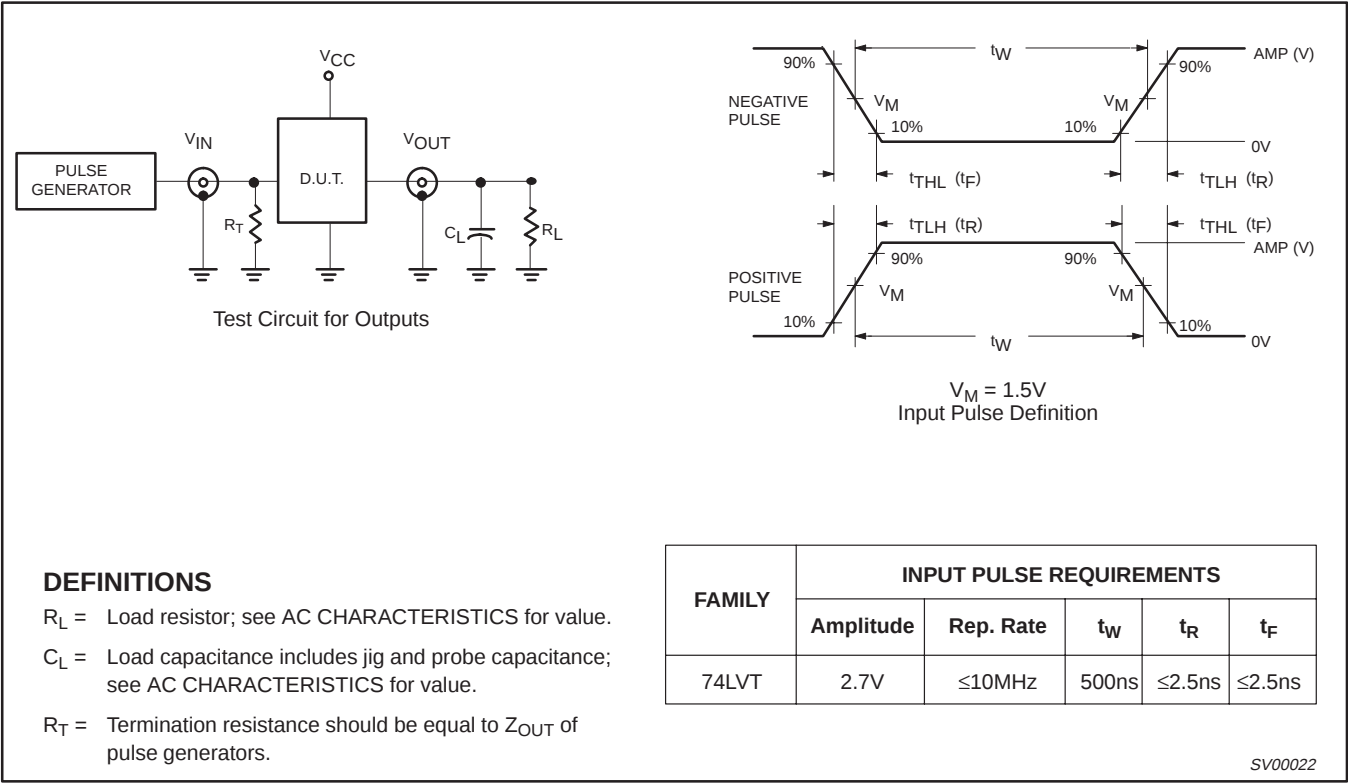


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

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TEST CIRCUIT AND WAVEFORMS

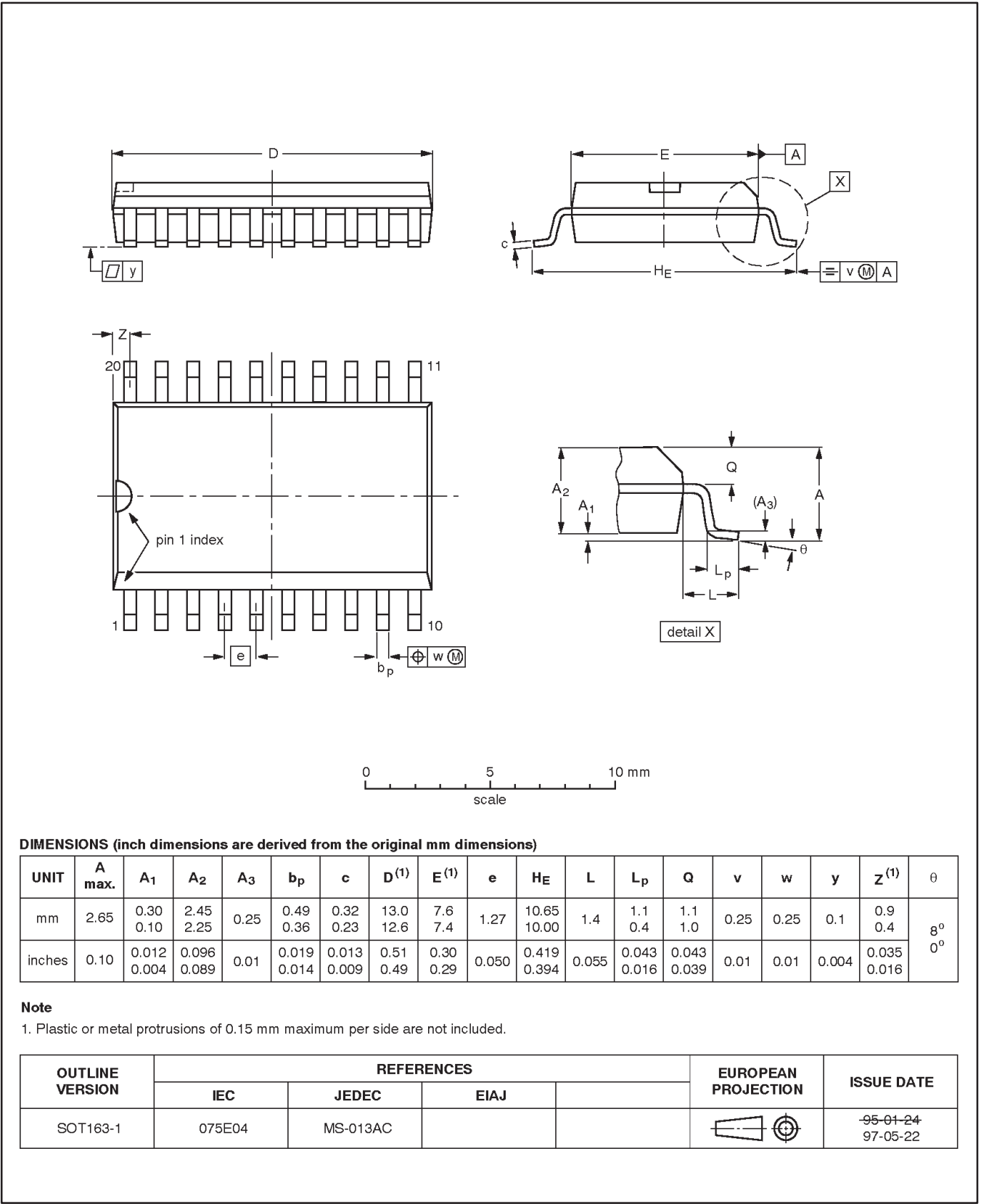


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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

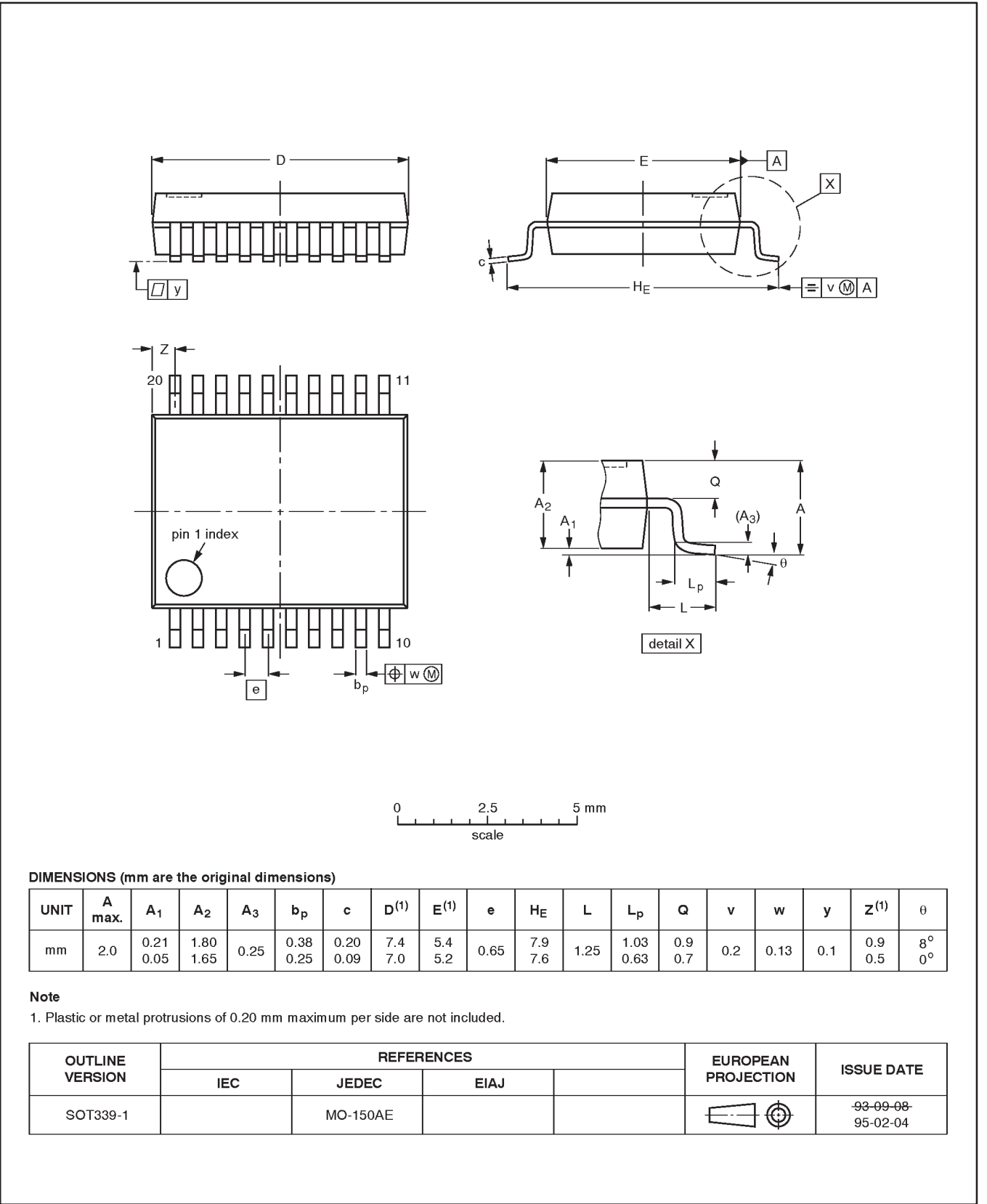


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

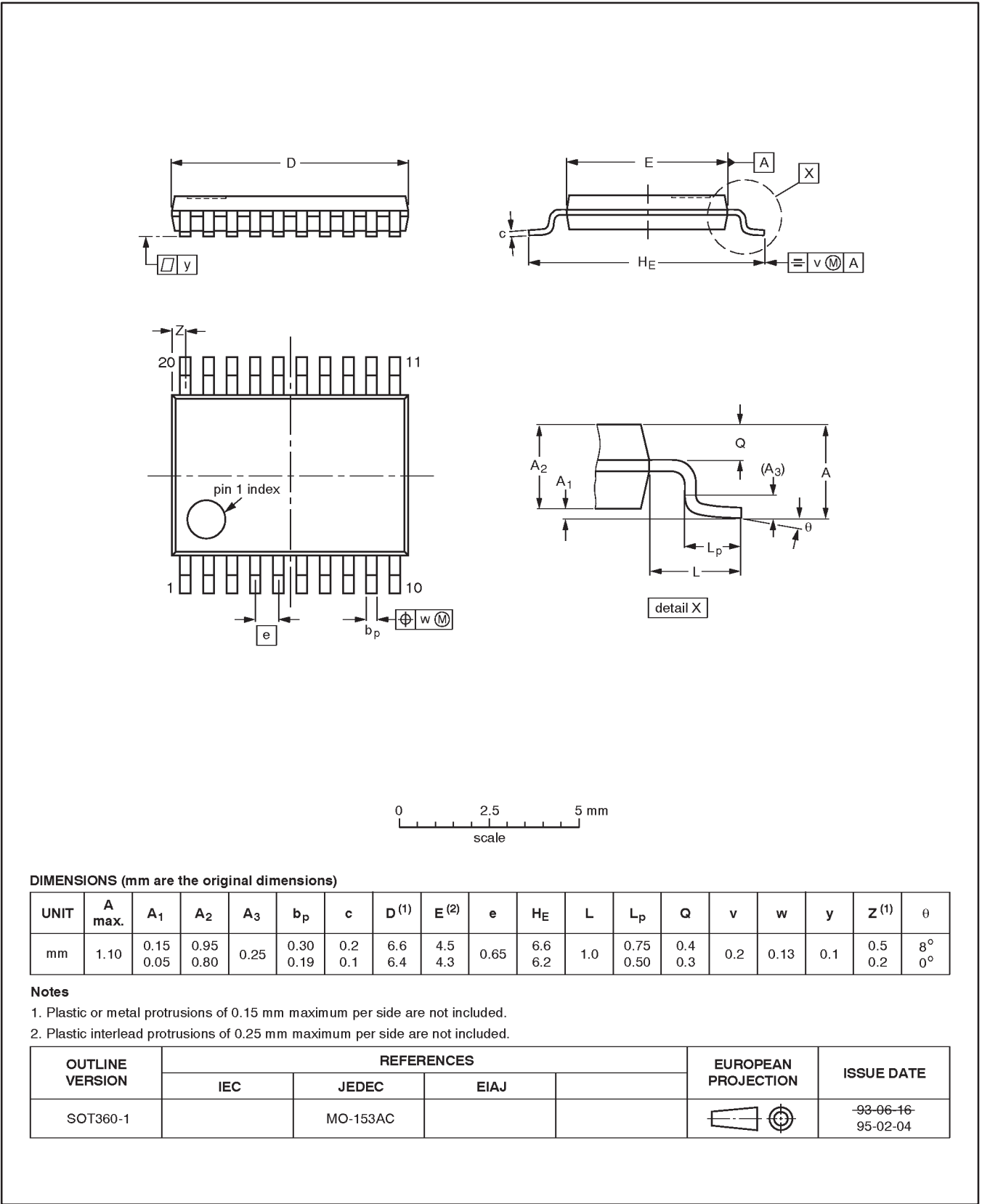


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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